

IRLR8103V

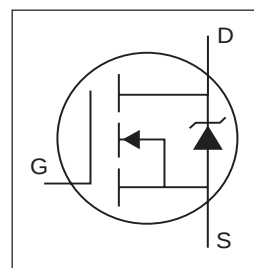
- N-Channel Application-Specific MOSFETs
- Ideal for CPU Core DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Minimizes Parallel MOSFETs for high current applications

Description

This new device employs advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make it ideal for high efficiency DC-DC converters that power the latest generation of microprocessors.

The IRLR8103V has been optimized for all parameters that are critical in synchronous buck converters including $R_{DS(on)}$, gate charge and Cdv/dt -induced turn-on immunity. The IRLR8103V offers an extremely low combination of Q_{sw} & $R_{DS(on)}$ for reduced losses in both control and synchronous FET applications.

The package is designed for vapor phase, infra-red, convection, or wave soldering techniques. Power dissipation of greater than 2W is possible in a typical PCB mount application.



DEVICE CHARACTERISTICS ⑤

IRLR8103V	
$R_{DS(on)}$	7.9m Ω
Q_G	27nC
Q_{sw}	12nC
Q_{oss}	29nC

Absolute Maximum Ratings

Parameter	Symbol	IRLR8103V	Units
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain or Source Current ($V_{GS} \geq 10V$)	$T_C = 25^\circ C$	I_D	A
	$T_C = 90^\circ C$		
Pulsed Drain Current①	I_{DM}	363	
Power Dissipation③	$T_C = 25^\circ C$	P_D	W
	$T_C = 90^\circ C$		
Junction & Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$
Continuous Source Current (Body Diode)	I_S	91	A
Pulsed Source Current①	I_{SM}	363	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	1.09	$^\circ C/W$

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Electrical Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	30	–	–	V	$V_{GS} = 0V, I_D = 250\mu A$
Static Drain-Source on Resistance	$R_{DS(on)}$		6.9	9.0	$m\Omega$	$V_{GS} = 10V, I_D = 15A$ ②
			7.9	10.5		$V_{GS} = 4.5V, I_D = 15A$ ②
Gate Threshold Voltage	$V_{GS(th)}$	1.0			V	$V_{DS} = V_{GS}, I_D = 250\mu A$
Drain-Source Leakage Current	I_{DSS}			20	μA	$V_{DS} = 24V, V_{GS} = 0$
				100		$V_{DS} = 24V, V_{GS} = 0,$ $T_j = 100^\circ C$
Gate-Source Leakage Current	I_{GSS}			± 100	nA	$V_{GS} = \pm 20V$
Total Gate Chg Cont FET	Q_G		27		nC	$V_{GS} = 5V, I_D = 15A, V_{DS} = 16V$
Total Gate Chg Sync FET	Q_G		23			$V_{GS} = 5V, V_{DS} < 100mV$
Pre-Vth Gate-Source Charge	Q_{GS1}		4.7			$V_{DS} = 16V, I_D = 15A$
Post-Vth Gate-Source Charge	Q_{GS2}		2.0			
Gate to Drain Charge	Q_{GD}		9.7			
Switch Chg($Q_{GS2} + Q_{GD}$)	Q_{SW}		12			
Output Charge	Q_{OSS}		29			$V_{DS} = 16V, V_{GS} = 0$
Gate Resistance	R_G		2.4		Ω	
Turn-on Delay Time	$t_{d(on)}$		10		ns	$V_{DD} = 16V, I_D = 15A$ $V_{GS} = 5V$ Clamped Inductive Load
Rise Time	t_r		9			
Turn-off Delay Time	$t_{d(off)}$		24			
Fall Time	t_f		18			
Input Capacitance	C_{iss}	–	2672	–	pF	$V_{DS} = 16V, V_{GS} = 0$
Output Capacitance	C_{oss}	–	1064	–		
Reverse Transfer Capacitance	C_{rss}	–	109	–		

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Units	Conditions
Diode Forward Voltage	V_{SD}		0.9	1.3	V	$I_S = 15A$ ②, $V_{GS} = 0V$
Reverse Recovery Charge④	Q_{rr}		103		nC	$di/dt \sim 700A/\mu s$ $V_{DS} = 16V, V_{GS} = 0V, I_F = 15A$
Reverse Recovery Charge (with Parallel Schottky)④	$Q_{rr(s)}$		96		nC	$di/dt = 700A/\mu s$ (with 10BQ040) $V_{DS} = 16V, V_{GS} = 0V, I_F = 15A$

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ③ When mounted on 1 inch square copper board, $t < 10$ sec.
- ④ Typ = measured - Q_{OSS}
- ⑤ Typical values of $R_{DS(on)}$ measured at $V_{GS} = 4.5V$, Q_G , Q_{SW} and Q_{OSS} measured at $V_{GS} = 5.0V$, $I_F = 15A$.

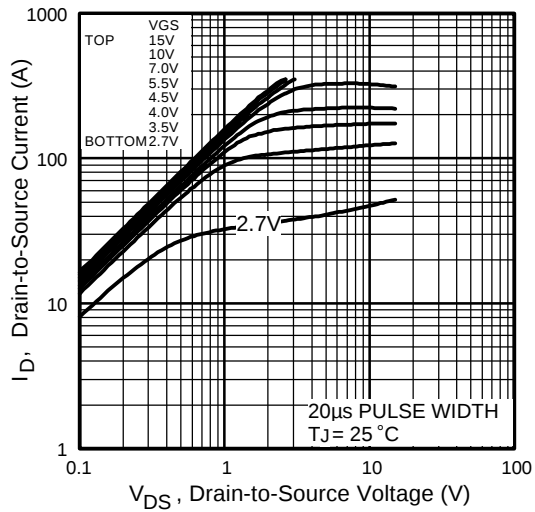


Fig 1. Typical Output Characteristics

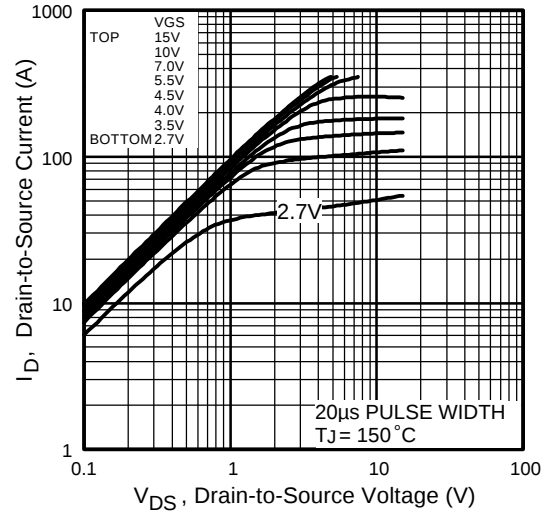


Fig 2. Typical Output Characteristics

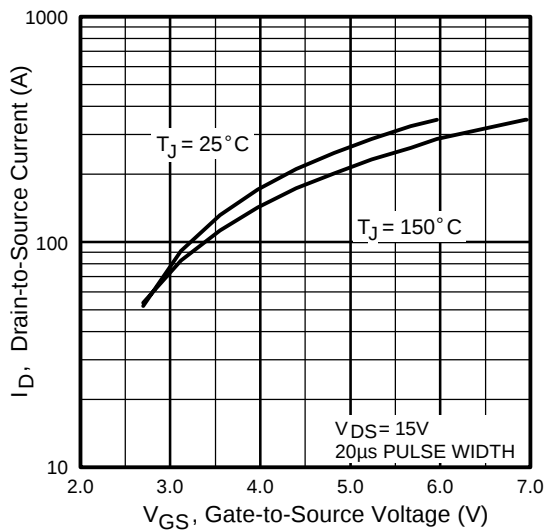


Fig 3. Typical Transfer Characteristics

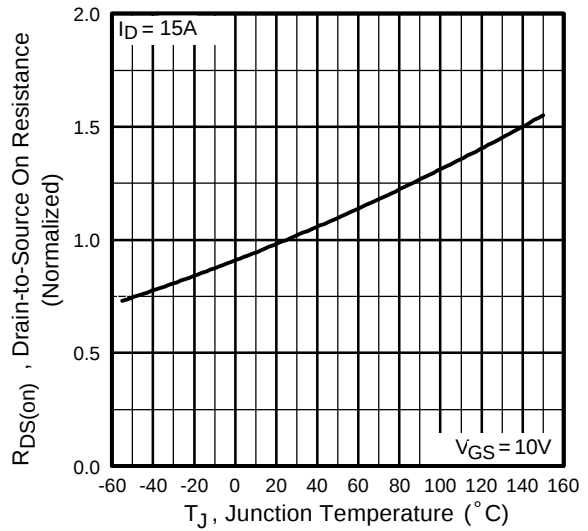


Fig 4. Normalized On-Resistance Vs. Temperature

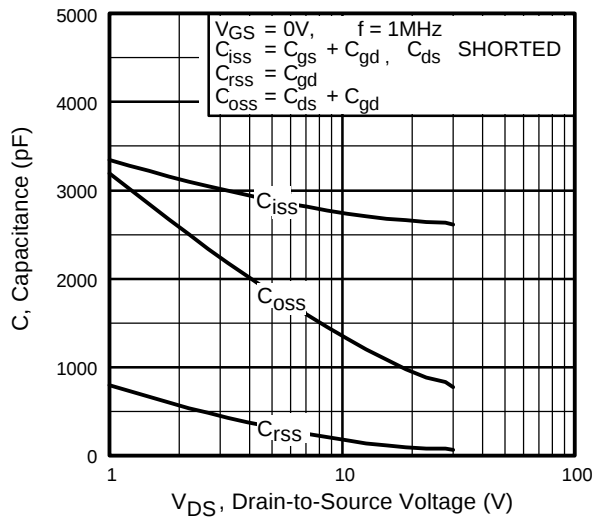


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

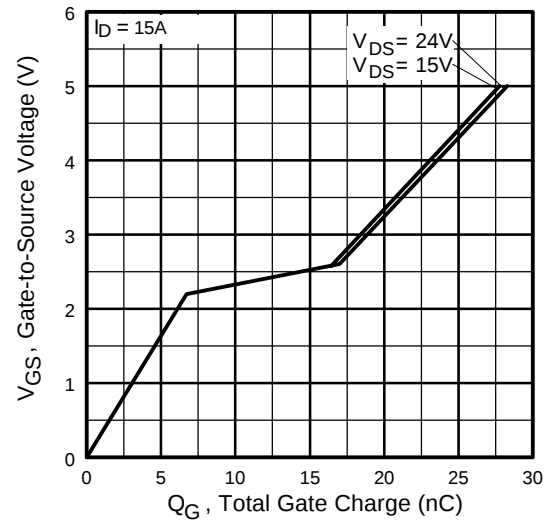


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

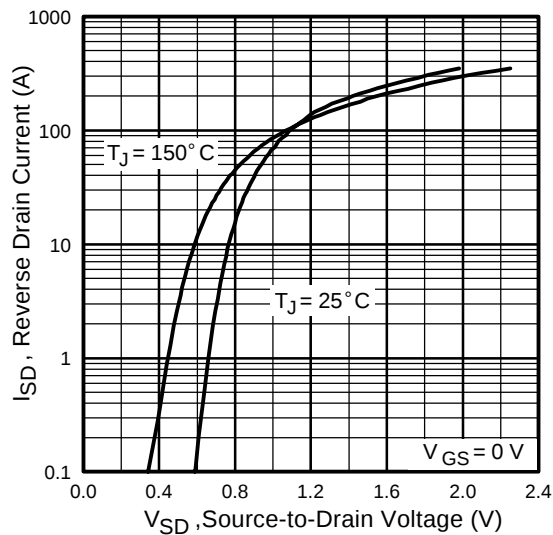


Fig 7. Typical Source-Drain Diode Forward Voltage

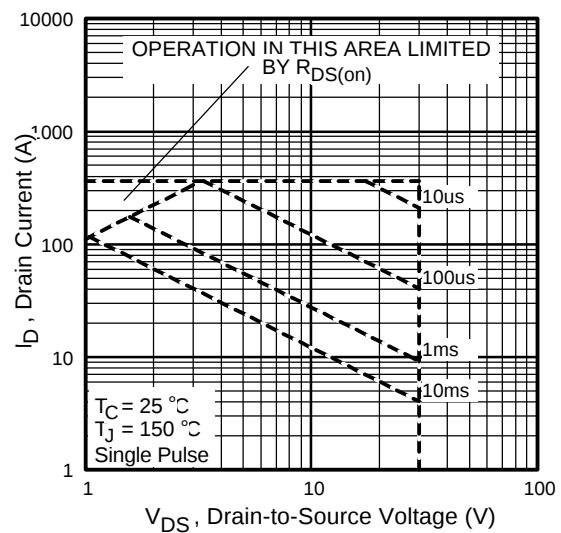


Fig 8. Maximum Safe Operating Area

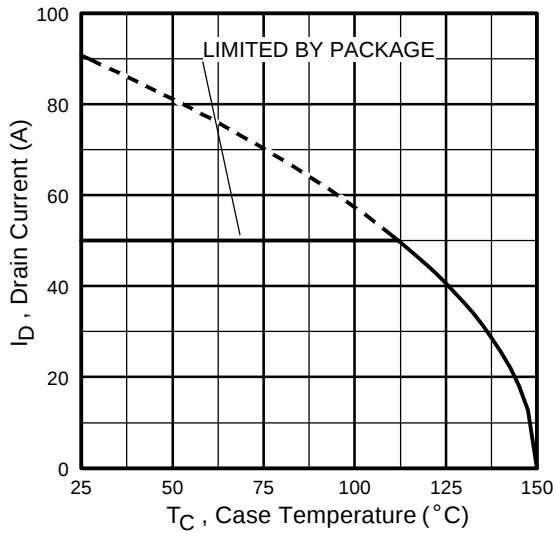


Fig 9. Maximum Drain Current Vs. Case Temperature

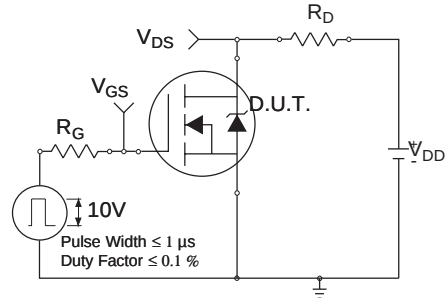


Fig 10a. Switching Time Test Circuit

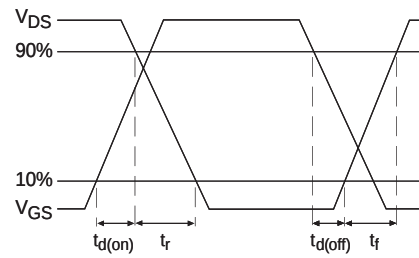


Fig 10b. Switching Time Waveforms

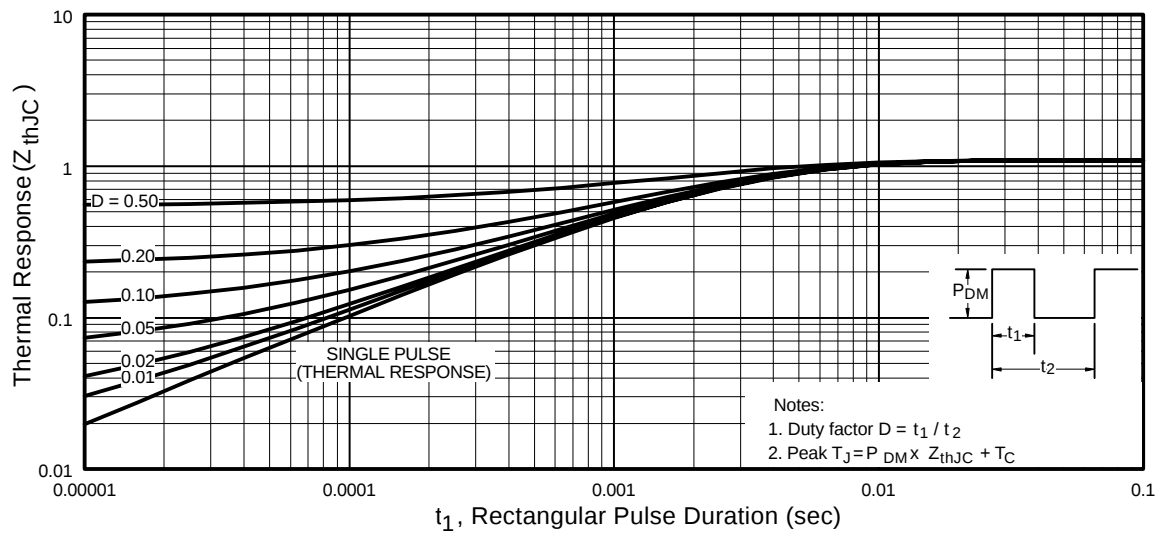


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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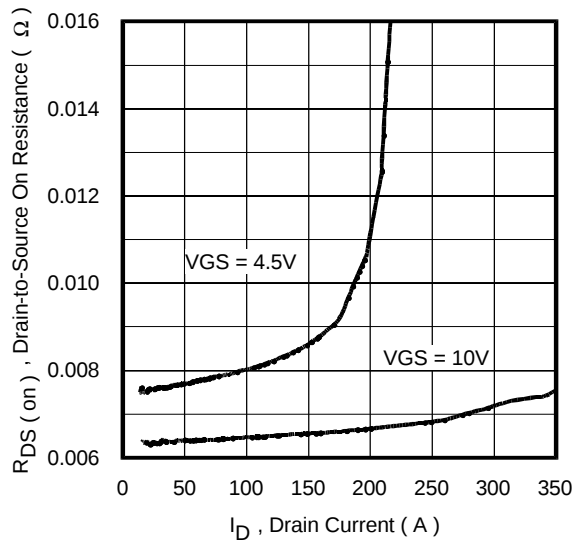


Fig 12. On-Resistance Vs. Drain Current

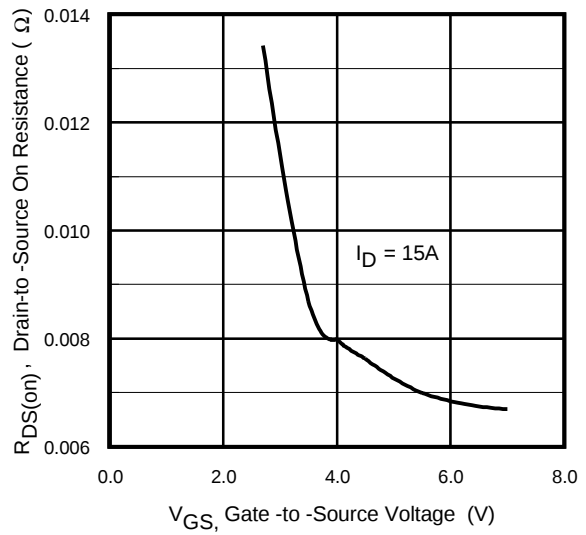


Fig 13. On-Resistance Vs. Gate Voltage

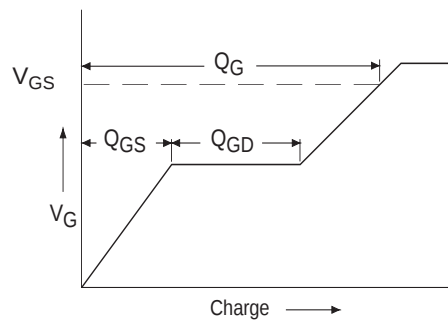
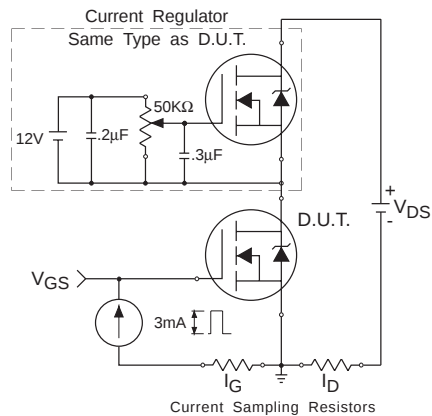
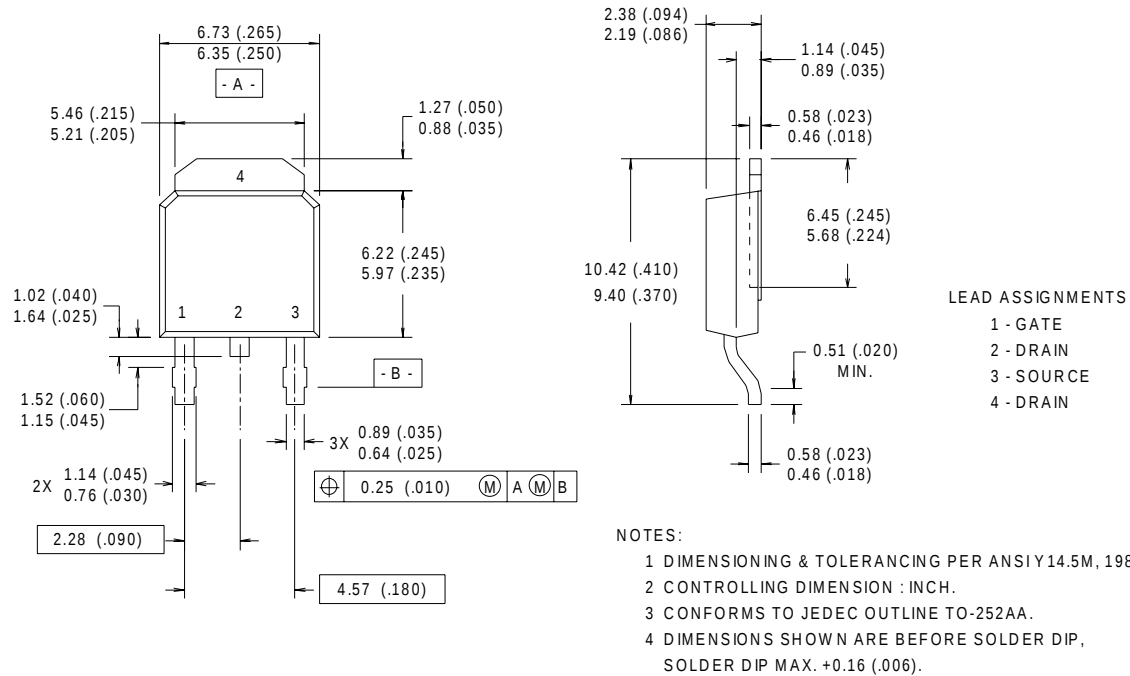


Fig 14a&b. Basic Gate Charge Test Circuit and Waveform

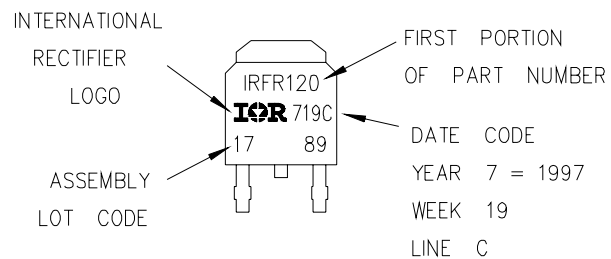
D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

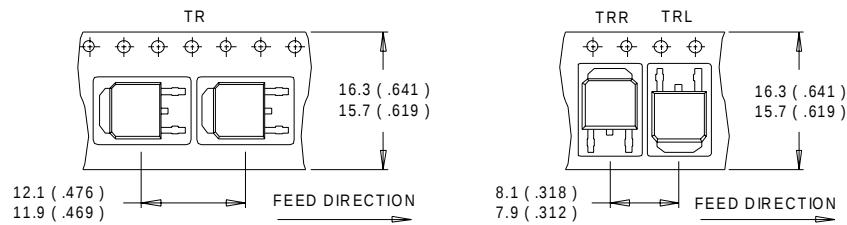


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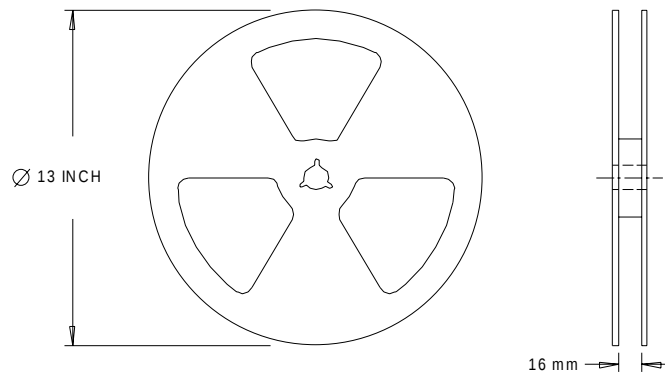
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

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IR GERMANY: Saalburgstrasse 157, 61350 Bad Homburg Tel: ++ 49 (0) 6172 96590

IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111

IR JAPAN: K&H Bldg., 2F, 30-4 Nishi-Ikebukuro 3-Chome, Toshima-Ku, Tokyo 171 Tel: 81 (0)3 3983 0086

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IR TAIWAN: 16 Fl. Suite D. 207, Sec. 2, Tun Haw South Road, Taipei, 10673 Tel: 886-(0)2 2377 9936

Data and specifications subject to change without notice.11/00