PM3386

S/UNI-2XGE

S/UNI Dual Gigabit Ethernet Controller

Reference Design

Preliminary

Issue 3: September, 2001

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1 Introduction

The PM3386 S/UNI-2xGE standard product finds application in equipment implementing high density Gigabit Ethernet Interfaces. The PM3386 has dual channel SERDES and GMAC functional blocks with embedded FIFOs that provide a high density, low power solution for direct connection to optical modules. Alternatively, a GMII interface is provided for connection to Gigabit Ethernet physical layer devices. For connectivity to upstream devices the S/UNI-2xGE supports a POS-PHY Level 3 interface which provides full bandwidth support via a 32-bit interface operating at 104MHz. The S/UNI-2xGE may find application within Multi-Service Edge and Core routers. Gigabit Ethernet is also becoming more widespread within Internet points of presence as a low cost, high speed Layer 2 interconnect solution.

The S/UNI-2xGE Reference Design provides a line card solution that can be integrated into a larger multi service reference design system via the common POS-PHY Layer 3 system interface. The line side supports independent user selectable optical or direct GMII interfacing on each channel. On the system side an FPGA provides configurable packet processing capability.

1.1 Reference Design Functionality

1. Supports one or two optical Gigabit Ethernet physical interfaces via a dual IEEE 802.3 compliant internal SERDES.

2. Provides access to a standard GMII interface for interconnection to external Gigabit Ethernet transceivers.

3. Provides a POS-PHY Level 3, 104 MHz, 32-bit System Interface to an external high-speed connector.

4. Optionally performs system side loopback of the POS-PHY Level 3 interface.

5. Initialization, configuration, control, and performance monitoring are provided via a CompactPCI bus interface.

1.2 Reference Design Features:

The reference design is based on a cPCI form factor card. The reference design will consist of:

- One PM3386 S/UNI-2xGE.
- Two Gigabit Ethernet capable Optical Transceivers.
- Access to the standard GMII interface via a high speed matched impedance connector.
- FPGA capable of supporting the 100MHz POS-PHY Level 3 interface for drop-side loop back, trfansparent or packet processing operations.

- One PLX PCI9030 Interface chip for interfacing to the host processor.
- Reference oscillators required for Gigabit Ethernet and POS-PHY L3 interfaces.
- Powered by +1.8 and +3.3 Volt supplies. +5.0 Volt components are avoided where possible.

2 Applications

The S/UNI-2xGE Reference Design demonstrates a physical interface implementation for Gigabit Ethernet that can be used in the following applications where ethernet services are deployed.

- Core/Edge Routers
- Multi-Service Switches/Routers
- SONET/SDH Transport Muxes

These applications typically integrate various interfaces including Gigabit Ethernet, ATM, SONET, or DS3. With the POS-PHY interface, numerous service cards implementing various physical layer protocols can be integrated into a common architecture implementing higher layer functions such as scheduling and traffic classification. This type of modularity increases expansion capabilities while simplifying line card development and aiding time to market.

Connections between Edge and Core Routers within a POP, or Enterprise Routers and Multi-Service switches are also becoming attractive applications for Gigabit Ethernet. Please refer to the S/UNI-2xGE Technical Overview (PMC-1991728) for more information on S/UNI-2xGE applications.

The 2xGE reference design operates in one of two modes:

- PL3 Drop Side Loop Back
- PL3 Transparent.

The following sections outline in more detail these two options.

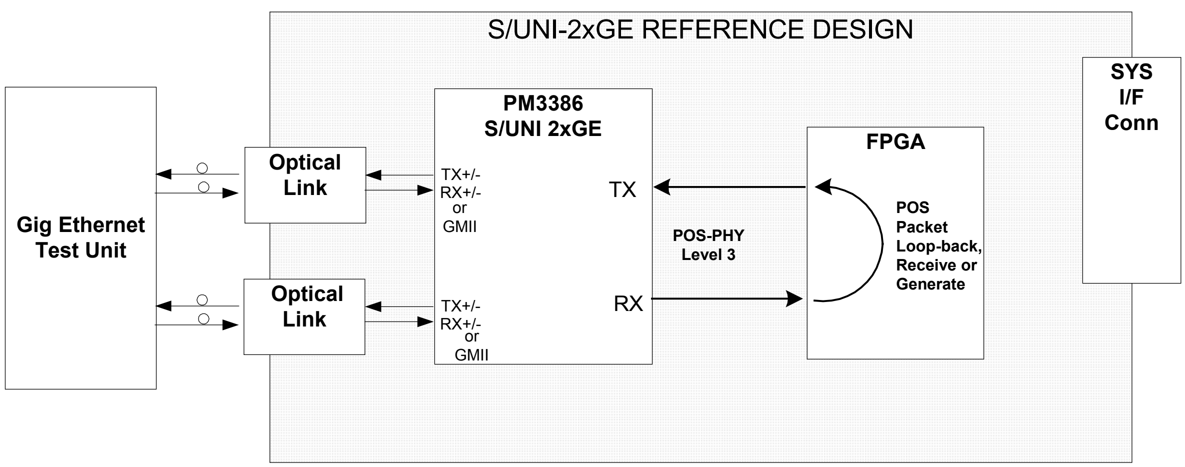
2.1 PL3 Drop Side Loop Back

Typically, the S/UNI-2xGE performs data recovery on the ingress Gigabit Ethernet streams, MAC level frame checking and then sends the frame to an upper layer device (such as an IP processor) via the POS-PHY Level 3 Interface. Extensive statistics for SNMP and RMON are maintained by the device.

On the S/UNI-2xGE Reference Design the FPGA can be used to loop the received packets back to the PL3 compliant TX interface on the PM3386. This loop back is performed on a PHY by PHY basis (i.e. each packet will be looped back to same port from which it was received.) In addition, the FPGA can be configured to generate and/or receive packets on board.

In the egress direction, the PL3 add data is formatted into physical frames with proper inter-frame gap, preamble and start of frame delimiter. The physical packet is then serialized for transmission via the optical interface or output to an external GE PHY via the GMII interface, as required.

Figure 1: PL3 Drop Side Loop Back

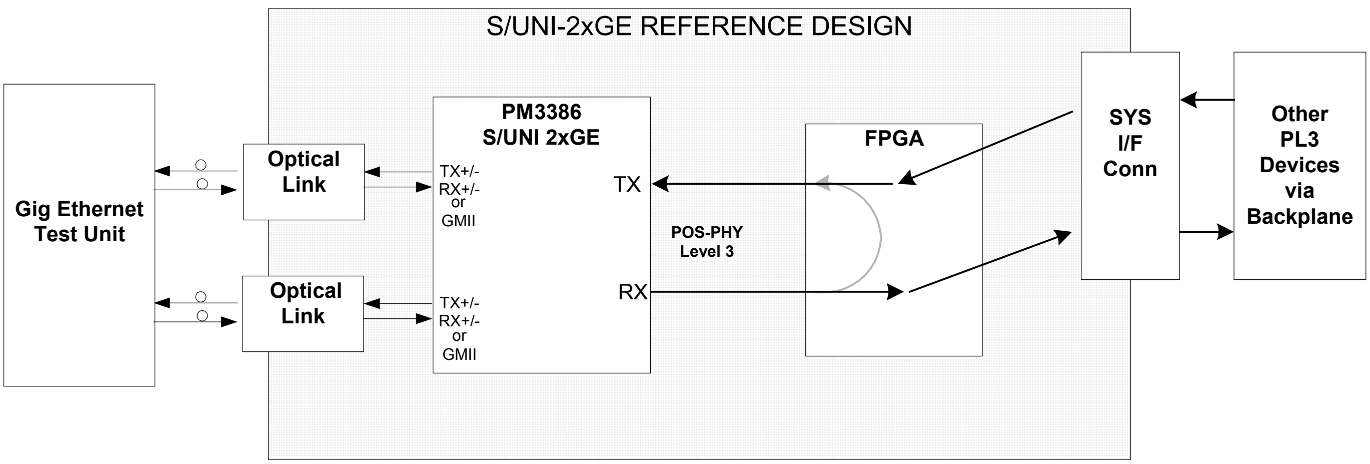


2.2 PL3 Transparent

Ingress processing will be performed identically to the PL3 Loopback mode discussed above. Upon output to the PL3 interface, the FPGA will be used to direct the packets to the POS-PHY Level 3 compliant RX interface provided via a high-speed connector. This interface will provide Ethernet frames to an external system such as an Ethernet tester or Link Layer device, as well as accept packets generated by this external system. If necessary, the FPGA can provide timing adjustments or packet processing for applications such as Ethernet over SONET. (See Application Note PMC-2001398 for more information).

The POS-PHY Level 3 compliant TX interface on the PM3386 will accept packets via the FPGA. The egress data will then be properly formatted and output to the selected Gigabit Ethernet port.

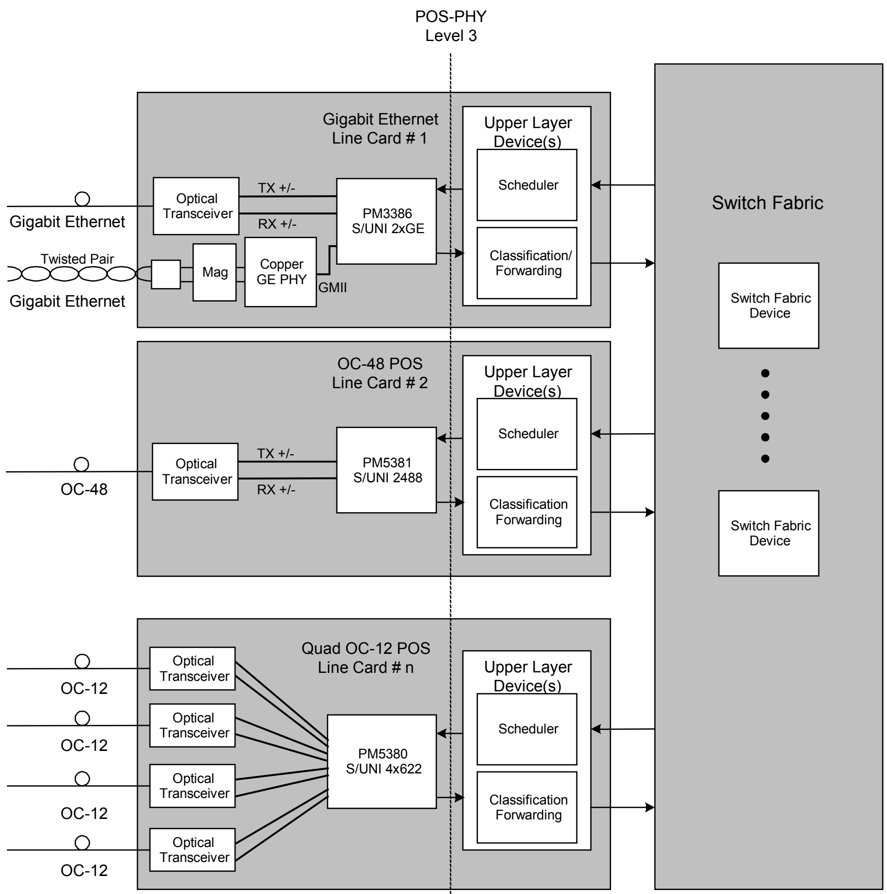
Figure 2: PL3 Transparent



2.3 Integration into a Multi-Service Reference Design System

As discussed in the Application Examples section, the S/UNI-2xGE reference design card may be implemented into a multi-service system that utilizes a number of PMC's other PL3 compliant devices. Such a system can provide multi service line interfaces including Ethernet over SONET.

Figure 3: PM3386 Multi-Service Application



3 References

1. CompactPCI™ Specification, PICMG 2.0 R2.1, September 2, 1997.

2. IEEE 802.3 Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.

3. PMC-Sierra, Inc., PMC-2001398 "Gigabit Ethernet Over SONET Using the S/UNI-2xGE", Issue 1, September, 2000.

4. PMC-Sierra, Inc., PMC-1991129 "PM3386 S/UNI-2xGE Dual Gigabit Ethernet Controller Data Sheet", Issue 5, November, 2000.

5. PMC-Sierra, Inc., PMC-980495 "POS-PHY Level 3", Issue 4, November 1999.

6. PMC-Sierra, Inc., PMC-1991728 "S/UNI-2xGE Technical Overview", Issue 1, October.

4 Definitions

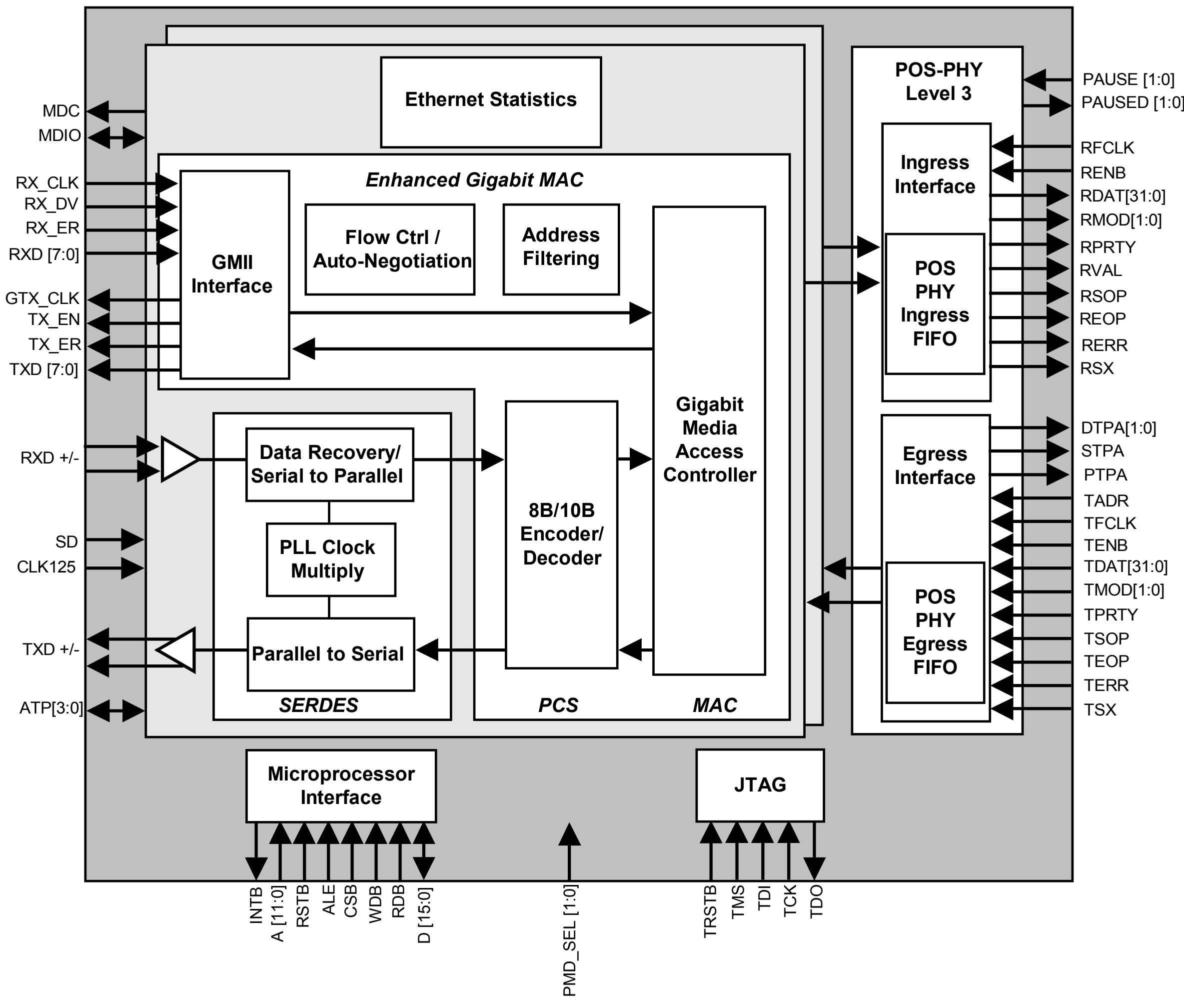
The following table defines abbreviations used throughout this document.

CSMA/CD	Carrier Sense Multiple Access with Collision Detection.
1000BASE-T	IEEE 802.3-1998 Physical Layer specification for 1000 Mb/s CSMA/CD LAN using four pairs of Category 5 balanced copper cabling.
1000BASE-SX	IEEE 802.3-1998 using short wavelength laser devices over multimode fiber
1000BASE-LX	IEEE 802.3-1998 using long wavelength laser devices over multimode and single-mode fiber.
Auto-Negotiation	The algorithm that allows two devices at either end of a link segment to negotiate common data service functions.
Base Page	The first 16-bit message exchanged during IEEE 802.3-1998 Auto-Negotiation.
Comma	The seven-bit sequence that is part of an 8B/10B code-group that is used for the purpose of code-group alignment.
Comma-	The seven-bit sequence (1100000) of an encoded data stream.
Comma+	The seven-bit sequence (0011111) of an encoded data stream.
Data Frame	Consists of Destination Address, Source Address, Length Field, logical link control (LLC) Data, PAD, and Frame Check Sequence.
DTE	Any source or destination of data connected to the local area network.
EOF	End of frame.
EOP	End of packet
EOS	Ethernet over SONET
Even Parity	The count of the number of 1's in the data word of n bits. If there are an odd number of 1s, then the parity bit will be a 1 so that including the parity bit, the number of 1s are an even number.
Frame	Same as Data Frame
Full Duplex	A mode of operation that supports simultaneous communication between a pair of stations, provided that the Physical Layer is capable of supporting simultaneous transmission and reception without interference.
GMII	Gigabit Media Independent Interface.
IPG	Inter-Packet Gap (IPG): A delay or time gap between CSMA/CD physical packets intended to provided interframe recovery time for other CSMA/CD sublayers and for the Physical Medium.
MIB	Management Information Base (MIB): A repository of information to describe the operation of specific network device.
MAC	Media Access Control (MAC): The data link sublayer that is responsible for transferring data to and from the Physical Layer.
MII	Media independent Interface (MII): A transparent signal interface at the bottom of the Reconciliation sublayer.
Next Page	General class of pages optionally transmitted by Auto-Negotiation able devices following the base page word negotiation.

Nibble	A group of four data bits. The unit of exchange on the MII.
Packet	The logical unit of data transferred across the POS-PHY Level 3 interface. This generally corresponds to the Data Frame as defined previously, although the CRC may or may not be present in the POS-PHY Level 3 egress direction.
Physical Packet	Consists of a Data Frame as defined previously, preceded by the Preamble and the Start Frame Delimiter, encoded, as appropriate, for the Physical Layer (PHY) type.
POS-PHY	SATURN compatible Packet over SONET interface specification for physical layer devices. POS-PHY level 3 defines an interface for bit rates up to and including 2.488 Gbit/s.
PL3	POS-PHY Level 3
Odd Parity	The count of the number of 1's in the data word of n bits. If there are an odd number of 1s, then the parity bit will be a 0 so that including the parity bit, the number of 1s are an odd number
SOF	Start of Frame.
SOP	Start of Packet.

5 Device block diagram

Figure 4: PM3386 S/UNI-2xGE Block Diagram.

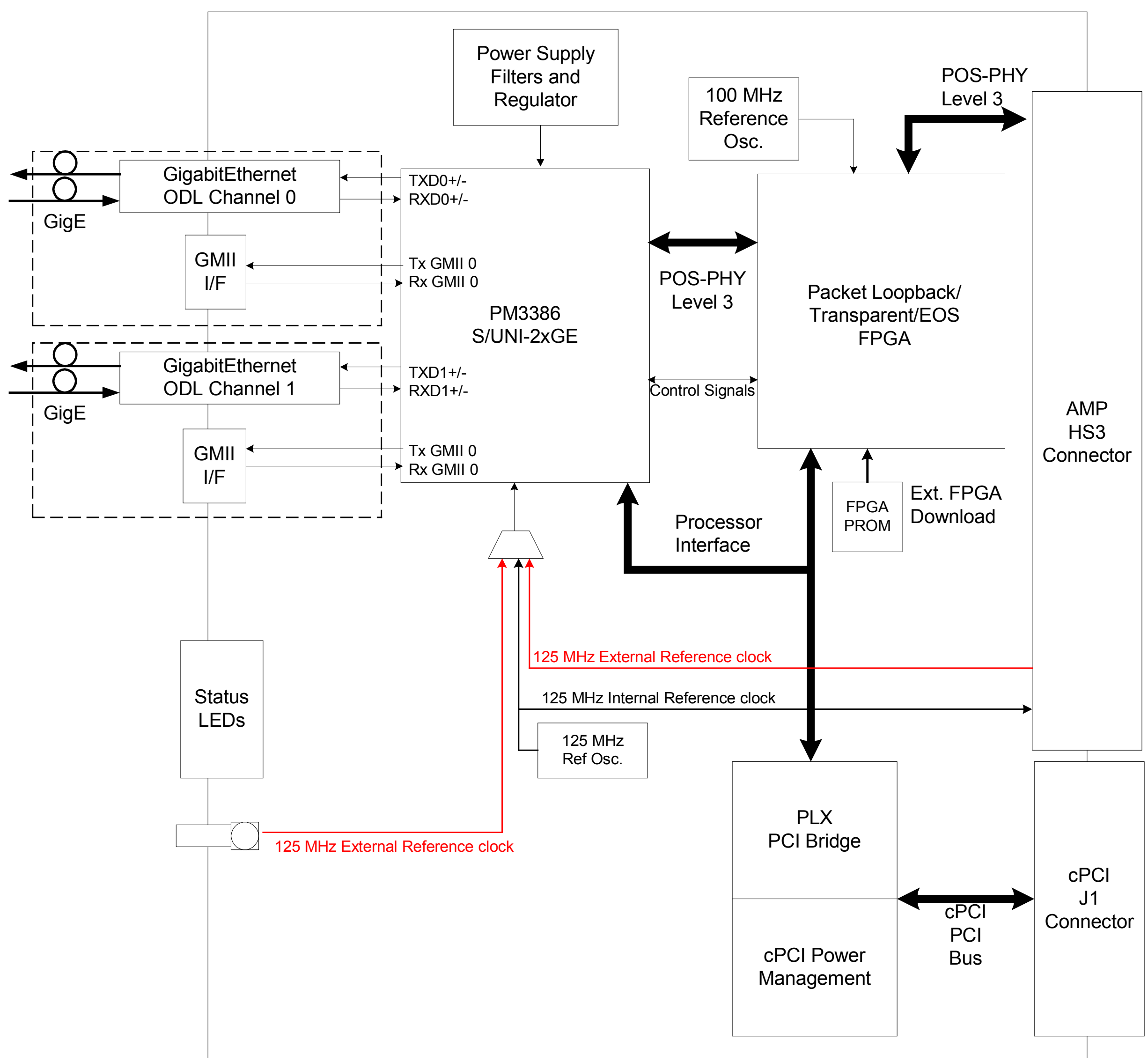


6 Reference Design Functional Description

6.1 Block Diagram

This figure depicts the major functional blocks of the Reference Design.

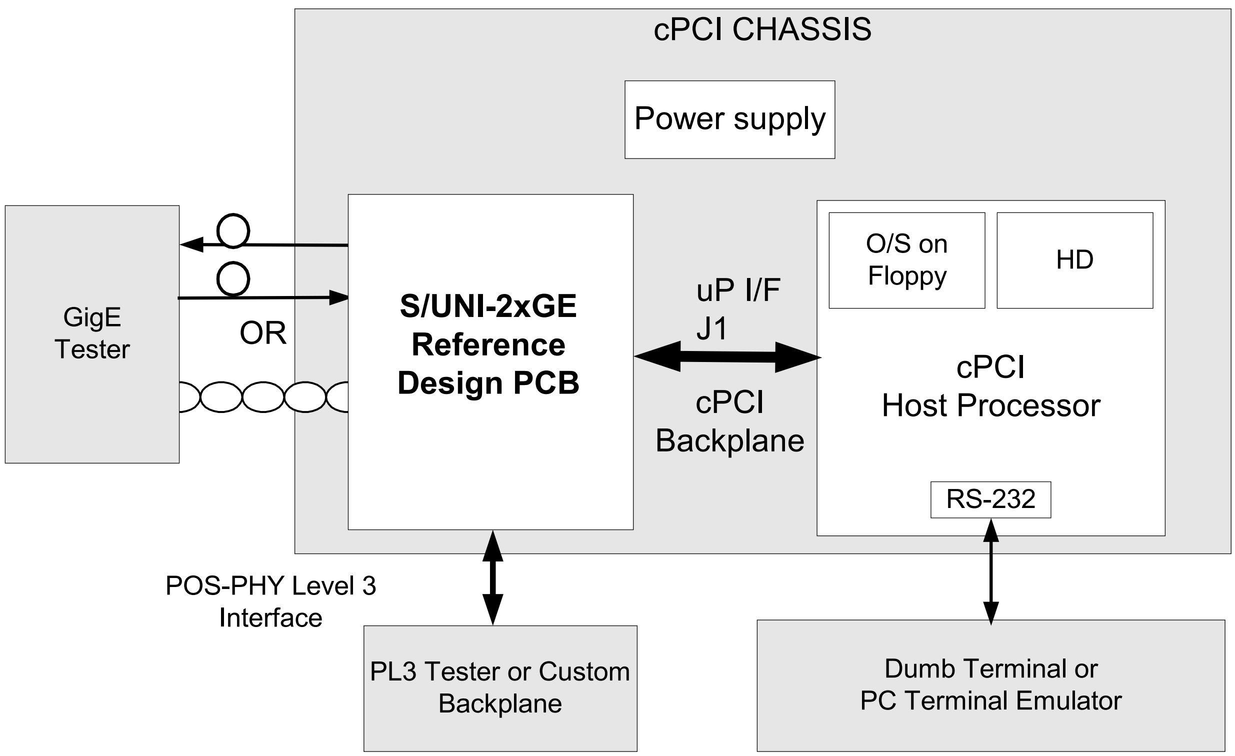
Figure 5: Reference Design Block Diagram



7 System Functional description

This Reference Design Board utilizes a 6U cPCI form factor and may only be tested within the cPCI environment. This system is composed of a cPCI chassis, the S/UNI-2xGE Reference Design PCB, single board computer with PCI support and operating system SW, and an external PC with terminal emulation software. In addition, an external Gigabit Ethernet test setup, such as a SmartBits unit is required to generate traffic and run system tests. The cPCI chassis in conjunction with a custom system side backplane provides expansion capability for a multi-service reference system implementation.

Figure 6: System Level Block Diagram



8 Implementation Description

The following descriptions refer to the S/UNI-2xGE Reference Design Schematics found in Section 11.

8.1 Root Drawing, Sheet 1

The root drawing provides a hierarchical overview of the S/UNI-2xGE reference design. Each of the major functional blocks of the design are shown, and the interconnections between the 2xGE_BLOCK, FPGA_BLOCK, SYS_INTERFACE, PCI_INTERFACE and POWER_BLOCK are drawn and labeled. On all sub-sheets of the design the interconnect signals are labeled with a "\I" suffix.

8.2 2xGE Block, Sheet 2

8.2.1 Optical Line Side Interface

The Optical Interface consists of the Gigabit Ethernet optical transceivers, power supply filtering and PECL interconnection to the serial line side interface on the S/UNI-2xGE. Two different optical transceivers are used on the board to characterize operation. One is an Infineon V23826-K305-C353 1x9 AC coupled unit, the other is an Infineon 2x5 LC unit, V23818-K305-L57. Both transceivers are internally AC coupled which eliminates the need for external terminations on the reference design, simplifying layout and improving signal integrity.

The traces for each of TXD+/- and RXD+/- (LVPECL) are controlled impedance 50 ohm. Trace lengths should be matched between pairs and the total length minimized to avoid signal degradation.

Figure 7 below provides a block diagram of the internal termination architecture used to interface the internally terminated S/UNI-2xGE PECL pins to the ODLs.

Figure 7: PM3386 to ODL Interface

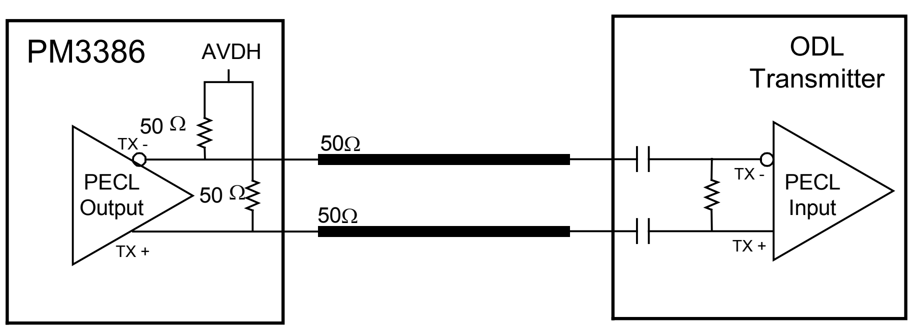
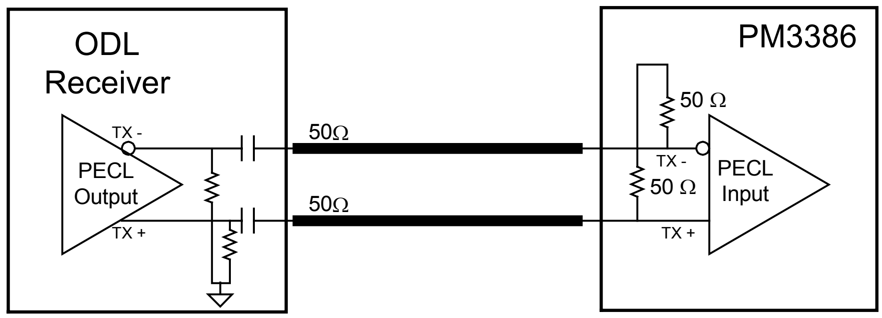


Figure 8: ODL to PM3386 Interface



8.2.2 Optical Power Supply Filtering

The power supplies are filtered as recommended by the manufacturer. The TX and RX supplies are filtered with a 1uH series inductor, and two 4.7uF Tantalum capacitors. A series resistor is inserted to help prevent the LC filter structure from ringing. A noisy analog supply may require additional filtering to achieve proper operation.

8.2.3 125MHz PHY Reference Clock Circuit

The PM3386 requires a 125 MHz Reference Clock from which to synthesize the line rate clock. In SERDES mode, the PM3386 requires only one clock source. The CLK_125 input should be supplied from a reliable clock source such as an on board oscillator or external timing circuit. The clock source must meet the following requirements, outlined in Table 1, for 802.3 compliant operation:

Table 1: CLK_125 Timing Requirements

Parameter	Min	Max	Units
Nominal CLK_125 Reference Frequency	125	125	MHz
Frequency Deviation from Nominal	-100	+100	ppm
CLK125 Reference Clock Duty Cycle	40	60	%
CLK_125 Reference Clock Deterministic Jitter (peak to peak above 200 KHz)		0.007 56	UI ps
CLK_125 Reference Clock Total Jitter (peak to peak above 200 KHz)		0.020 160	UI ps
CLK_125 Reference Clock Rise / Fall Time		1	ns

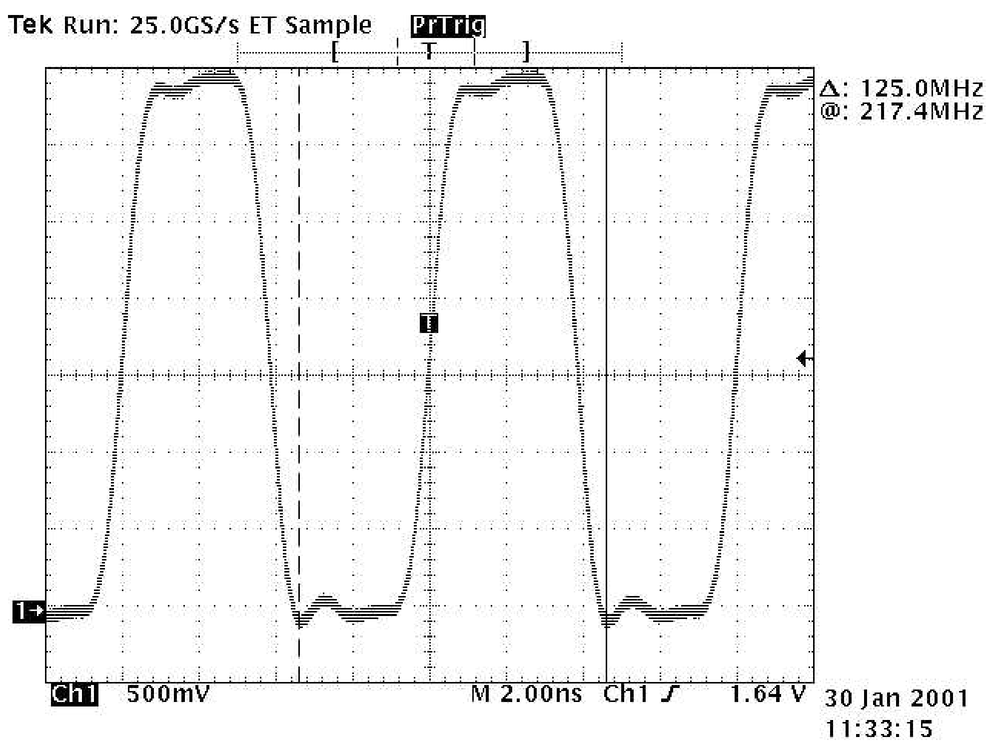
In GMII mode, the PM3386 requires 3 separate clock inputs. The RX_CLK0 and RX_CLK1 inputs must be present for the respective PHY devices. This clock source is typically generated by the Gigabit Ethernet PHY device. Additionally, the CLK_125 input must be present and meet the timing requirements above. It can be sourced from the PHY device if a valid clock is provided, otherwise the 125MHz reference clock can be sourced from a high precision on board oscillator.

Additionally, the PM3386 can operate with one channel in SERDES mode and one channel in GMII mode. In this configuration, the PM3386 shares the CLK125 input for both channels, and a valid RX_CLK must be input to the channel operating in GMII mode.

The Reference Design provides the reference clock via an Ecliptek 125MHz HCMOS crystal oscillator or from an external source via an SMB connector. Other oscillator vendors that could be used include Connor-Winfield, Raltron and MMD.

Figure 9 below shows a captured waveform of the CLK_125 signal on the S/UNI-2xGE Reference Design.

Figure 9: Ecliptek 125MHz Oscillator Waveform



8.3 2xGE Block, Sheet 3

8.3.1 GMII Interface

The two GMII interfaces on the S/UNI-2xGE are routed to a pair of high speed matched impedance connectors. GMII channel 0 is routed to J11 and GMII channel 1 is routed to J12. Each connector distributes the GMII signals associated with a single channel, and provides access to the management interface, the global reset signal, and the 125MHz system clock. The Samtec QSE-020-01-F-D connectors provide a matched impedance interface to a daughter card or other external hardware that implements a physical interface via the standard GMII port on the S/UNI-2xGE. All high speed outputs are source terminated with 33 ohm resistors.

8.4 2xGE Block, Sheet 4

8.4.1 POS-PHY Level 3 Interface

The PM3386 interfaces to higher layer devices via a 104MHz POS-PHY Level 3 interface. On the S/UNI-2xGE Reference Design, the output signals are source terminated with 33 ohm resistors. No end terminations are used. The PL3 interconnection between the S/UNI-2xGE and the FPGA is made with short 50 ohm traces.

Figure 10 below shows a captured waveform of the PM3386 output RSX signal on the S/UNI-2xGE Reference design. Figure 11 shows the 100MHz POS-PHY Level 3 RFCLK signal that drives the FPGA and PM3386 PL3 interfaces.

Figure 10: S/UNI-2xGE Reference Design RSX Signal

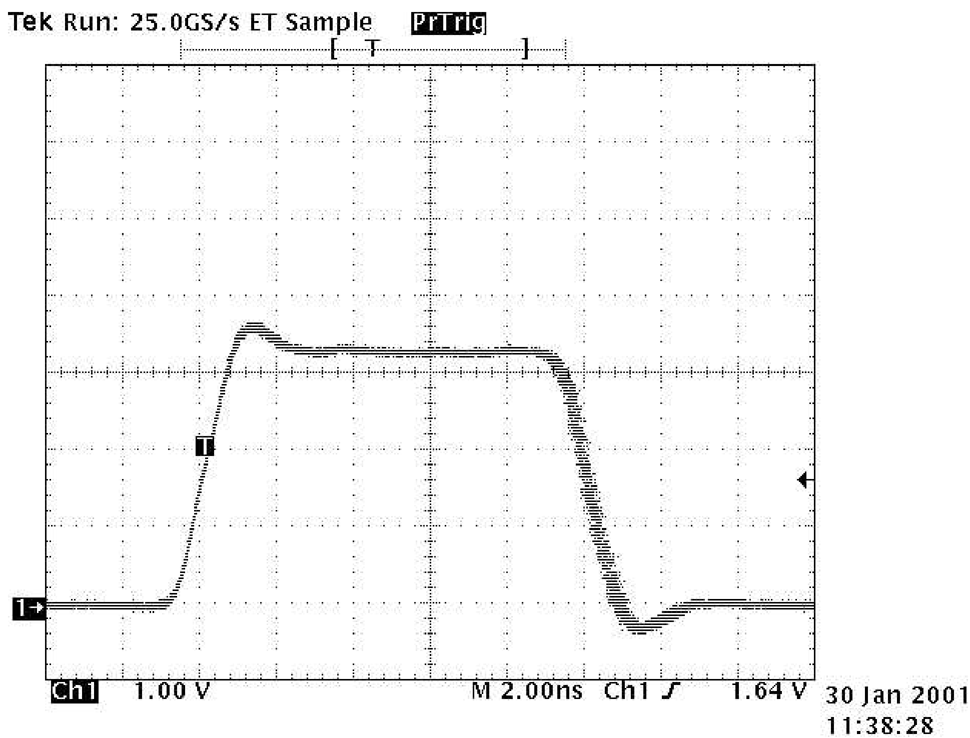
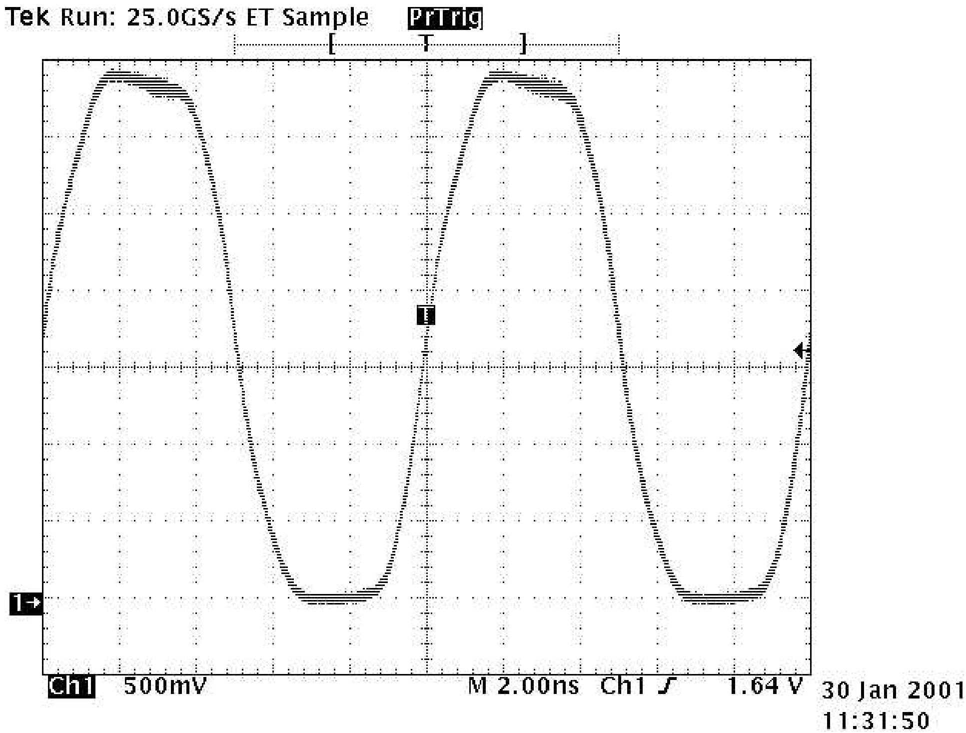


Figure 11: S/UNI-2xGE Reference Design RFCLK Signal



8.4.2 Microprocessor Interface

Sheet 4 also shows the microprocessor interface on the S/UNI-2xGE. The interface operates in non-multiplexed mode, and the chip select signal is generated by the PCI bridge device, eliminating the need for on board decode logic. A valid read or write cycle occurs when both the SUNI_CSB and WRB or RDB signal is asserted with valid address and data on the bus.

The side band flow control signals PAUSE<1..0> and PAUSED<1..0> are routed to the FPGA and can be used to initiate flow control on the S/UNI-2xGE or signal higher layer devices that the S/UNI-2xGE is receiving PAUSE frames. This functionality can be utilized effectively in EOS applications to handle near and far end backpressure across the network. See PMC-2001398 for more information regarding EOS applications.

Header J9 is provided to allow the user to select which line side interface is active on the S/UNI-2xGE. Any combination of SERDES or GMII interfacing is valid, as long as the configuration is set before power-up. By default, with no jumpers installed the S/UNI-2xGE reference design will power-up in dual SERDES mode.

8.5 2xGE Block, Sheet 5

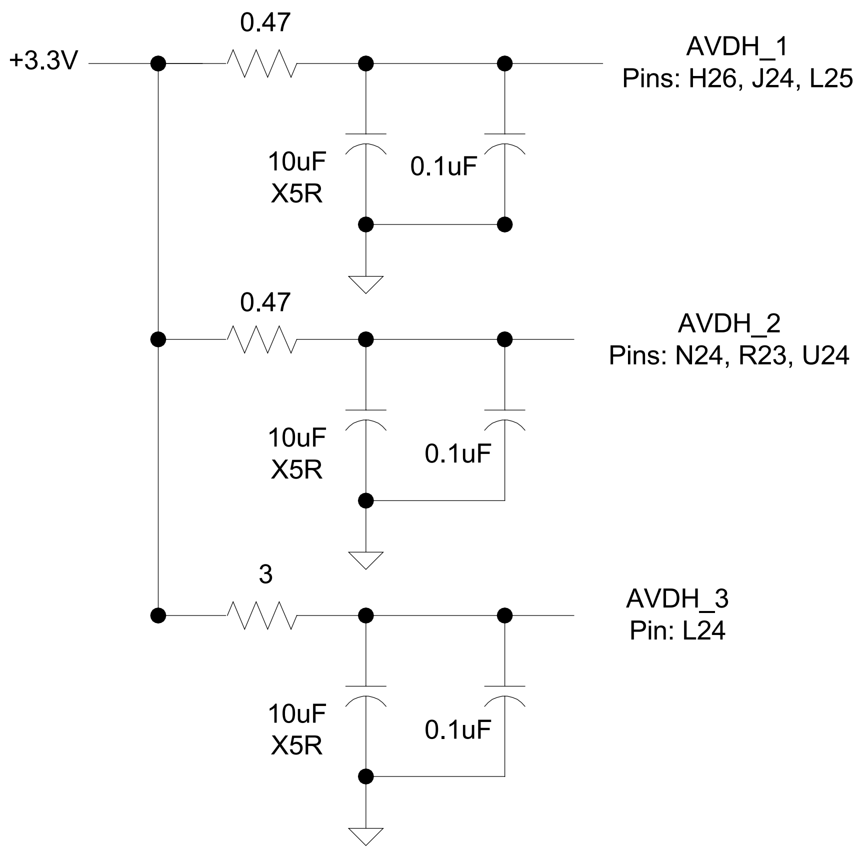
The power supply configuration for the S/UNI-2xGE is shown on Sheet 5. The PM3386 is a 0.18 micron device which requires 1.8V and 3.3V digital and analog supplies for proper operation:

- 3.3V Digital I/O – VDDO. Supplied via the CPCI interface. VDDO is well decoupled to ground. 0.1uF decoupling capacitors are placed next to the following pins: C3, V4, H4, AD3, AC9, AC19, AD24, Y23, J23, D24, B25.
- 1.8V Digital Core – VDDI. Supplied via a switching 1.8V regulator in the POWER_BLOCK. VDDI is well decoupled to ground. 0.1uF capacitors are placed next to the following pins: G1, M4, W4, AC8, AC16, AC20, V23, F23, D16, D10.
- 3.3V Quiet Analog – AVDQ. Quiet Analog power for the analog cells. The CPCI 3.3V supply is filtered and decoupled for AVDQ.
- 3.3V Quiet Digital – VDDQ. The CPCI 3.3V supply is filtered and decoupled for VDDQ.
- 3.3V Analog – AVDH. The 3.3V analog pins are filtered and decoupled to improve performance of the analog blocks. Figure 12 below outlines the pin groupings and filter architecture.
- 1.8V Analog – AVDL. The 1.8V core analog pins are filtered and decoupled to improve performance of the analog core blocks.

Until full characterization of the device can be completed all filter values should be considered preliminary.

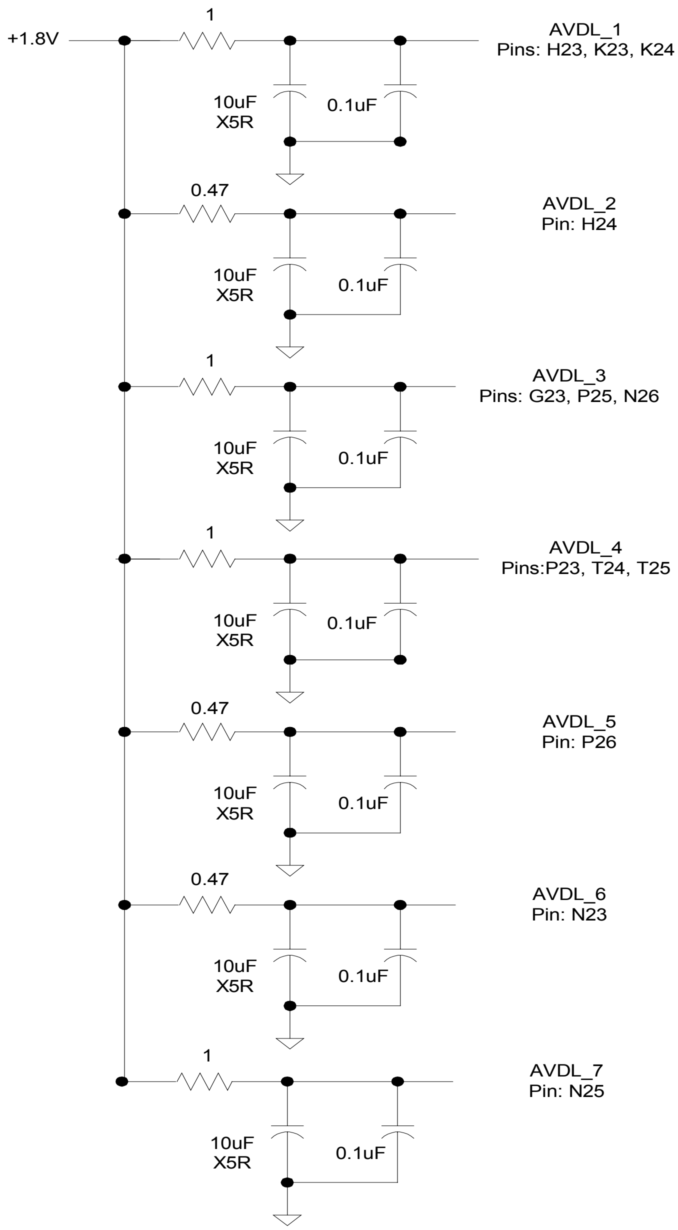
8.5.1 Power Filtering Recommendations

Figure 12: 3.3V Analog Supply Filter Architecture



The Supply Filtering for the 1.8V AVDL pins is shown below in Figure 13.

Figure 13: 1.8V Analog Filter Architecture



The 1.8V filter architecture provides optional connection to a 1.8V regulated supply that is placed near to the S/UNI-2xGE device.

All 0.1uF capacitors should be placed as close as possible to the pads on the device. Effort should be made to place the resistor and 10uF capacitor filter circuit as close as possible to the power pins as well.

Larger 10uF bulk capacitors are provided for further decoupling and should be placed near each corner of the device.

8.6 FPGA Block, Sheet 6

The FPGA supports a number of functions on the S/UNI-2xGE Reference Design. These include:

- PL3 system side loopback.
- Reset logic
- Packet processing for EOS or other applications
- LED control for status monitoring.

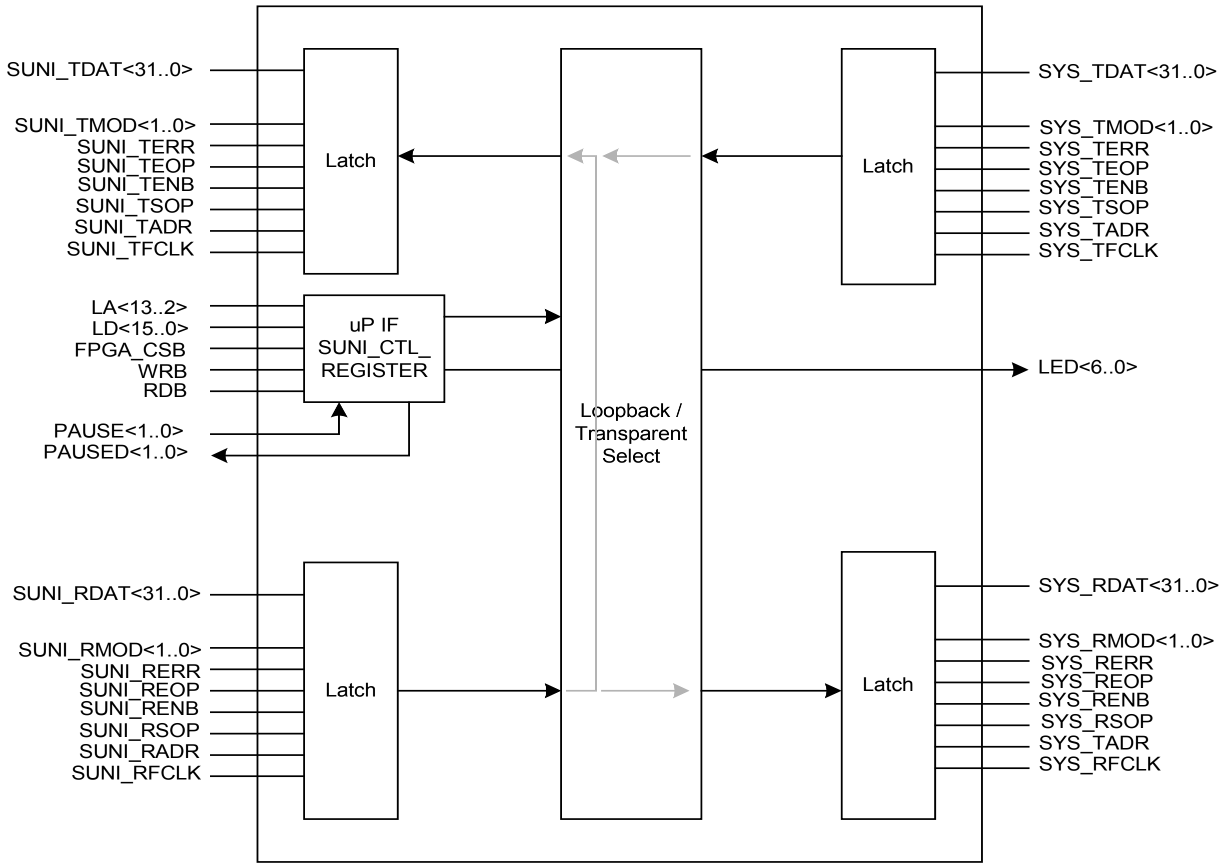
Since two full POS-PHY Level 3 interfaces are implemented on the FPGA to allow for packet processing capability and transparent interfacing to the system side, the FPGA requires a very high number of I/Os. This reference design uses a Xilinx Virtex-E FPGA. The XCV200E-6BG352 provides up to 260 I/Os in a low power 1.8V and 3.3V 352 pin BGA package. Table 2 below outlines the distribution of I/Os on the device.

Table 2: Virtex Pin Distribution

Signal Type	No. of Pins	Description
S/UNI PL3 I/F	42 TX, 42 RX, 84 Total	POS-PHY Level 3 data bus and control pins S/UNI-2xGE interface.
SYS PL3 I/F	42 TX, 42 RX, 84 Total	PL3 data bus and control pins – system side interface.
Micro I/F	34 Total	16 data lines, 11 address lines, 7 control lines.
Status/Control	35 Total	Reference clocks, PM3386 control and status, LEDs, General Purpose I/O, Reset logic.
Total	233 I/Os	Note: 13 Unused – routed to test points.

Figure 14 below shows a block diagram of the FPGA used on the S/UNI-2xGE Reference Design.

Figure 14: FPGA Block Diagram



8.6.1 Control Register Function

The S/UNI-2xGE FPGA functionality is controlled via the S/UNI Control Register. The register bit functions are outlined below.

Register 00H: S/UNI Control Register

Bit	Type	Function	Default
Bit 15	R	SUNI_PAUSED1	0
Bit 14	R	SUNI_PAUSED0	0
Bit 13	R/W	SUNI_PAUSE1_ENB	0
Bit 12	R/W	SUNI_PAUSE0_ENB	0
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	RESET	0
Bit 3	R/W	TXENA	0
Bit 2	R/W	RXENA	0
Bit 1	R/W	XPRNT_ENA	0
Bit 0	R/W	LPBK_ENA	1

Bits 0 and 1 configure the loopback/transparent functionality of the FPGA. The following combinations are valid:

- 0x01 : LPBK_ENA. The receive PL3 bus is looped back to the S/UNI-2xGE.
- 0x10 : XPRNT_ENA. The FPGA passes the RX and TX interfaces transparently to/from the backplane connector.
- 0x11 : Loop and Pass. In this mode the Receive data will be looped to the TX inputs and passed to the backplane connector.
- 0x00 : Not used. Could be used to implement packet processing functionality.

The RXENA and TXENA bits are used to enable the Receive and Transmit S/UNI side PL3 interfaces. Setting these bits to '1' enables the interface.

Bit 4 is the software reset bit. When set to a 1, the reference design global reset is asserted, resetting the S/UNI-2xGE, but not the FPGA.

Setting Bit 12 or 13 will set the PAUSE pin on the corresponding channel. The S/UNI-2xGE will output PAUSE frames to assert flow control while this bit is set high. It is synchronously sampled by the PM3386 on the rising edge of RFCLK, but can be set or cleared in the Pause Control Register at any time.

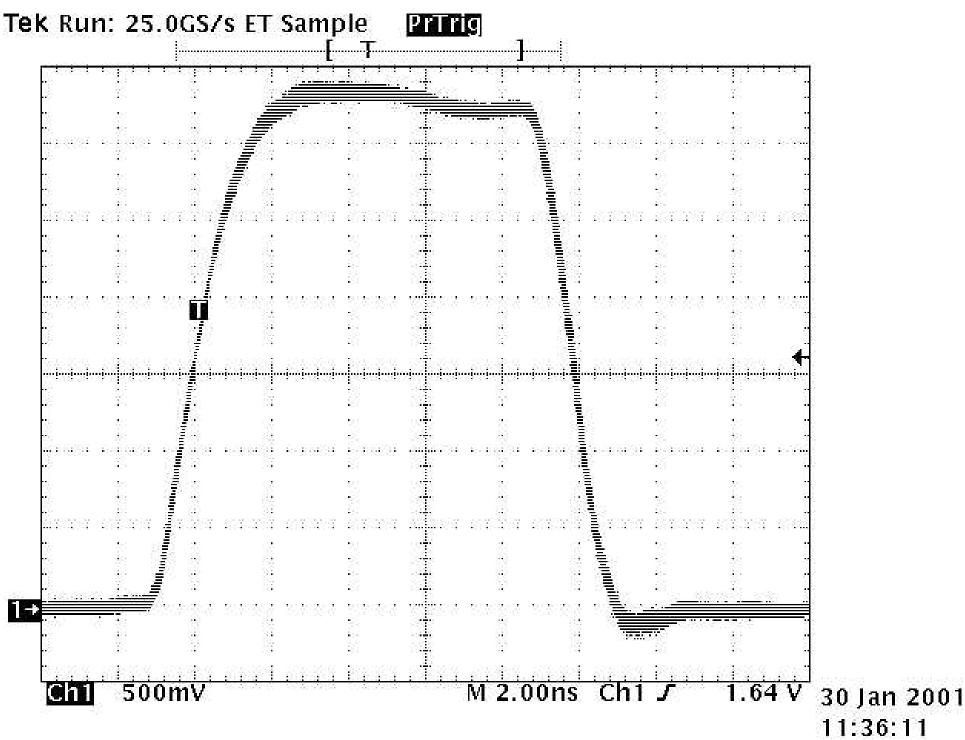
When read, bits 14 and 15 indicate the status of the PAUSED pins on the PM3386. When high, PAUSE frames are being received on the respective Gigabit Ethernet channel.

8.6.2 S/UNI-2xGE POS-PHY Level 3 Interface

Each output pin on the PL3 bus (Transmit side) is source terminated with a 33 ohm resistor. On the receive side, the signals are source terminated at the PM3386 and no end terminations are used since the trace lengths between the S/UNI-2xGE and the Virtex device are relatively short.

The TSX output from the FPGA on the S/UNI-2xGE Reference Design is shown below in Figure 15.

Figure 15: S/UNI-2xGE Reference Design TSX Signal



8.6.3 Status LEDs and Reset Circuit

Sheet 6 also shows the status LEDs and the pushbutton reset circuit for the S/UNI-2xGE Reference Design. A single LED is wired to the DONE pin and will turn on after the Virtex FPGA is successfully configured. Table 3 below outlines the function of the remaining LEDs.

Table 3: LED Display Function

Bit (D3)	Function	Bit (D3)	Function
Bit 7	Done	Bit 3	PAUSE1
Bit 6	Unused	Bit 2	PAUSE0
Bit 5	PAUSED1	Bit 1	Transparent
Bit 4	PAUSED0	Bit 0	Loopback

The pushbutton reset is provided via a MAX811 voltage monitor device that will assert a reset signal when the voltage supply is below 3.08V. The minimum reset pulse is 140ms. By logically ORing the RESET_PB signal with PWROK_1_8V, and RSTOB (from the cPCI bus) within the FPGA the system reset signal (SUNI_RSTB) is generated.

A 16x2 100mil header provides access to the microprocessor interface bus for debugging purposes.

Matched impedance MICTOR connectors that have been used in past reference designs for access to the PL3 bus are not used in this design due to the constraints they put on routing and the excessive lead times of the parts themselves. No headers are provided on the board due to space contstraints, but if probing of the PL3 bus is required the user can pass all PL3 bus signals through the FPGA and probe the signals at the backplane connector (POS Transparent Mode). A small test jig could be built to interface to a logic analyzer if desired.

8.7 FPGA Block, Sheet 7

8.7.1 System Side POS-PHY Level 3 Interface

Sheet 7 provides the remainder of the S/UNI PL3 interface signals and the system side PL3 interface. As on the S/UNI interface, all outputs are source terminated with 33 ohm resistors.

8.8 FPGA Block, Sheet 8

8.8.1 Configuration Circuit

The S/UNI-2xGE Reference Design FPGA can be configured in 3 ways:

- Via an EPROM.
- Via an XCHECKER cable.
- Via the JTAG port.

Jumpers allow the user to select between EPROM configuration or configuration via the XCHECKER cable. By default the FPGA will download configuration information from the EPROM. To configure the device via the XCHECKER cable, install all jumpers on J7 and remove the EPROM. If the EPROM is installed and the configuration is downloaded via the XCHECKER cable, the downloaded configuration will be overwritten by the contents of the EPROM.

The JTAG port is always active and takes priority over the other configuration modes, if used.

8.8.2 Power Supply Decoupling

The Virtex family of devices are capable of operating at speeds well above 200MHz. With a number of I/Os switching simultaneously at high speeds, a stable power supply is essential to achieve good performance and signal quality. The XCV200E is part of the Virtex-E family of 0.18µ devices which uses 3.3V for I/O and 1.8V for core power. On the S/UNI-2xGE reference design the 3.3V digital supply is provided by the cPCI interface and is well decoupled to ground. The 1.8V digital supply is provided via the switching regulator in the POWER_BLOCK and is also well decoupled to ground. Based on Xilinx recommendations, eight 10uF bulk capacitors are added to further decouple the device, and placed near each I/O bank on the Virtex device. Finally, four 0.47uF capacitors are placed at the corners.

8.9 FPGA Block, Sheet 9

8.9.1 100 MHz PL3 Clock Distribution

A 100 MHz oscillator, 100 ppm, is used for the POS-PHY Level 3 interface. No series termination resistor is used between the oscillator output and the input to due to the extremely short trace length.

A clock distribution driver is used to provide low skew clocks to the PM3386, the FPGA, and to the external HS3 connector. The PI49FCT3807D (the 110MHz rated FCT3807C would suffice) was selected as the clock driver as it provides up to 10 outputs with a maximum skew of 350 ps and can operate from a +3.3 Volt supply. The +3.3 Volt supply is bypassed with two capacitors to help reduce power supply glitches when all 10 outputs switch simultaneously at 100 MHz.

Each output from the FCT3807 is source terminated through a 33 ohm resistor in order to match the impedance of the 50 Ω traces distributing the clock signal. Correct termination of the clock signals is especially important to ensure monotonic, glitch-free, clocking of the S/UNI device, the FPGA, and the external system.

8.9.2 100 MHz Clock Source Switching

The clock architecture on the S/UNI-2xGE Reference Design has been developed to operate as either a clock master or a clock slave when connected to an external system. The 100MHz PL3 clock is distributed to the FPGA and the S/UNI device via solder bridges and to the system side backplane. By configuring the solder bridges to source the clock from the on board oscillator or from the FPGA, the board can operate as a clock master or clock slave.

If the external system is the clock master, The FPGA routes the TFCLK and RFCLK signals from the backplane to the S/UNI-2xGE, taking advantage of the built in Delay Lock Loop architecture to improve clock performance.

8.10 CPCI Interface Block, Sheet 10

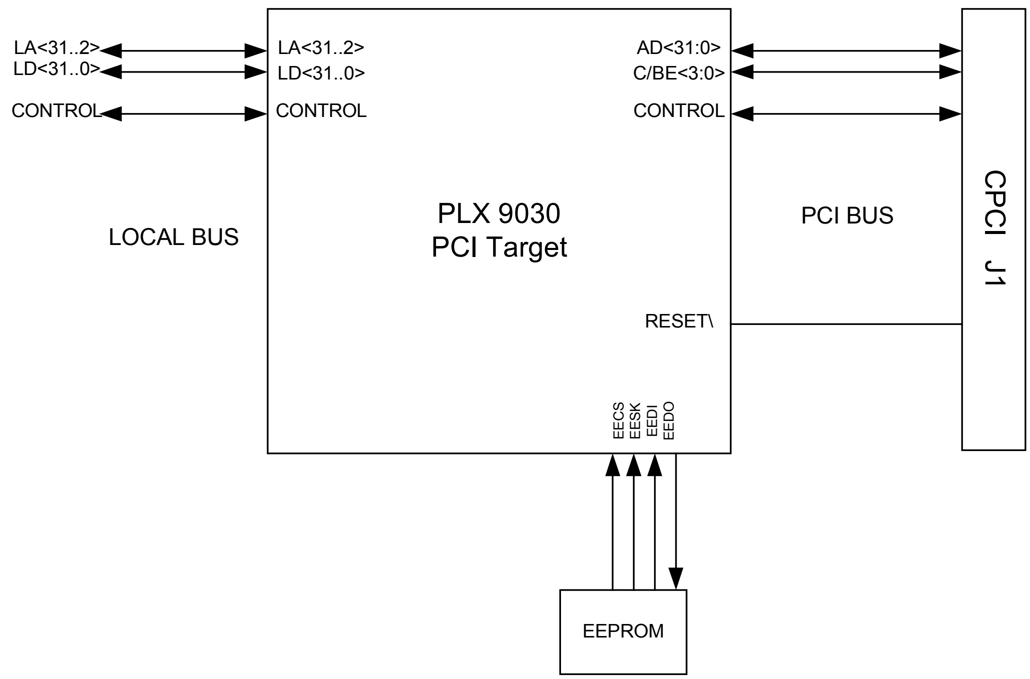
8.10.1 CPCI Interface Controller

The cPCI Host Processor Interface is based on the PCI 9030 device. This device is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Target Interface Device, that provides flexible local bus configurations and Hot Swap capability.

The PCI 9030 operates with a 32-bit non-multiplexed bus on the local bus side. It provides up to four configurable chip selects and up to nine user configurable general purpose I/O pins eliminating the need for external glue logic to interface to devices on the local bus. The PCI9030 provides full Hot Swap capability and has the required 1V cPCI bus precharge voltage function built in, eliminating the need for external pull-up resistors and voltage regulator.

A serial EEPROM is used for device configuration after a reset. This design supports the Fairchild Semiconductor 93CS66LEN (4K) or 93CS56LEN (2K) serial EEPROM.

Figure 16: Host Processor cPCI Interface



8.11 CPCI Interface Block, Sheet 11

8.11.1 CPCI J1 Connector

An AMP Z-PACK connector is used to provide a cPCI compliant J1 interface. For details regarding this interface, please refer to the current Compact PCI specifications.

8.11.2 ESD Strip

An ESD strip is integrated into the PCB along the front edge

8.12 cPCI Power_Block, Sheet 12

Note: A discrepancy exists between the power-up sequencing used in this reference design and the power-up sequencing described in the S/UNI-2xGE Datasheet (PMC-1991129) and its related errata (PMC-2010140). Please refer to the S/UNI-2xGE Datasheet (PMC-1991129) and its related errata (PMC-2010140) for the proper power-up sequencing recommendations.

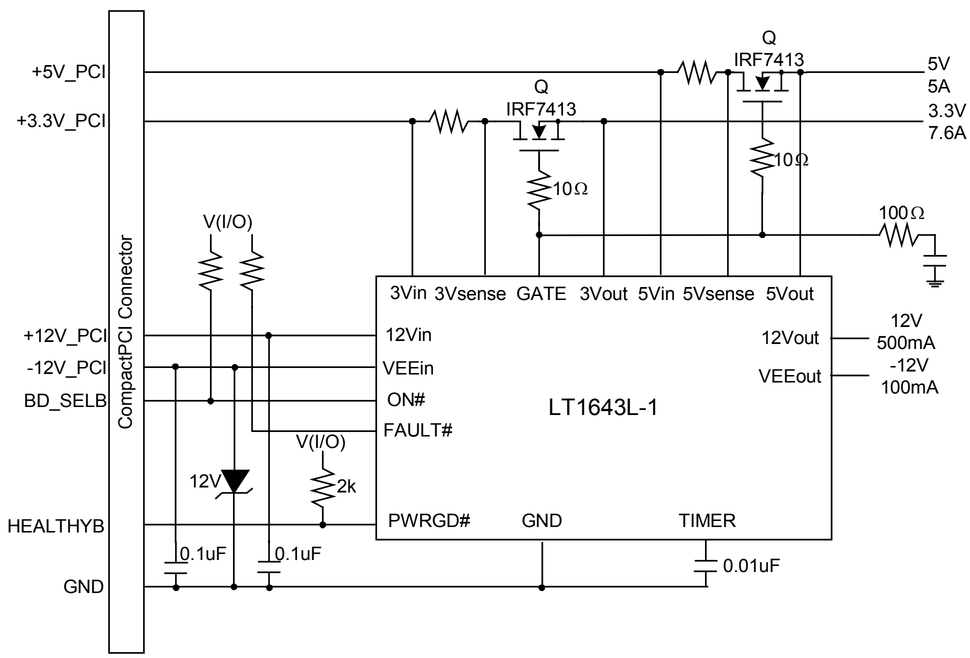
8.12.1 Hot Swap Controller System Block

The Hot Swap Controller is used to allow a board to be safely inserted or removed from a live cPCI slot. The Hot Swap controller on the Power Supply Board System Block is implemented using the Linear Technology LTC1643L-1 The Hot Swap controller allows the supply voltages to be ramped up at a programmable rate, detects over-current and over-voltage conditions, and shuts down power to the board until those conditions are rectified. The LTC1643L-1 PWRGD# logic ignores the +/-12V rails which is applicable in systems that do not implement or have poor 12V supplies.

The +12V and –12V supplies are controlled with on-chip switches, while external N-channel MOSFETS are used to control the 3.3V and 5V supplies.

A DC/DC converter is used to generate 1.8V from the 5V rail.

Figure 17: cPCI Hot Swap Controller



8.13 System Interface, Sheet 13

8.13.1 POS-PHY Level 3 Interface

The S/UNI-2xGE POS-PHY L3 interface is connected to the FPGA and to the drop side HS3 connector.

The HS3 connector uses a PMC-Sierra, Inc. proprietary pin out for the PL3 bus as shown in the following two tables

Table 4: PL3 High Speed RX Interface, J11

Pin Name	Type	Pin No.	Function
RDAT[0]	Output	B4	Receive Packet Data Bus
RDAT[1]		A4	For POS-PHY Level 3 this bus carries Packets that are read from the selected receive FIFO.
RDAT[2]		E5	
RDAT[3]		D5	
RDAT[4]		C5	
RDAT[5]		B5	
RDAT[6]		A5	
RDAT[7]		E6	
RDAT[8]		D6	
RDAT[9]		C6	
RDAT[10]		B6	
RDAT[11]		A6	
RDAT[12]		E7	
RDAT[13]		D7	
RDAT[14]		C7	
RDAT[15]		B7	
RDAT[16]		A7	
RDAT[17]		E8	
RDAT[18]		D8	
RDAT[19]		C8	
RDAT[20]		B8	
RDAT[21]		A8	
RDAT[22]		E9	
RDAT[23]		D9	
RDAT[24]		C9	
RDAT[25]		B9	
RDAT[26]		A9	
RDAT[27]		E10	
RDAT[28]		D10	
RDAT[29]		C10	
RDAT[30]		B10	
RDAT[31]		A10	
RPRTY	Output	A3	Receive Bus Parity The receive parity signal indicates the parity of the RDAT bus.
RENB	Input	E1	Receive Write Enable The RENB signal is an active low input which is used to initiate reads from the receive FIFO.

Pin Name	Type	Pin No.	Function
RVAL	Output	B3	Receive Data Valid RVAL indicates signals RDAT, RSOP, REOP, RMOD, RPRTY and RERR are valid. This signal is not used in UTOPIA mode.
RSOP	Output	D4	Receive Start of Packet This signal marks the start of packet on the RDAT bus.
RERR	Output	C4	Receive Error This signal indicates that the current packet has been aborted.
REOP	Output	E4	Receive End of Packet This signal marks the end of packet on the RDAT bus.
RMOD[1] RMOD[0]	Output	D3 C3	Receive Word Modulo Indicates number of bytes in the last RDAT bus transaction of a packet.
RSX	Output	E3	Receive Start of Transfer RSX indicates when the in-band PHY port address is present on RDAT bus.
RFCLK	Input	F1	104 MHz Receive Bus Slave Clock Input Provided to the PM3386 RFCLK input via CMOS switches during RX Slave mode operation.
RSYSCLK	Output	C1	104 MHz Receive Bus Master Clock Output Provided to the external system and timed to coincide with RFCLK signal to PM3386 during RX Master mode operation.
GND	Power	AB1 -AB10, CD1 -CD10, EF1 - EF10	Ground

Table 5: PL3 High Speed TX Interface, J10

Pin Name	Type	Pin No.	Function
TDAT[0]	Input	C4	Transmit Packet Data Bus This data bus carries the POS packet octets that are written to the selected transmit FIFO.
TDAT[1]		B4	
TDAT[2]		A4	
TDAT[3]		E5	
TDAT[4]		D5	
TDAT[5]		C5	
TDAT[6]		B5	
TDAT[7]		A5	
TDAT[8]		E6	
TDAT[9]		D6	
TDAT[10]		C6	
TDAT[11]		B6	
TDAT[12]		A6	
TDAT[13]		E7	
TDAT[14]		D7	
TDAT[15]		C7	
TDAT[16]		B7	
TDAT[17]		A7	
TDAT[18]		E8	
TDAT[19]		D8	
TDAT[20]		C8	
TDAT[21]		B8	
TDAT[22]		A8	
TDAT[23]		E9	
TDAT[24]		D9	
TDAT[25]		C9	
TDAT[26]		B9	
TDAT[27]		A9	
TDAT[28]		E10	
TDAT[29]		D10	
TDAT[30]		B10	
TDAT[31]		A10	
TPRTY	Input	D4	Transmit Bus Parity. The transmit parity signal indicates the parity of the TDAT bus.
TENB	Input	C2	Transmit Write Enable. The TENB signal is an active low input which is used to initiate writes to the transmit FIFO

Pin Name	Type	Pin No.	Function
TSOP	Input	B3	Transmit Start of Packet This signal indicates the first byte in a packet.
TERR	Input	E4	Transmit Error This signal indicates the current packet must be aborted.
TEOP	Input	C3	Transmit End of Packet This signal marks the end of a packet on the TDAT bus.
TMOD[1] TMOD[0]	Input	B2 A2	Transmit Word Modulo This signal indicates the size of the current word.
TADR	Input	E1	Transmit PHY Address Allows selection of either PHY channel on the S/UNI-2xGE for polling.
TSX	Input	A3	Transmit Start of Transfer TSX indicates when the in-band PHY port address is present on TDAT bus.
TFCLK	Input	F10	104 MHz Transmit Bus Slave Clock Input Provided to the PM3386 TFCLK input via switches during TX Slave mode operation.
TSYSCLK	Output	C10	104 MHz Transmit Bus Master Clock Output Provided to the external system and timed to coincide with TFCLK signal to PM3386 during TX Master mode operation.
GND	Power	AB1 -AB10, CD1 -CD10, EF1 - EF10	Ground

9 Physical Design considerations

9.1 PCB Layout Issues

Because of the high speed 1.25GHz PECL differential drivers, and fast edged signals on the PL3 bus, the reference design PCB requires careful layout. Typically the drivers have rise/fall times below 1ns. High speed traces should be as short as possible, controlled impedance transmission lines used where indicated and standard terminations must be incorporated to prevent signal reflections.

Standard FR-4 PCB material can be used for this application with as many layers as required to derive the final board thickness, achieve enough layers for signal routing and attain the required trace impedance. Please refer to the first page of the artwork for more details on the reference design PCB.

Table 6: Reference Design PCB Stack Up (Preliminary)

Layer	Location
TOP	Top Signal Layer, Component Side
GND1_PLANE	Power Plane
VCC1_PLANE	Ground
SIG1	Signal Layer
SIG2	Signal Layer
VCC2_PLANE	Power Plane
GND2_PLANE	Ground
SIG3	Signal Layer
SIG4	Signal Layer
VCC3_PLANE	Power Plane
GND3_PLANE	Ground
BOTTOM	Bottom Signal Layer, Solder Side

Although only one ground plane is required, additional planes can be used to attain the desired board thickness and correct trace impedance. A ground layer or a power plane can be used to achieve the desired signal transmission line trace impedance assuming there is adequate coupling between them.

All traces on the board are 50 characteristic impedance, except the cPCI bus traces which are required to be 65 ohms.

9.2 Thermal Issues

As stated in the product datasheet, the power dissipation is estimated at 2W. In order to achieve long term reliability, the device junction temperature (Tj) must be kept below 105°C.

The design of the chip cooling system will be influenced by a number of factors including:

- ambient temperature in which the device will operate
- proximity of other devices that may impede airflow
- orientation of device on board
- air movement through the design

The table below outlines basic thermal reliability information for the PM3386.

Table 7: PM3386 Reliability Information

RESULTS

Confidence Level		60%	90%	60%	90%
Package Type		352 UBGA	352 UBGA	352 UBGA	352 UBGA
Ambient Temperature	(deg C)	40	40	60	60
Theta JA at Operating Ambient	(deg C/Watt)	19	19	19	19
Base Failure Rate at TJ=55 deg C	(FITS)	24	35	24	35
Junction Temperature	(deg C)	111	111	131	131
Failure Rate at Ambient Temperature	(FITS)	892	1280	2547	3653
MTBF at Ambient Temperature	(years)	128	89	45	31

Notes

1. Theta JA is for a dense board device in natural convection.
2. Calculated FIT Rate (Failure rate at ambient temperature)
3. FIT is defined as failure rate per billion hours
4. See PMC-920615 for key to Branding Suffixes
5. Refer to PMC-930812 for other details

9.2.1 Sample calculations

In order to maintain a junction temperature Tj below 105°C with only natural convection cooling in a dense board implementation, the ambient air temperature surrounding the device could not exceed:

Max temperature = 105°C – (θ_{JA} x Power Dissipated)

= 105°C – (19°C/W x 2 Watts)

= 67°C

In many cases where the ambient temperature is expected to be higher or on boards that are more densely populated, additional heatsinking is required.

The reference design has been designed to operate in an environment with limited airflow and potentially high ambient temperatures. As a result, a heatsink and external airflow (via a fan) should be used to compensate.

The AAVID 335514 heatsink provides a thermal resistance between the case temperature and the ambient air temperature (θ_{SA}) of 7.9°C/W at 200 LFM. Based on a thermal resistance between the device junction and the device case (θ_{JC}) of 1°C/W, and a thermal resistance between the device case and the heatsink (θ_{CS}) of ~0.1°C/W, this heatsink will allow operation at ambient temperatures of up to:

Max temperature = 105°C – ((θ_{JC} + θ_{CS} + θ_{SA}) x Power Dissipated)

= 105°C – ((1+0.1+7.9)°C/W x 2 Watts)

= 87°C

10 Electrical Design Considerations

10.1 PECL Interface Issues

Because of the transmission stub created by the ODL internal PCB trace and through-hole solder mounting pins, care should be taken when artworking traces between the optics and the S/UNI-2xGE. No vias should be present on the point to point traces except where required for terminating components. Any vias present along the traces will degrade jitter performance. These differential traces should be of equal length and have as few corners as possible. To prevent transmission stubs, terminating components (resistors) should be placed after the IC pin(s) and on the solder side (bottom) of the PCB.

10.2 Optical Transceiver Terminations

The PECL transmit and receive interface on the S/UNI-2xGE requires AC coupling to operate correctly. When interfacing the PM3386 to ODLs that to not have integrated terminations, Figure 18 and Figure 19 below outline the recommended interface terminations.

Figure 18: PM3386 Transmit SERDES to Optical Transmitter

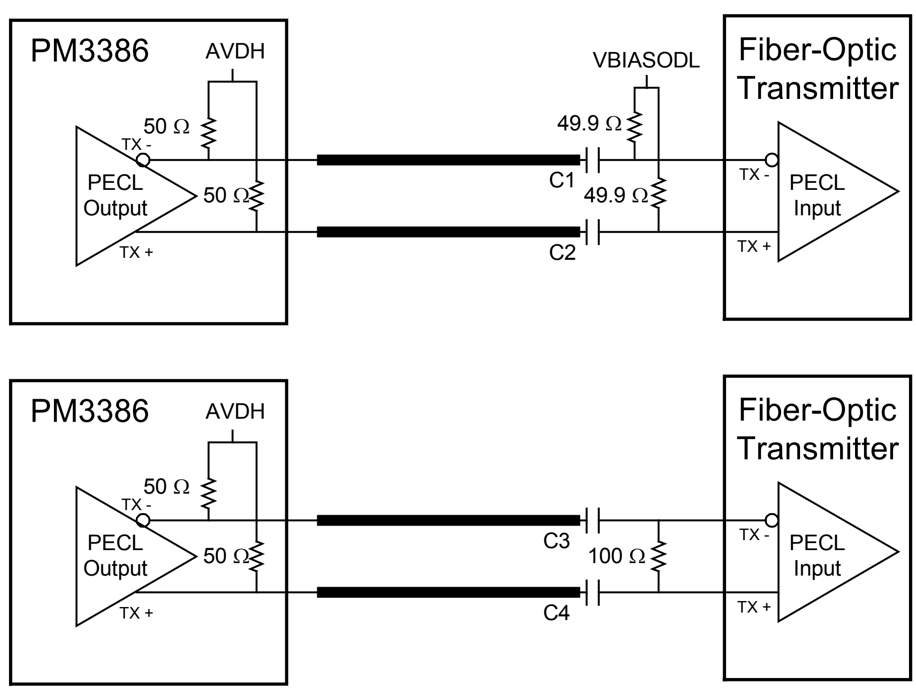


Figure 19 represents a typical application showing the transmit datapath termination. Note that the characteristic impedance for the termination is 50 Ω single ended or 100 Ω differential. Values for C1, C2, C3, and C4 are recommended to be 100nF. Please note that the many transceivers on the market may contain the needed termination resistors and capacitors. In addition the TX_EN0 or TX_EN1 signal may be used as the transmit enable while in SERDES mode.

Figure 19: Optical Receiver to PM3386 SERDES

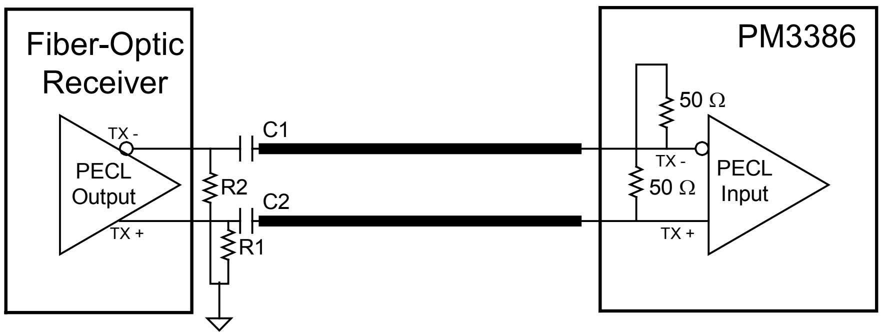


Figure 19 represents a typical application showing the receive datapath termination. Please note the internal 50 Ω single ended termination within the PM3386 receive PECL cells. Follow the manufactures recommended requirements when interfacing the Fiber-Optic Receiver to the PM3386. Differing Fiber-Optic Receivers require differing values for the R1 and R2 termination resistors. RXSD0 and RXSD1 may be used as the input signal detect for transceivers that support this feature.

10.3 Power Up/Down Considerations

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions it is possible to blow these ESD protection devices or trigger latch up. For more information on the required power up sequence, refer to the S/UNI-2xGE data sheet. The following features on the S/UNI-2xGE reference design ensure power up and power down occurs properly.

- AVDQ
  A 10 ohm resistor is placed in series between the 3.3 Volt supply and the AVDQ pins. The 10ohm resistor and a 10μF capacitor.

- VDDO, AVDQ, and AVDH
  VDDO, AVDQ, and the AVDH pins are supplied from the same 3.3V power plane. This keeps the voltage difference between the AVDH pins, VDDO and AVDQ pins small preventing current flow from AVD pins to the VDDO, and AVDQ pins.

10.4 Grounding

A single ground plane is recommended with no power or ground cuts in the plane. This one ground plane is shared among digital and analog signals. One ground plane simplifies design and layout. More than one ground layer can be used but all ground connections (vias) should be made to all layers to make it appear as one ground plane. Characteristic impedances can be realized by providing the current return path either through a ground or power plane.

Since the ODLs are optically isolated, there is no requirement for extensive high-voltage and/or high energy protection as in other metallic physical mediums such as T1/E1.

10.5 System Side Transmission Line Terminations

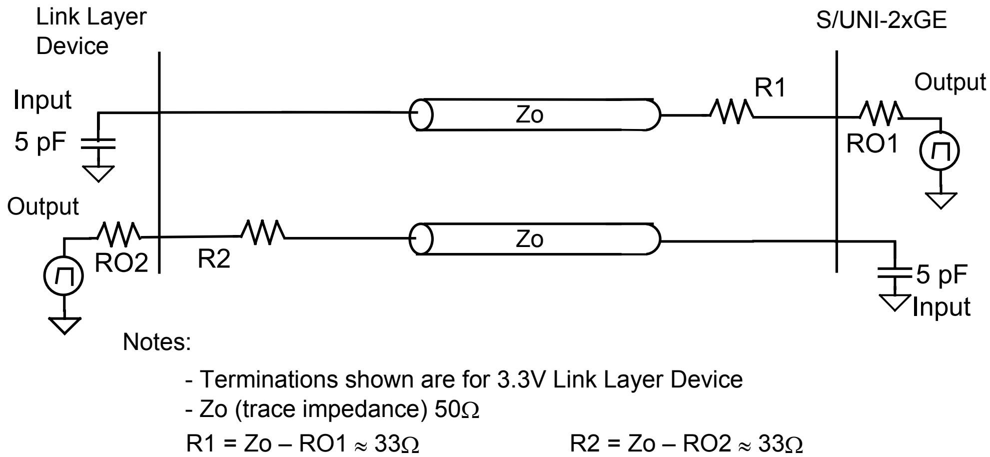
The S/UNI-2xGE is capable of system side interface speeds up to 104 MHz. Because of the high frequency content of the system side signals, terminations may be required to ensure reliable data transmission across the interface.

A “series source terminating resistor” may be required in a system where the PL3 Bus drivers have a fast rise/fall time and the distance between the 2xGE and the link layer device is substantial. If we consider that these CMOS PL3 drivers have typical 1ns edges then traces longer than 0.89in/2.26cm should be terminated.

On the S/UNI-2xGE Reference Design source terminations are implemented on the PL3 bus and work to eliminate signal reflections at the output pins. As stated above, if the trace length is sufficiently short additional terminations are not necessary.

Since the drivers are CMOS and have limited current drive/source capabilities, parallel far end terminations can’t be used. For point to point transmission, series source termination is a good option. The figure below illustrates the relative positioning and values of series source termination resistors. Resistor values may vary depending on Zo transmission line impedance and the output impedance of the I/O driver.

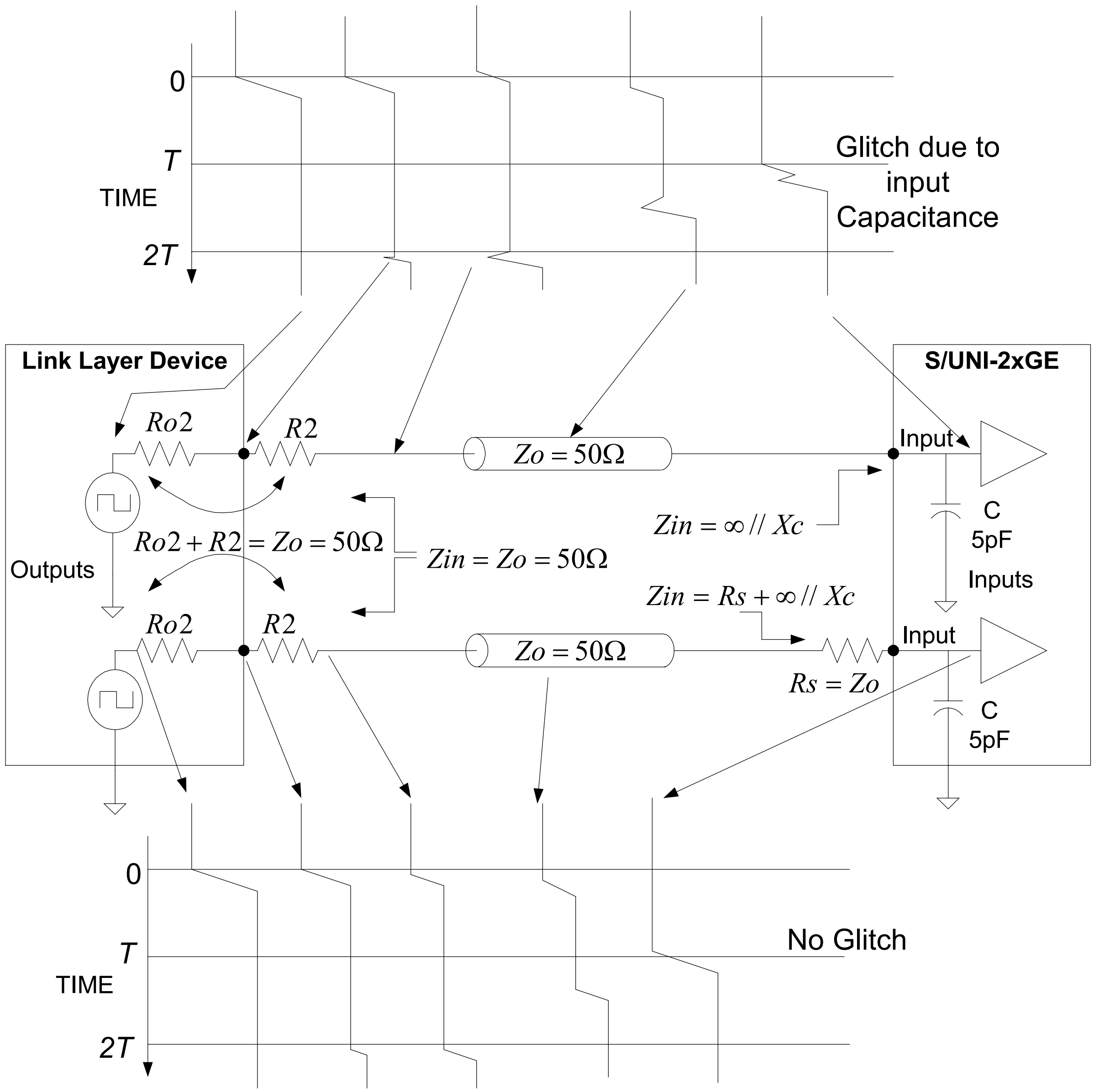
Figure 20: System Interface Terminations



Because of the relative uncertainty of the output impedance (RO1 and RO2), it's best to have Zo as large as possible so that the output impedance is as small as possible relative to Zo. However, a large Zo means a narrow, difficult to manufacture PCB trace. A small Zo would require wide traces and would take up a lot of PCB real-estate. On PCBs with BGA and other high density components a narrow trace is required to be able to route between chip pins/balls.

A "series source termination" scheme assumes that the far end has infinite impedance. However, as shown in Figure 21, all CMOS type infinite impedance inputs have finite capacitive inputs of about 5pF. Initially when the rising or falling edge hits the input pin, the far end looks like a short circuit until the capacitor is charged/discharged at which point the input looks like an infinite impedance. This causes a small glitch reflected back which may cause a problem. A simple way to solve this is to put another series resistor at the input to the far-end pin, equal to the impedance of the transmission line. On the S/UNI-2xGE Reference Design Post-Layout simulations have shown that end terminations are not necessary and do not improve performance.

Figure 21: Series Source Termination



T = time it takes for edge to reach far end of transmission trace.

each trace shows voltage vs. time at this position

11 Schematics Revision 1

REVISIONS				
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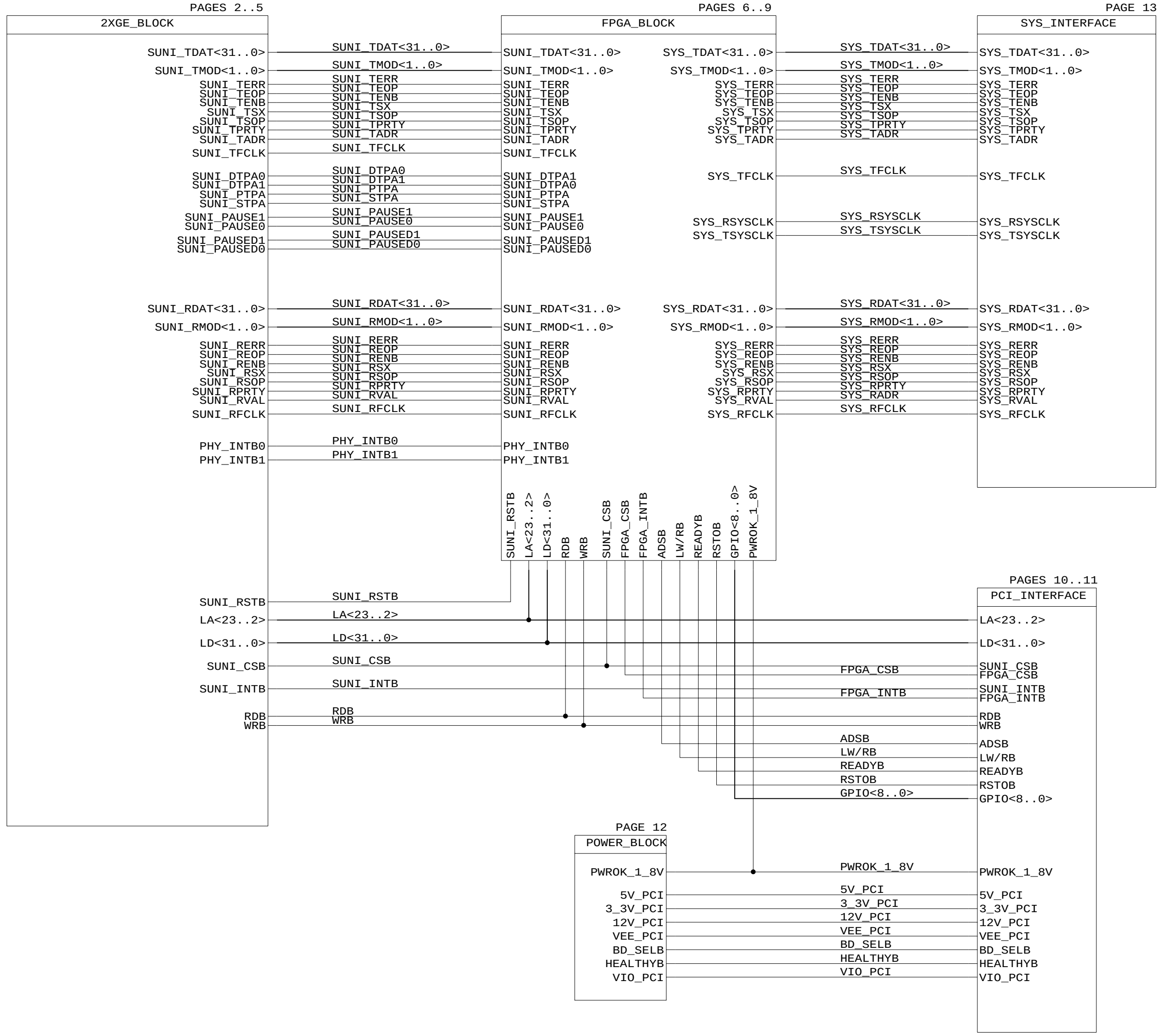

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ENGINEER: BDV	PAGE:1 OF 13

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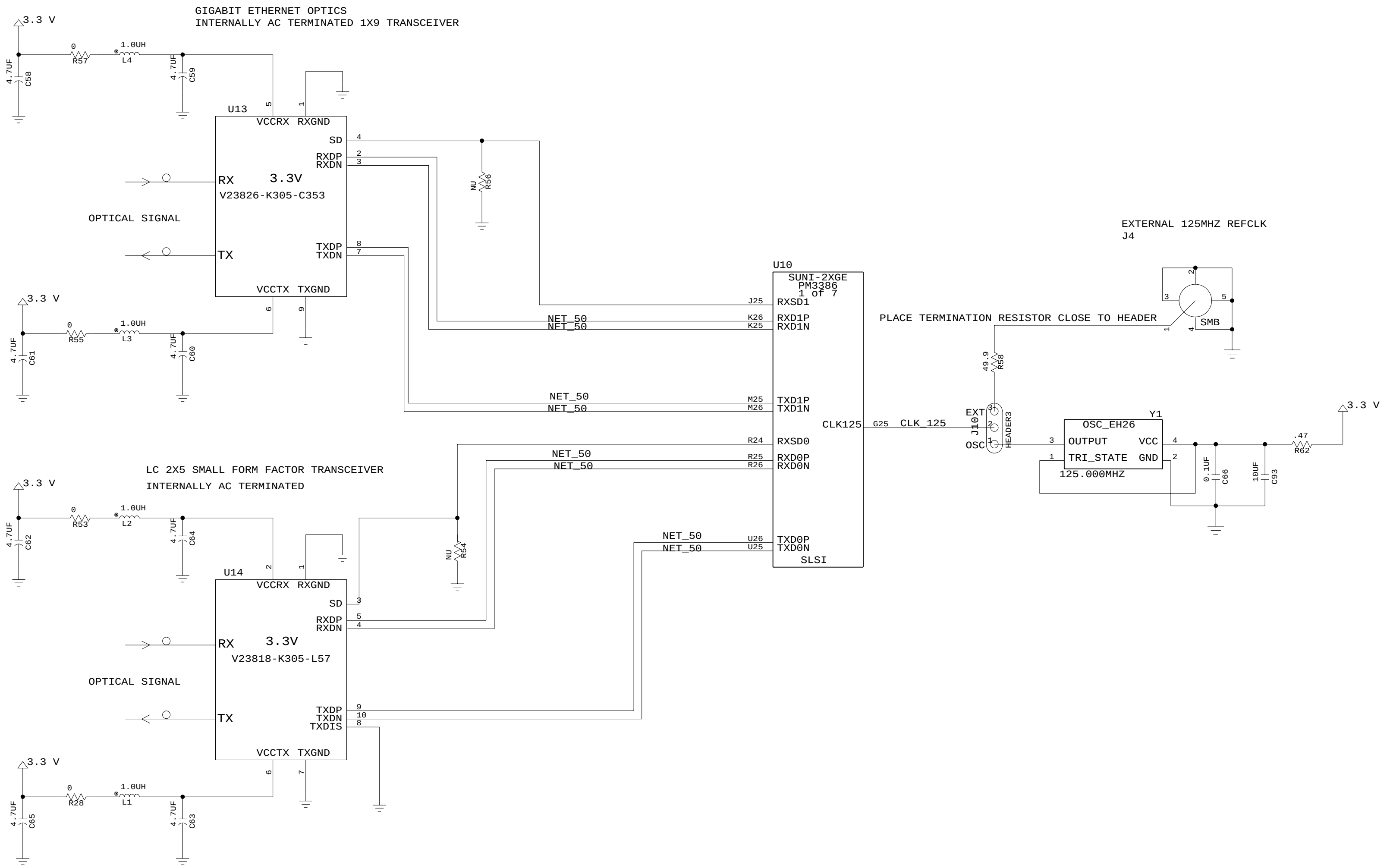

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TITLE: S/UNI-2XGE REFERENCE DESIGN OPTICAL LINE SIDE INTERFACE	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:2 OF 13

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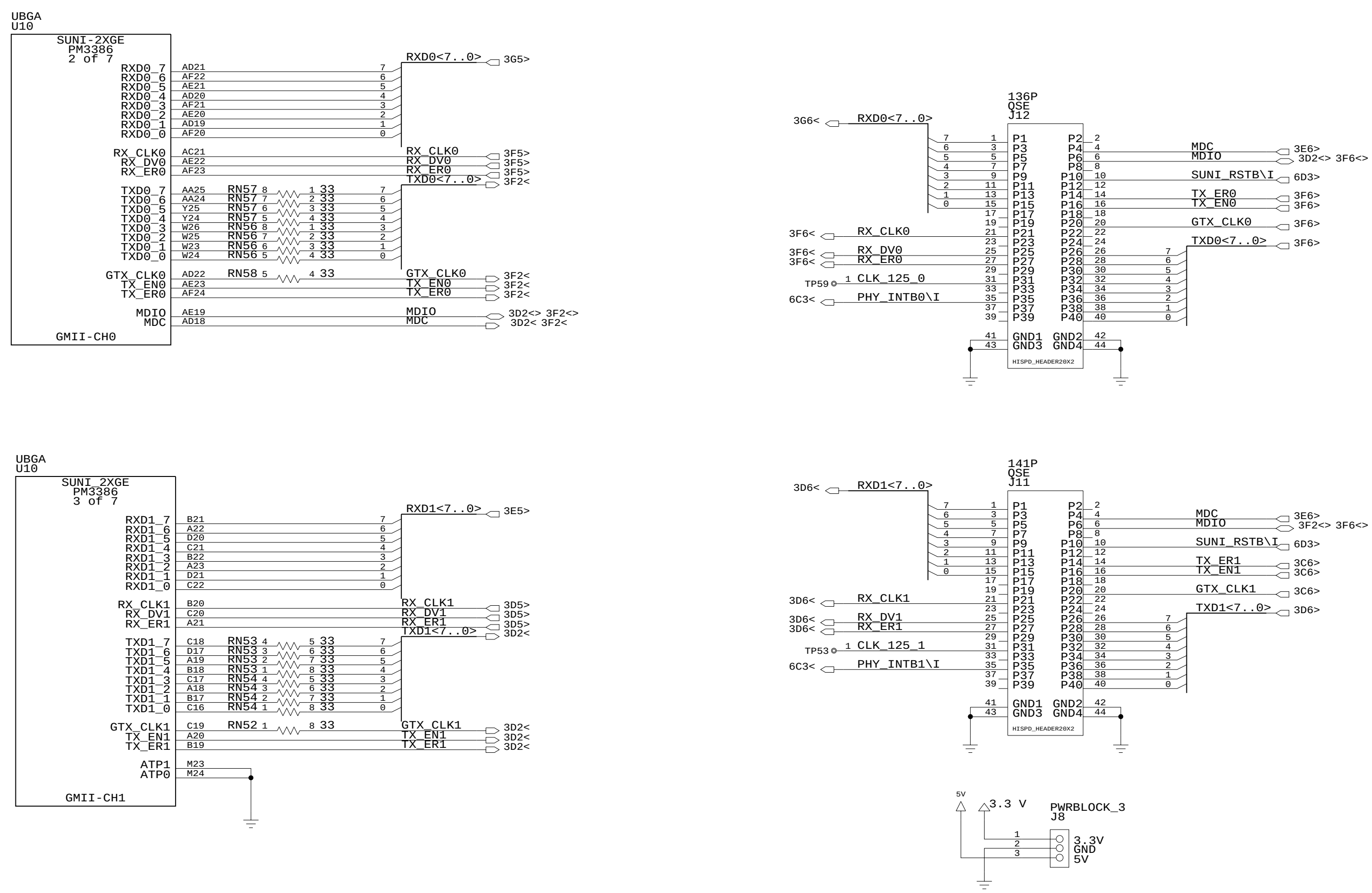

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ENGINEER: BDV	PAGE:3 OF 13

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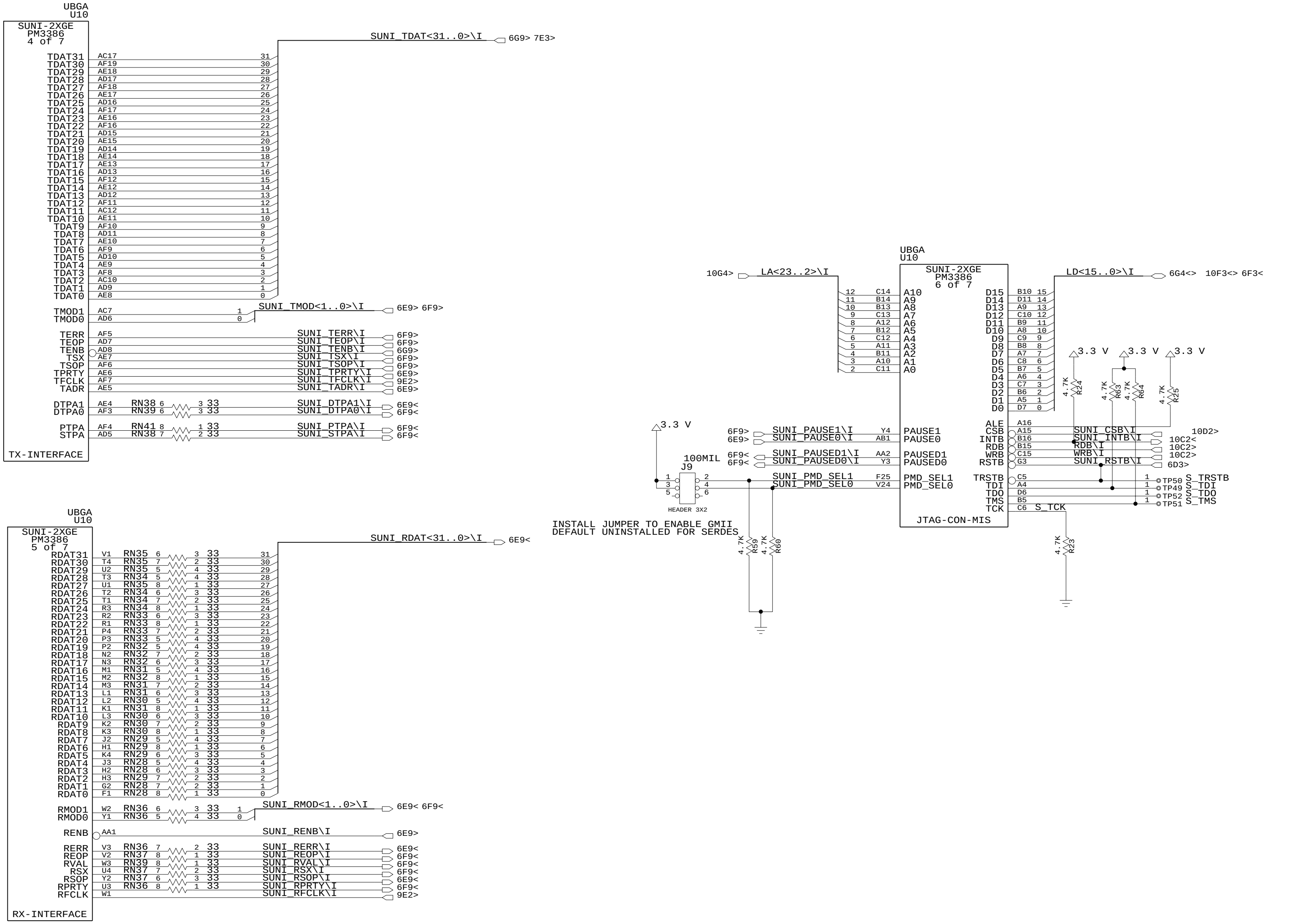

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ENGINEER: BDV	PAGE:4 OF 13

REVISIONS

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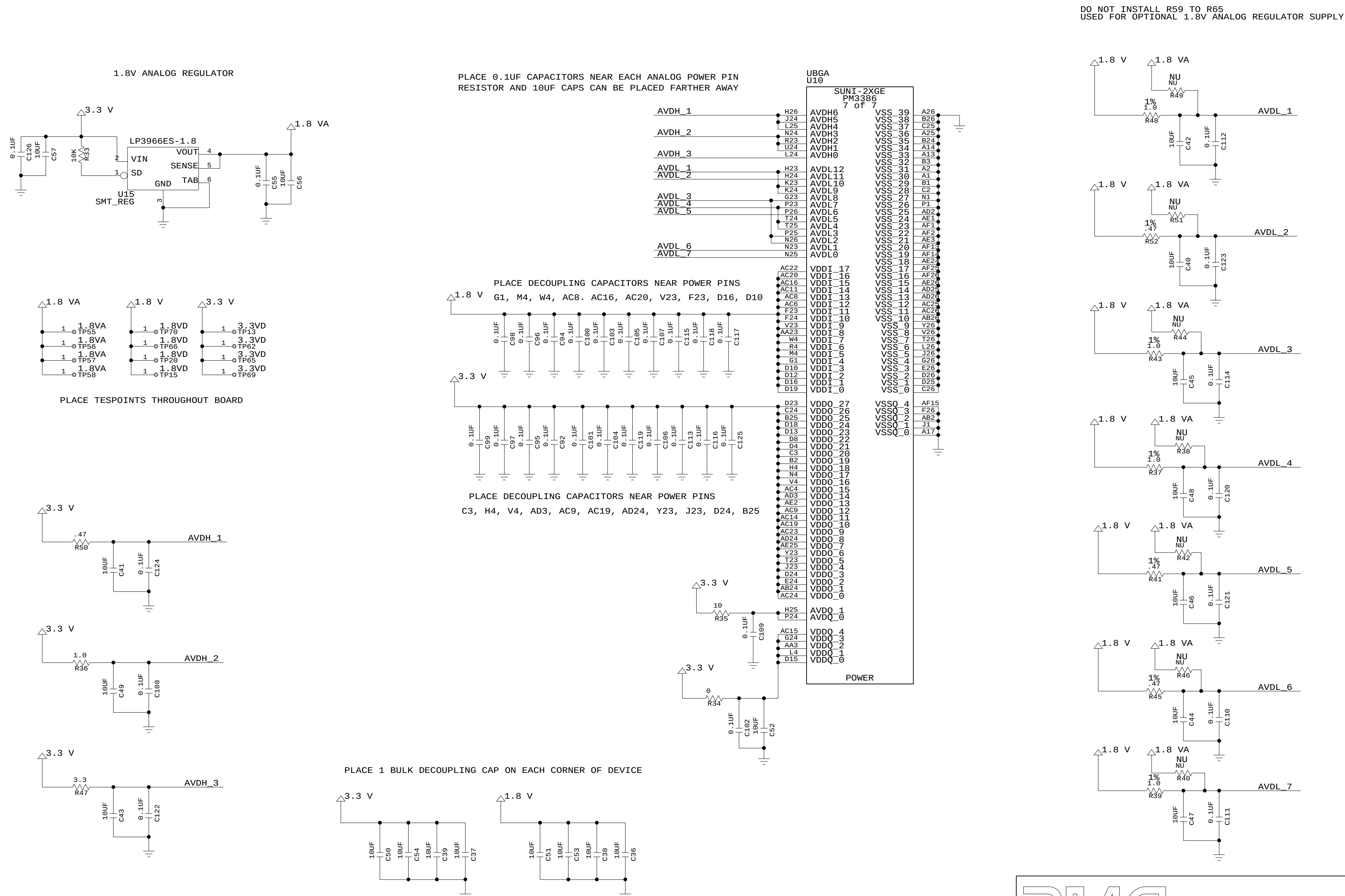

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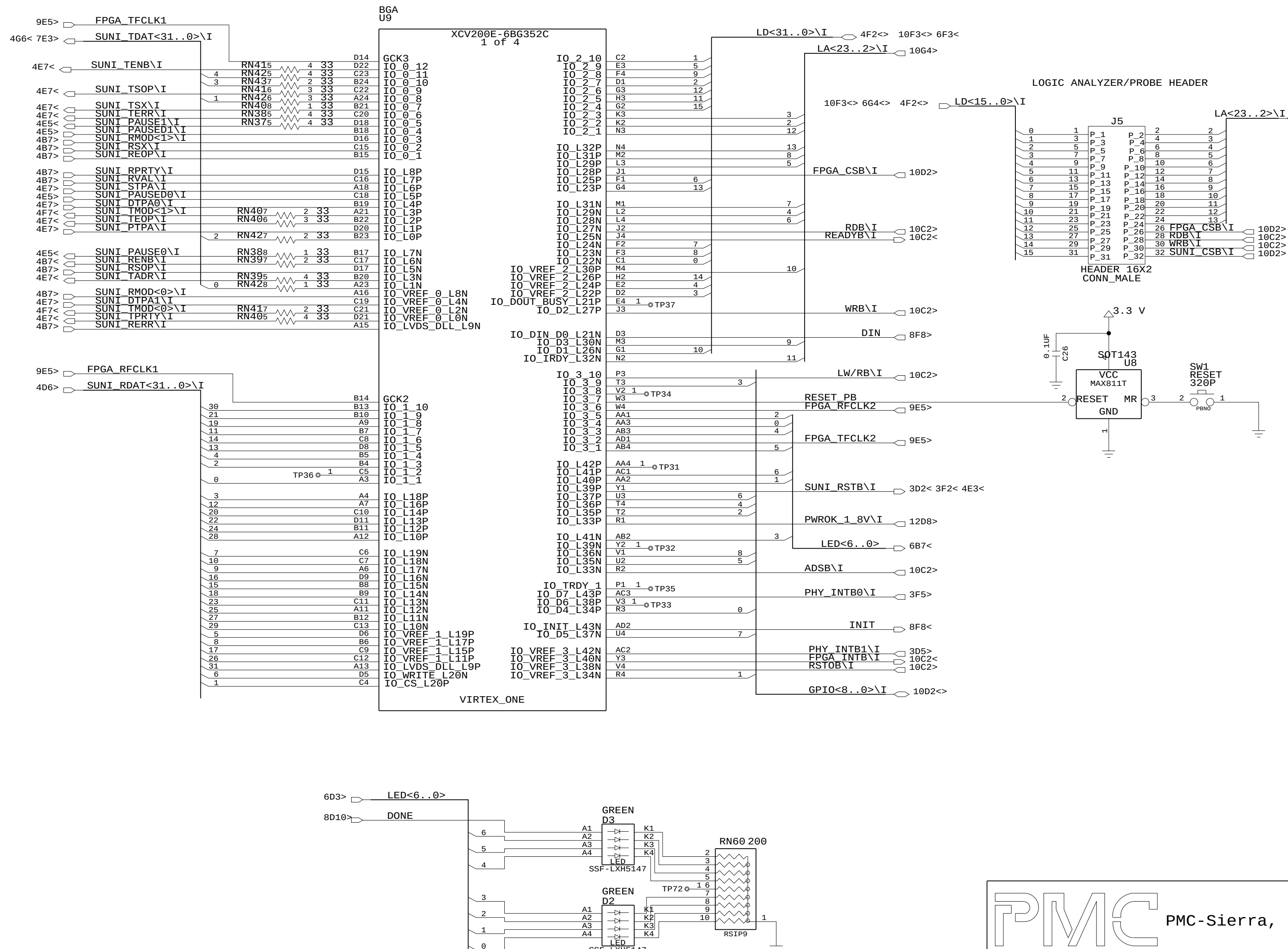

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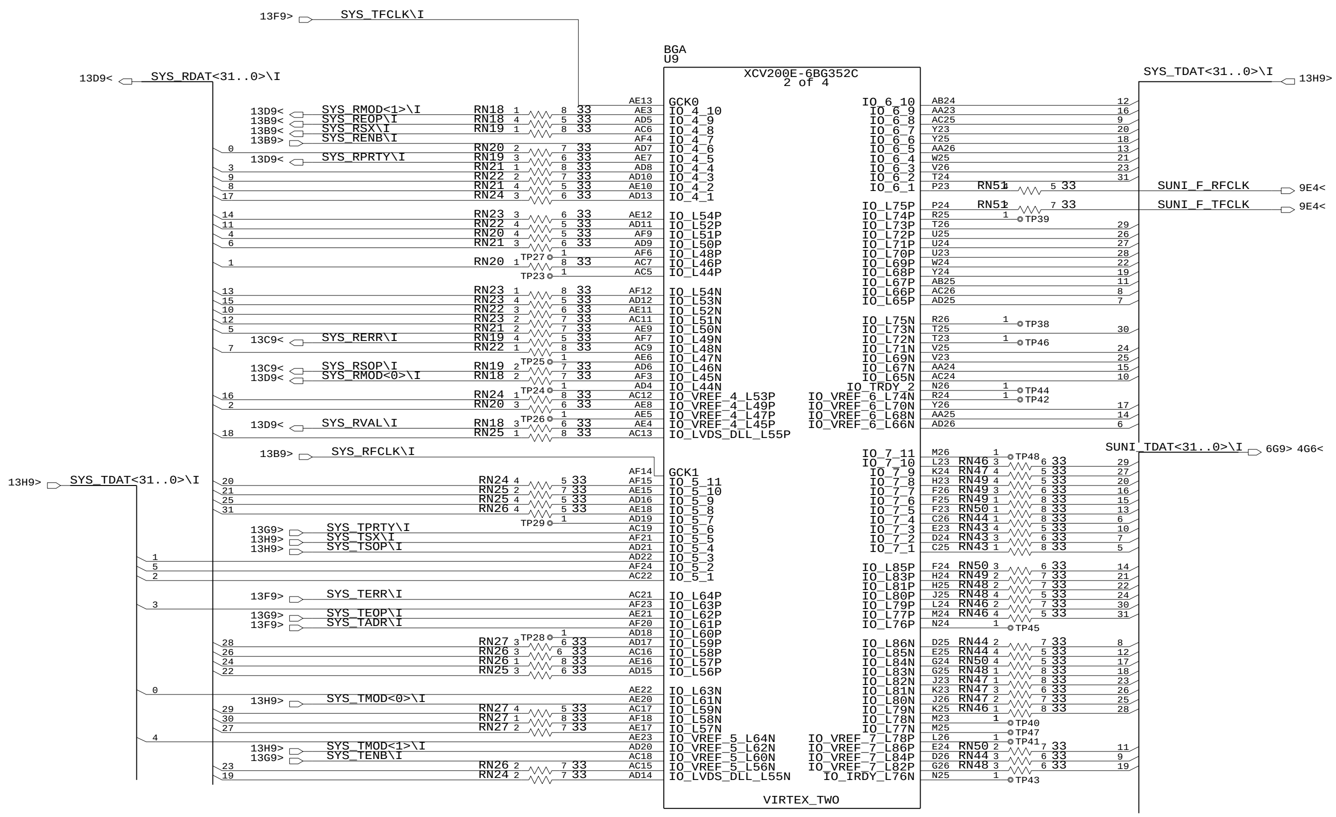
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



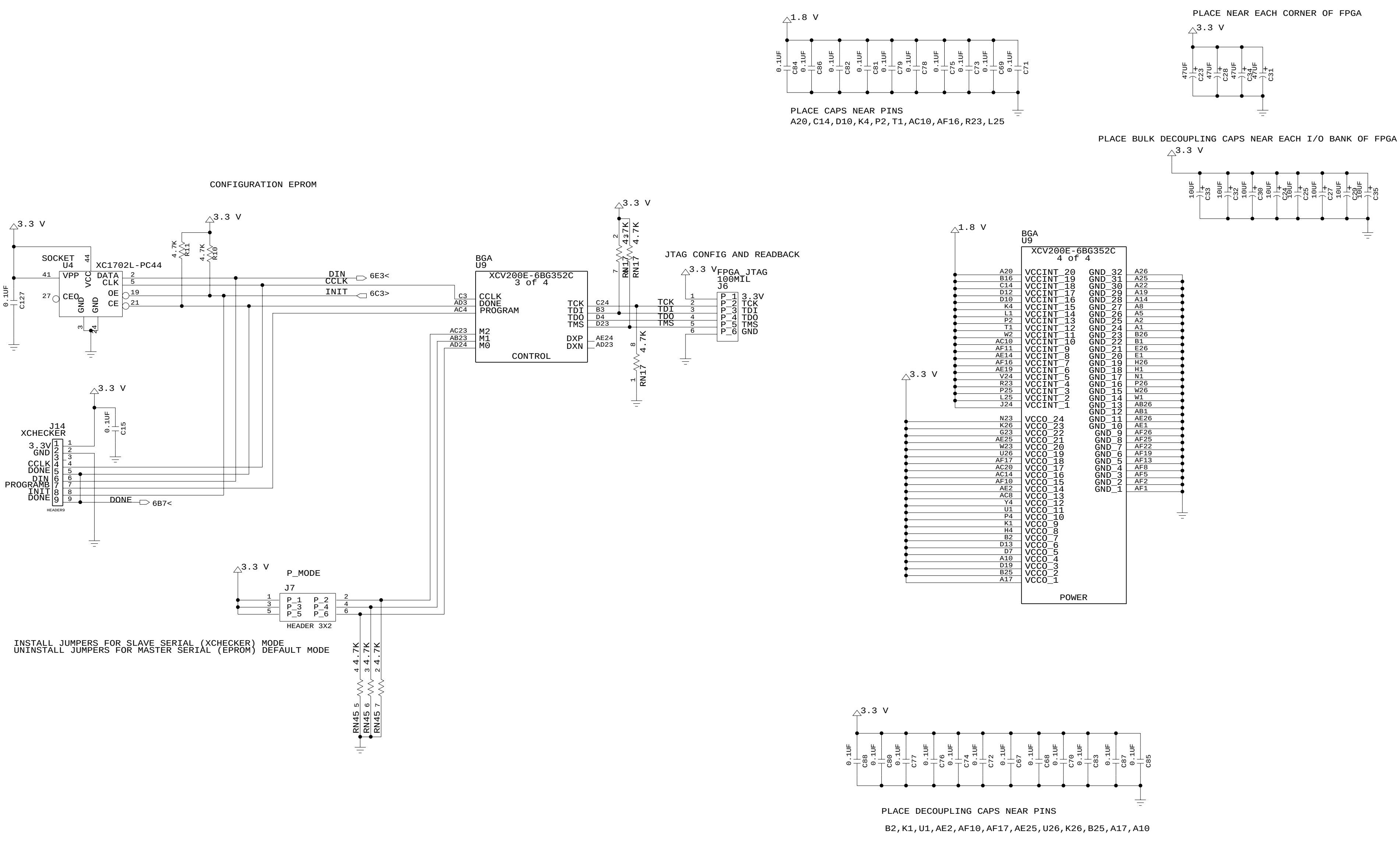
DRAWING:
FPGA_BLOCK
FPGA_BLOCK
Tue Jan 30 16:25:00 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000991 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: SUNI 2XGE REFERENCE DESIGN FPGA PL3 I/F	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:7 OF 13

ZONE	REV	DESCRIPTION	DATE	APPR

REVISIONS



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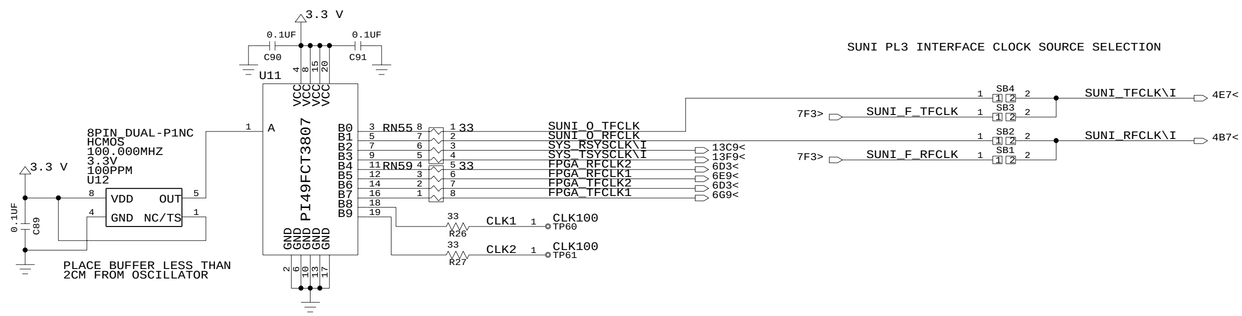
Tue Jan 30 16:25:03 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000991 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: S/UNI-2XGE REFERENCE DESIGN FPGA POWER & CONFIGURATION	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:8 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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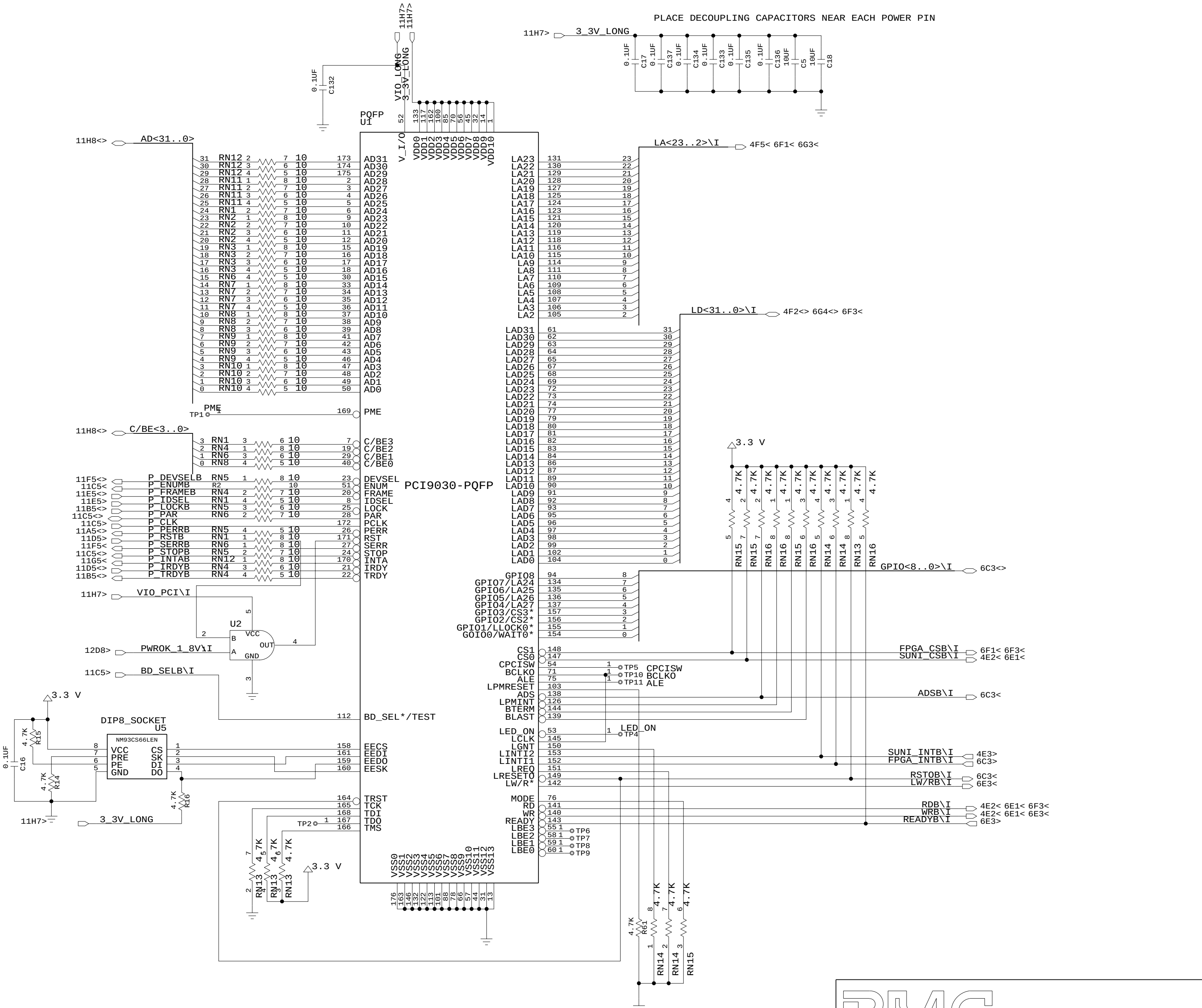
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000991 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YYYY/MM/DD
TITLE: S/UNI 2XGE REFERENCE DESIGN REFCLK AND PL3 CLOCK	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:9 OF 13

TRUE 1

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



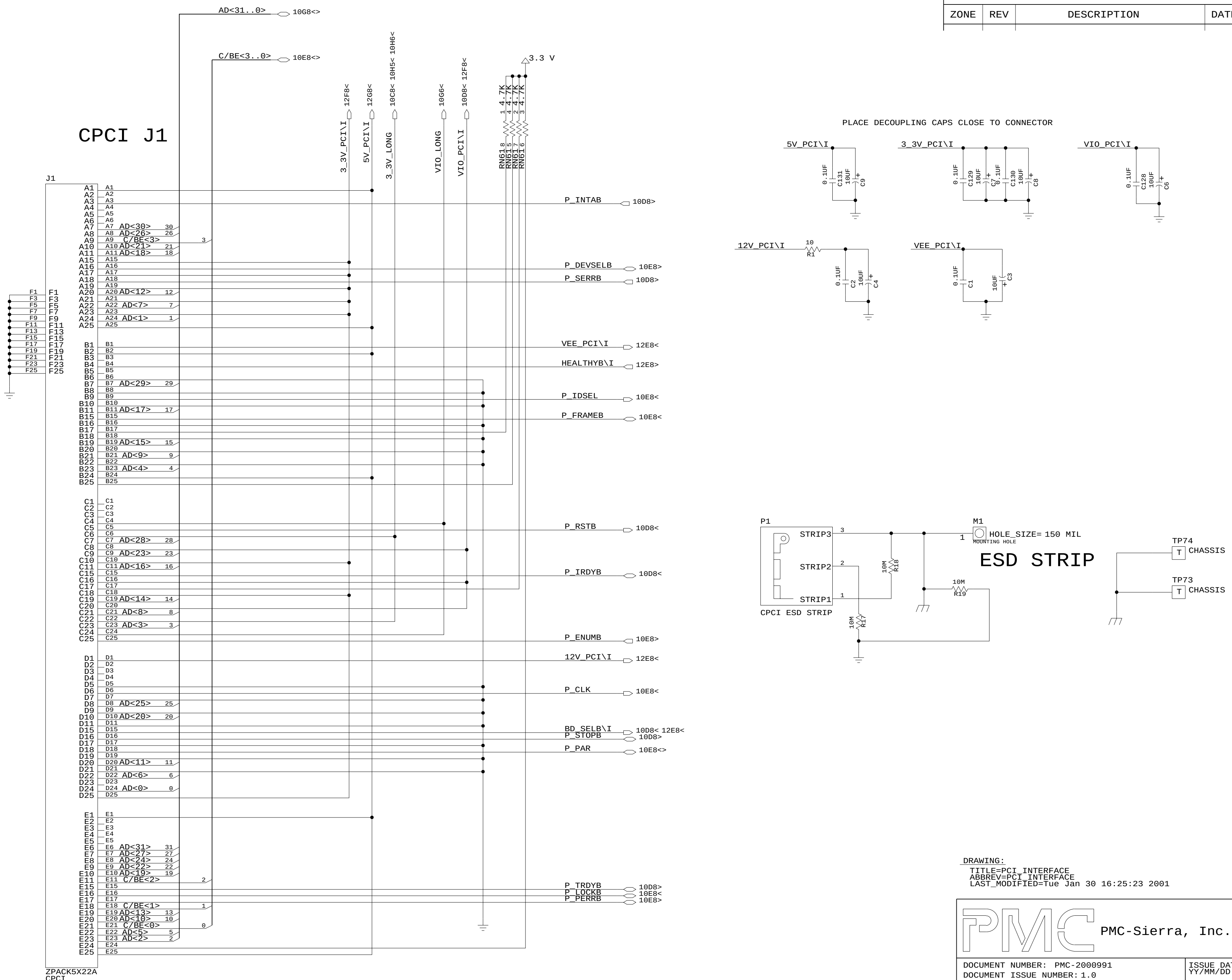
NOTES:
1. ALL 10 OHM STUBS WITHIN 0.6 OF J1
2. ALL PCI SIGNAL TRACES < 1.5 EXCEPT P_CLK
3. P_CLK TRACE MUST BE 2.5 +/- 0.1
4. CPCI BUS TRACES ARE 65 OHM
5. 39 OHM STUB RESISTOR ON REQB PLACED NEAR BRIDGE PIN

DRAWING:
PCI_INTERFACE
PCI_INTERFACE
Tue Jan 30 16:25:20 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000991 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: S/UNI-2XGE REFERENCE DESIGN CPCI INTERFACE	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:10 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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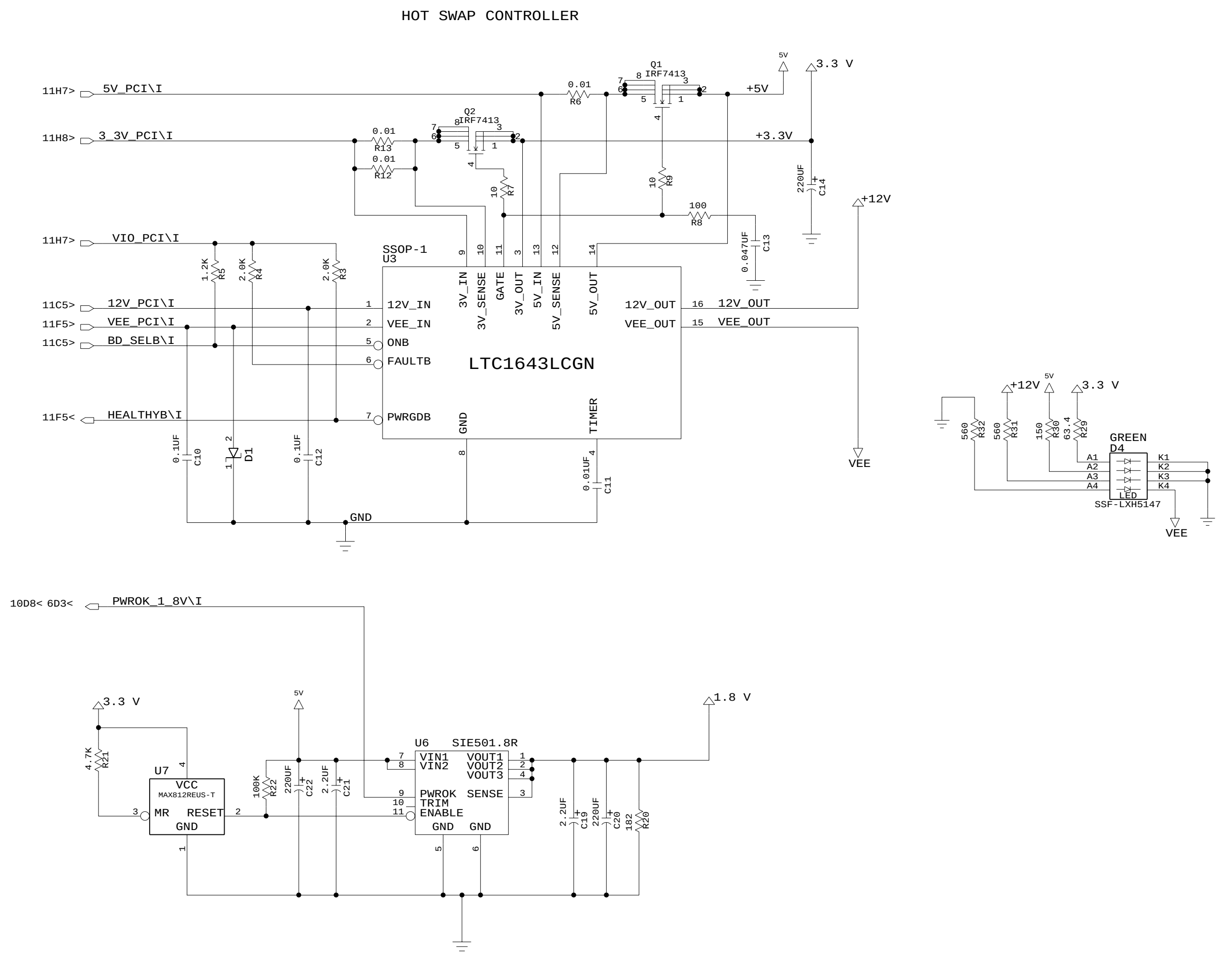
ABBREV=PCI_INTERFACE
LAST_MODIFIED=Tue Jan 30 16:25:23 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000991 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: S/UNI-2XGE REFERENCE DESIGN CPCI CONNECTOR	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:11 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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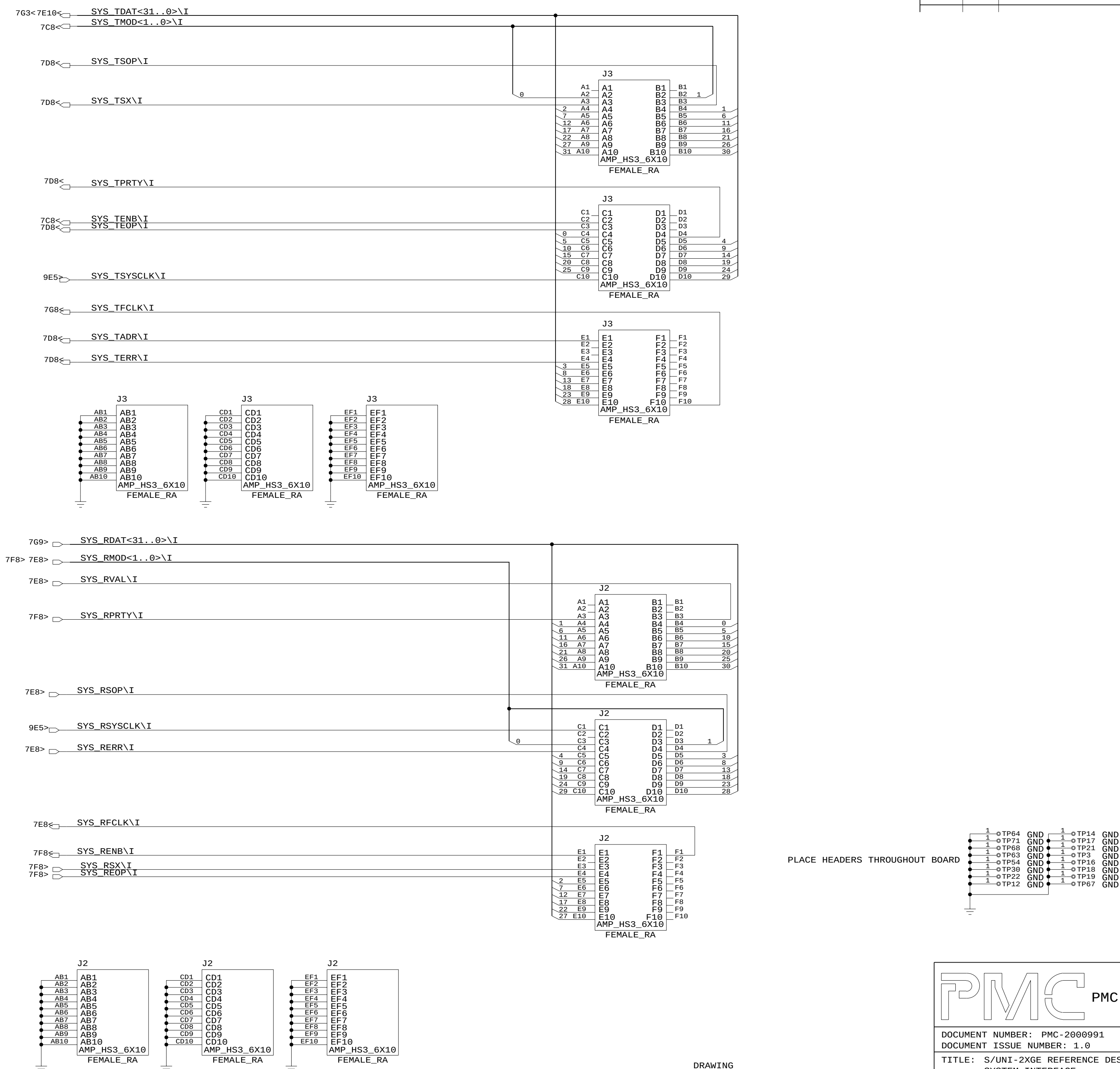
ABBREV=POWER_BLOCK
LAST_MODIFIED=Tue Jan 30 16:25:28 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991414 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: SUNI-2XGE REFERENCE DESIGN POWER_BLOCK	REVISION NUMBER: 3
ENGINEER: BDV	PAGE:12 OF 13

ZONE	REV	DESCRIPTION	DATE	APPR

REVISIONS



DRAWING
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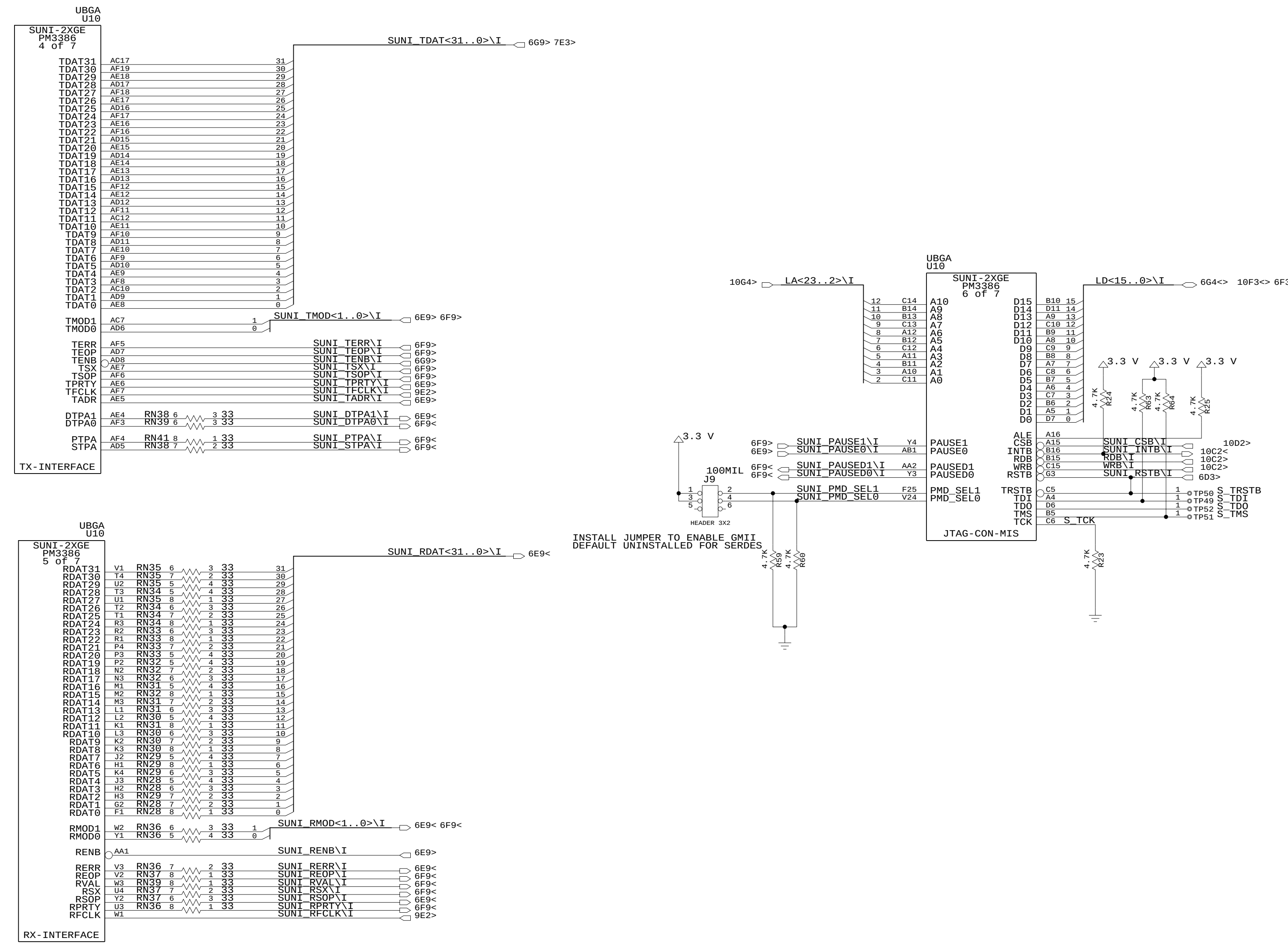
ABBREV=SYS_INTERFACE
LAST_MODIFIED=Tue Jan 30 16:25:25 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000991 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YYYY/MM/DD
TITLE: S/UNI-2XGE REFERENCE DESIGN SYSTEM INTERFACE	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:13 OF 13

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

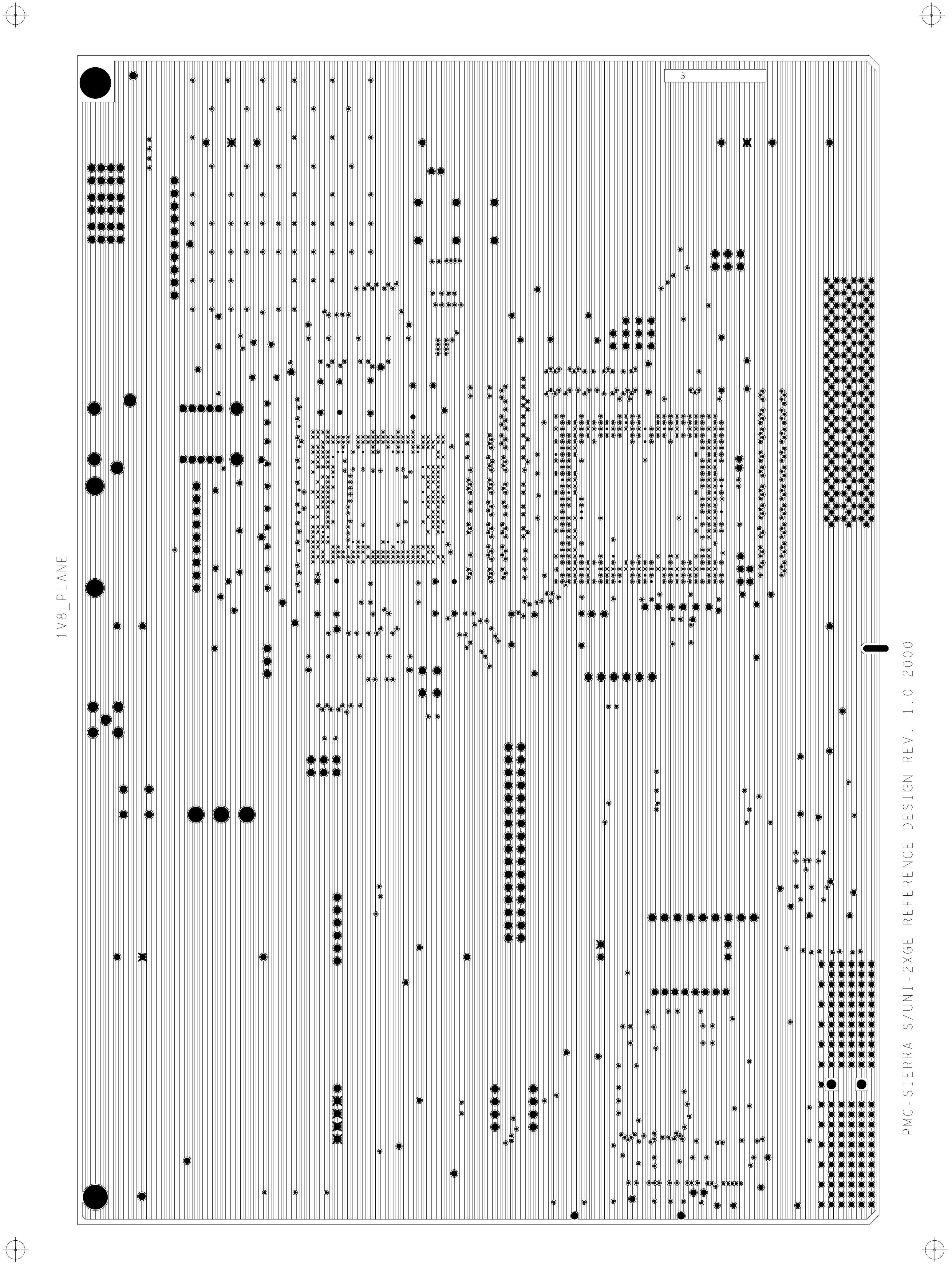


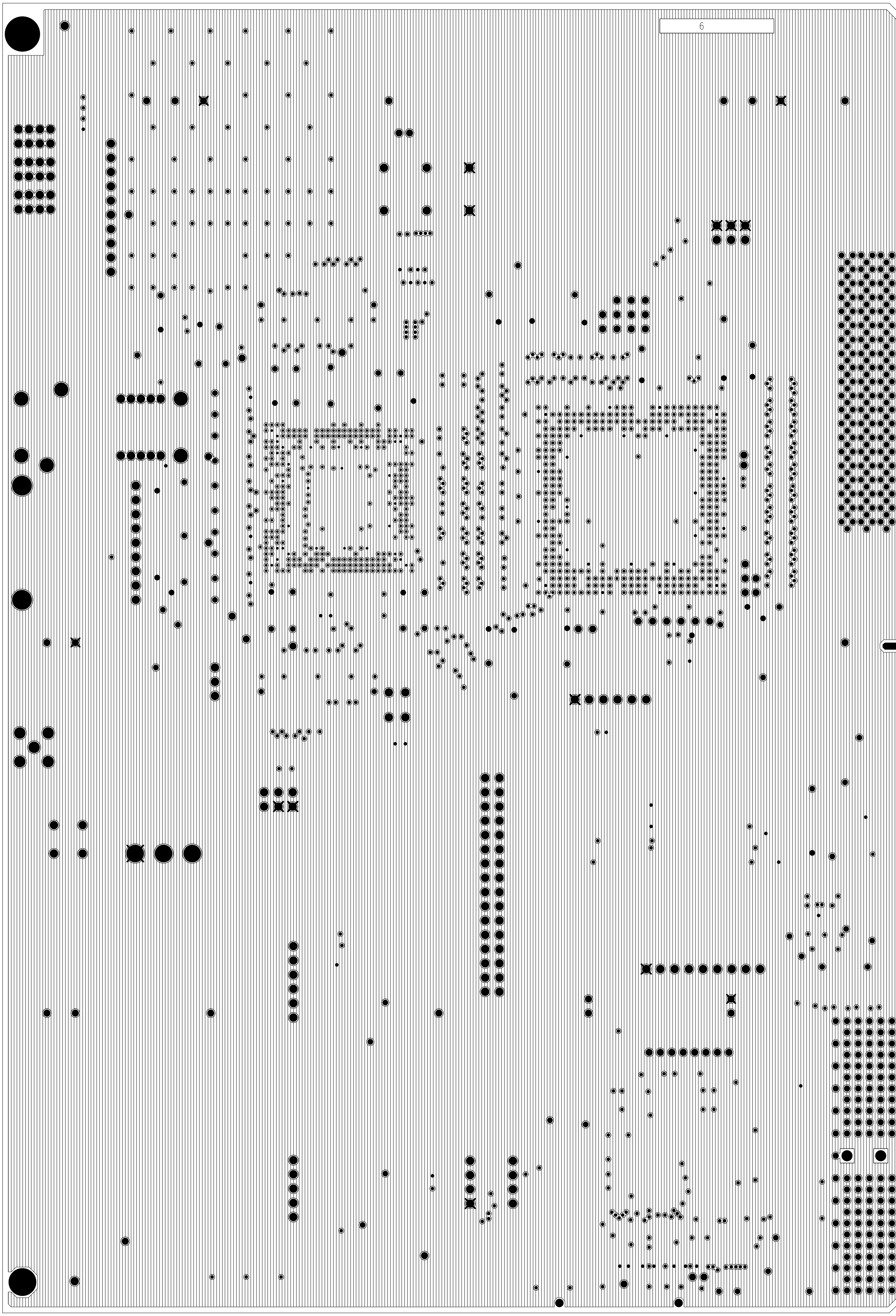
DRAWING:
2XGE_BLOCK
2XGE_BLOCK
Tue Jan 30 16:25:12 2001

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000991 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: S/UNI-2XGE REFERENCE DESIGN PL3 & MICRO INTERFACE	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:4 OF 13

12 PCB Layout Revision 1

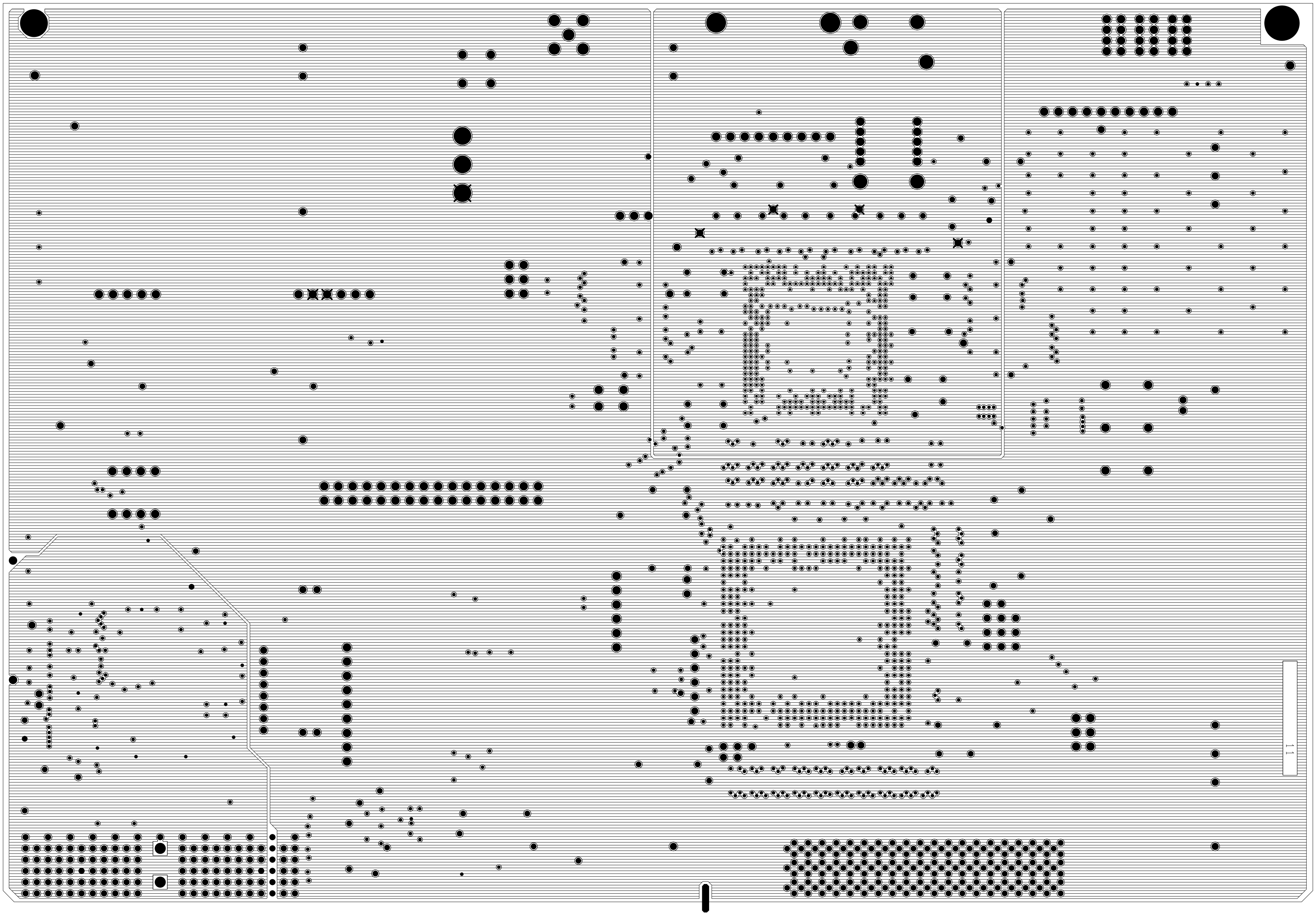

3
1V8_PLANE
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000



3V3_PLANE

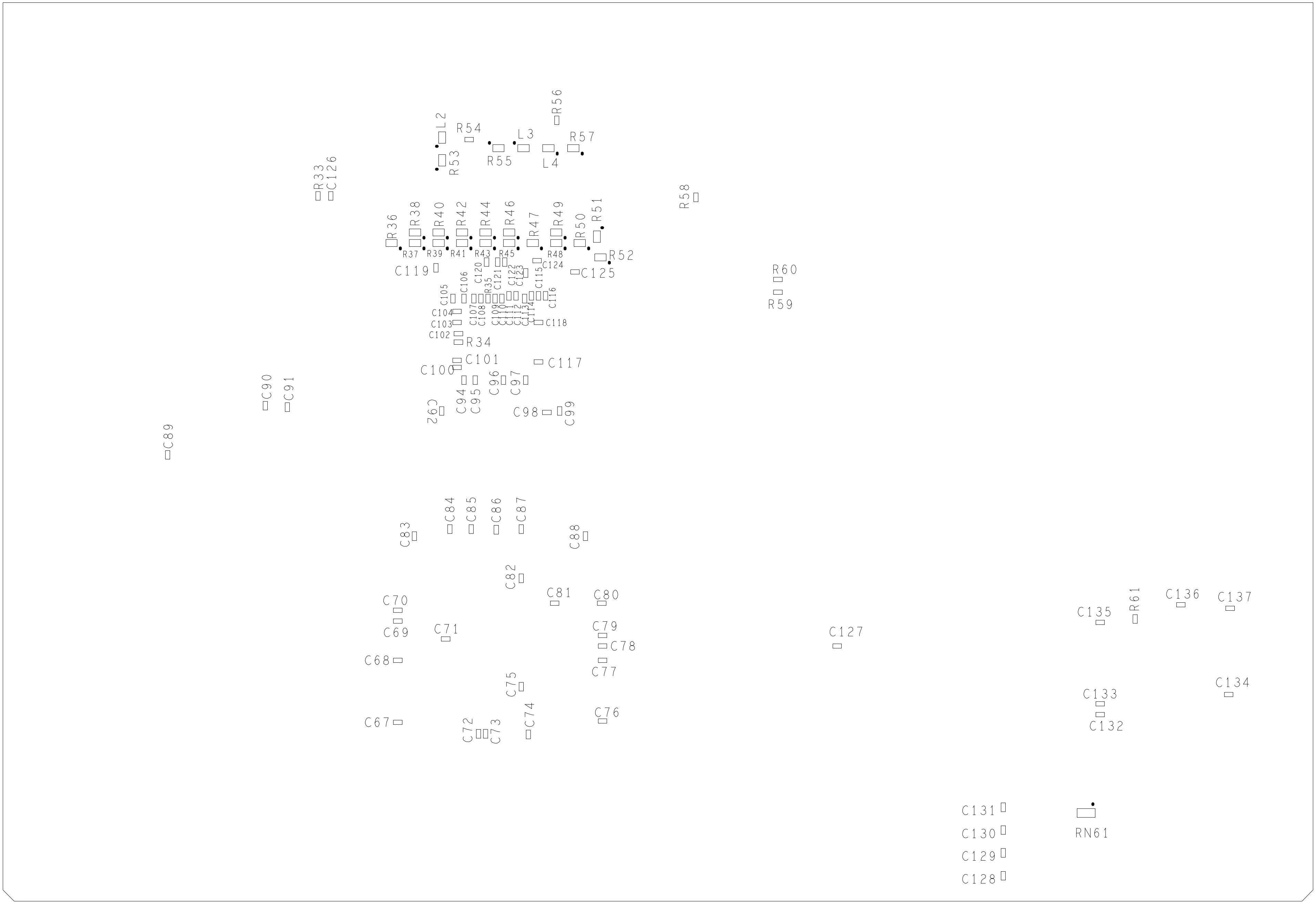
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

5V_3V3L_PLN

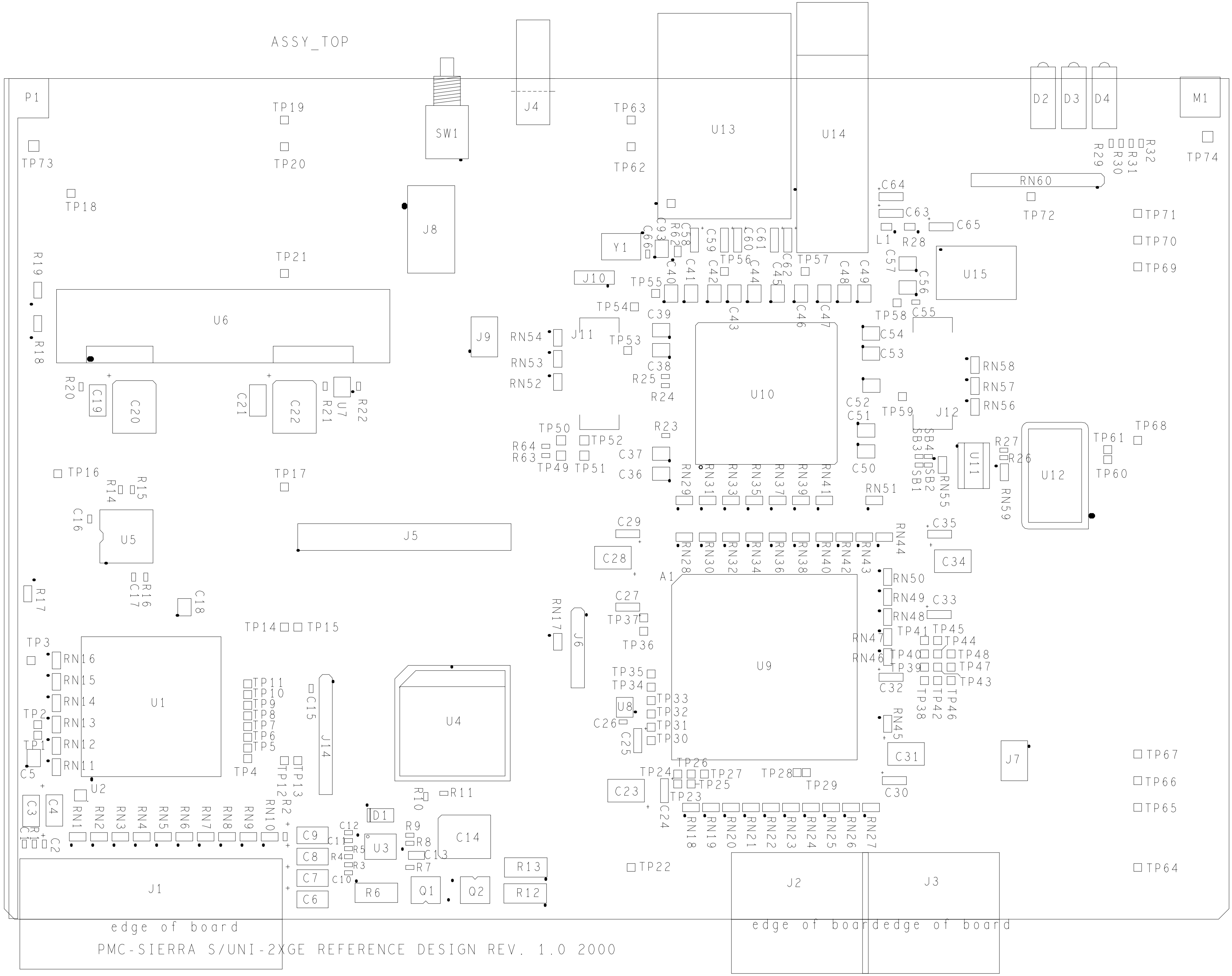


PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

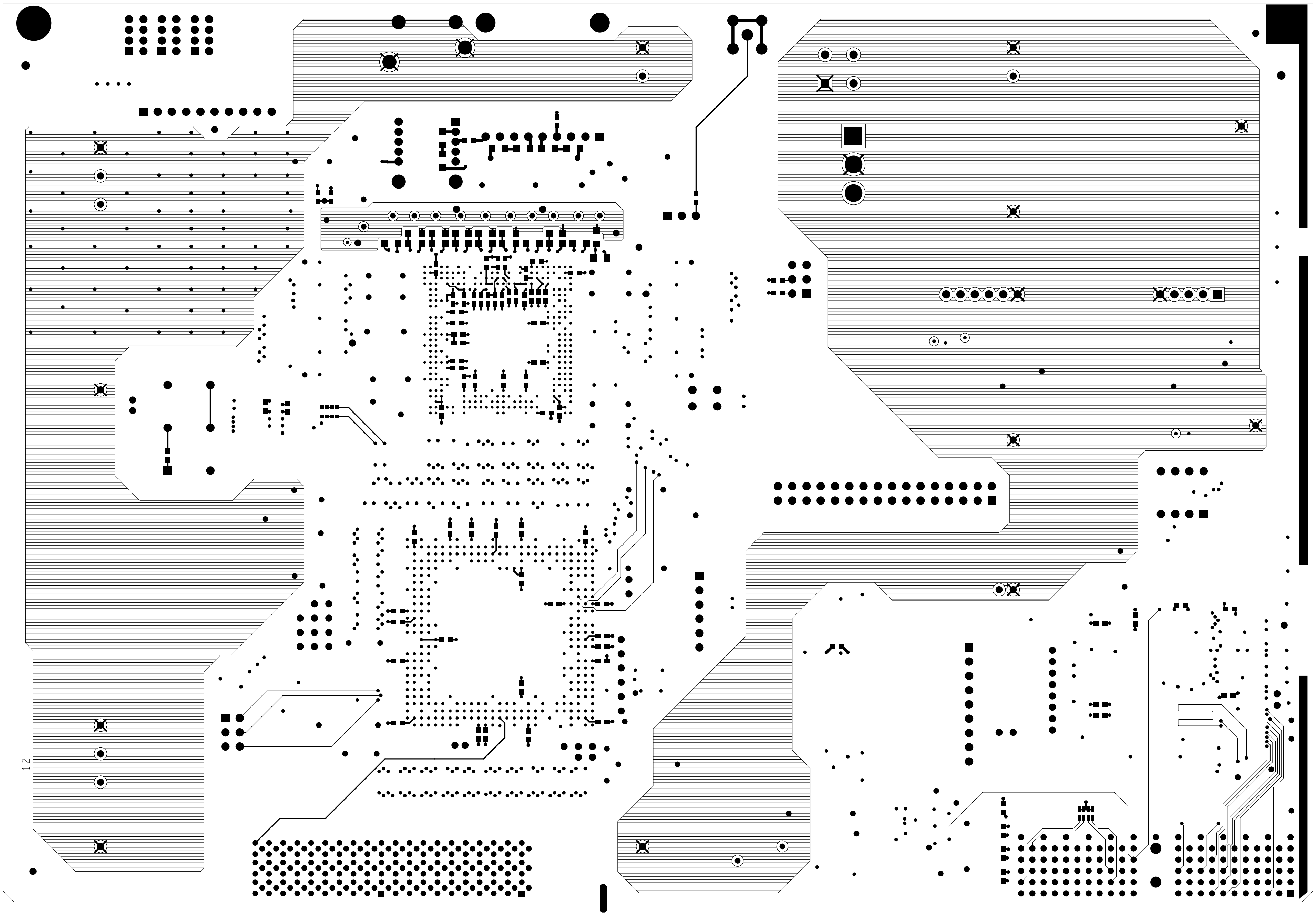
ASSY_BOTTOM



PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000


ASSY_TOP
edge of board
edge of board
edge of board
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

BOTTOM LAYER



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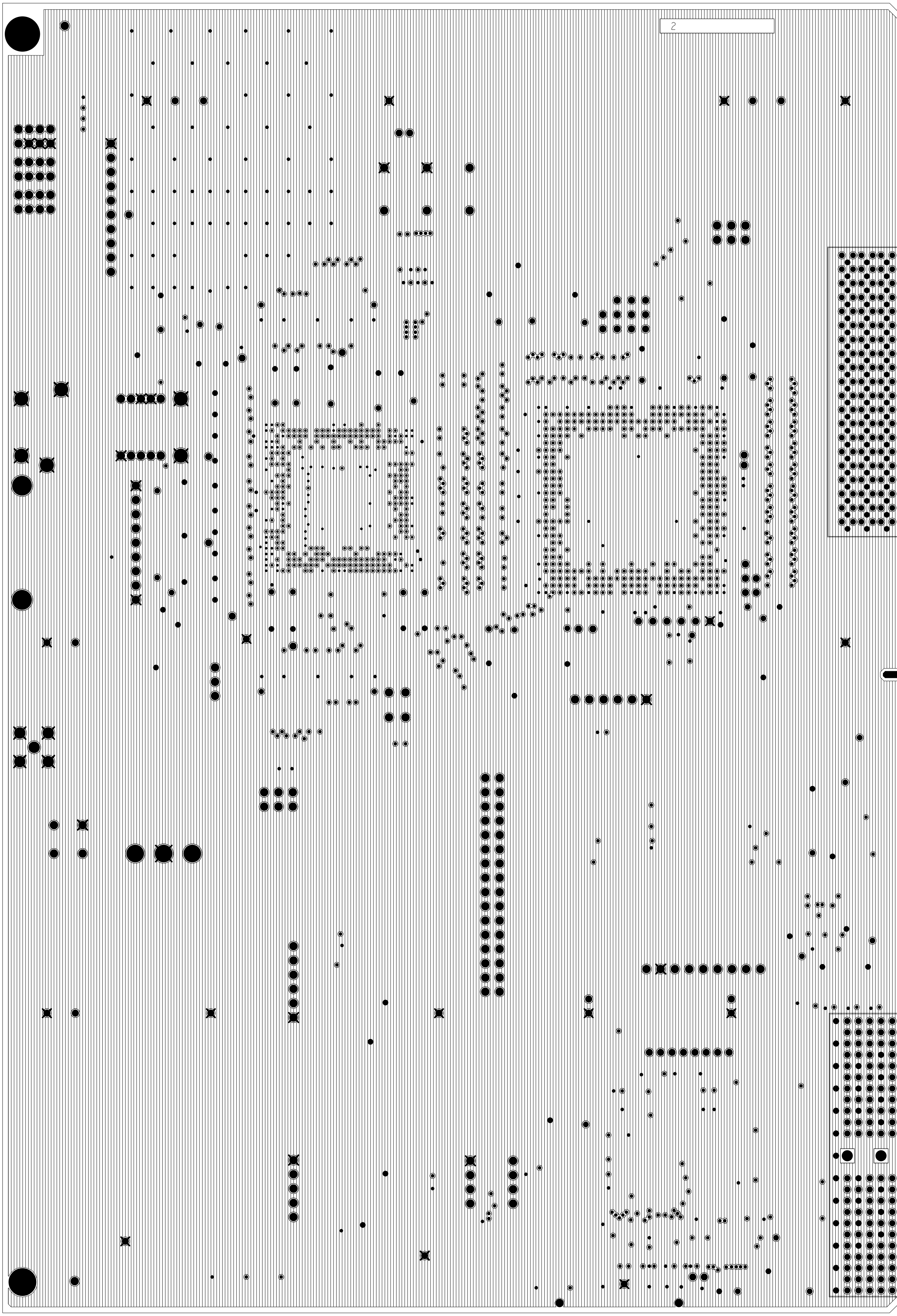
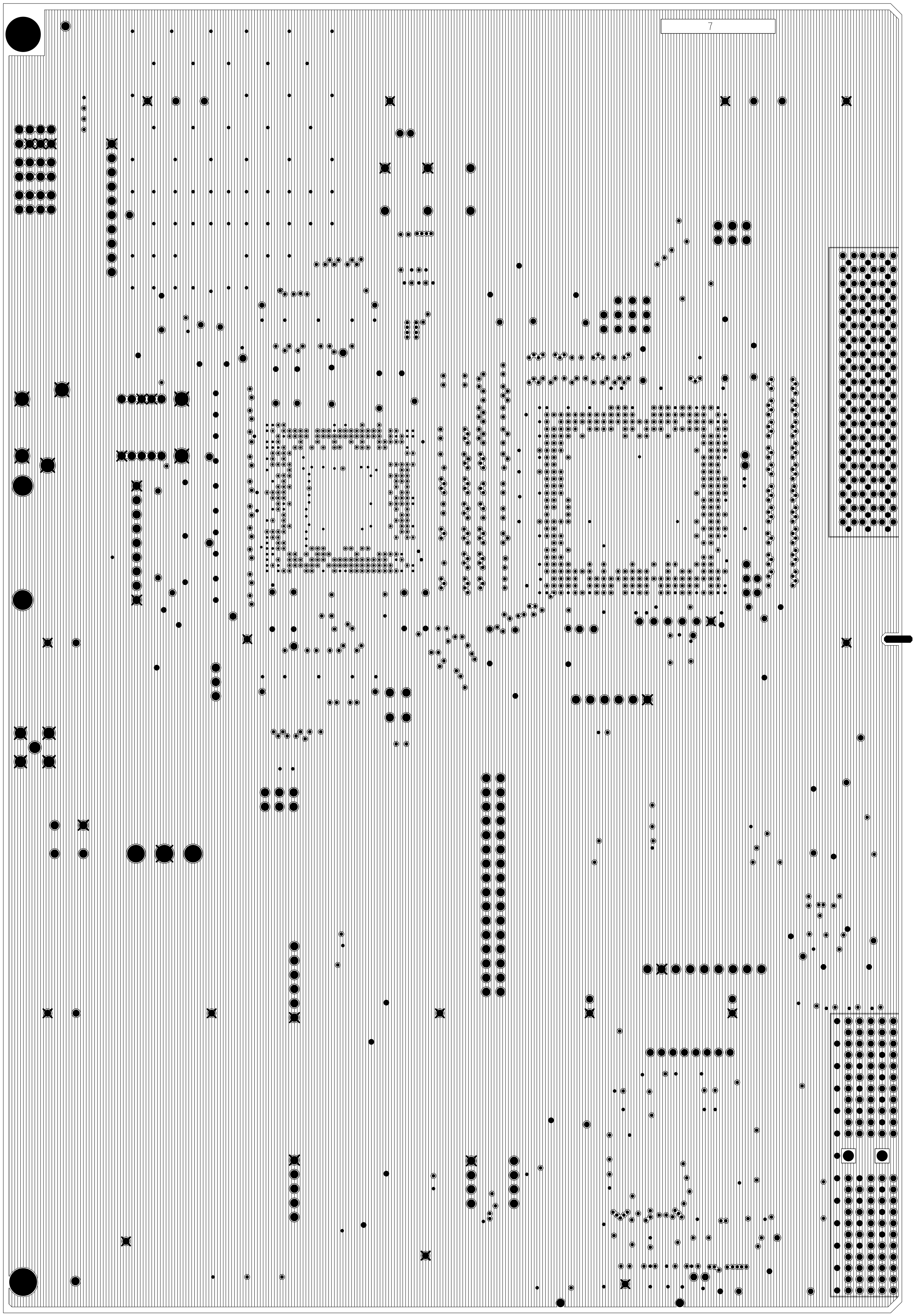


GND1_PLANE

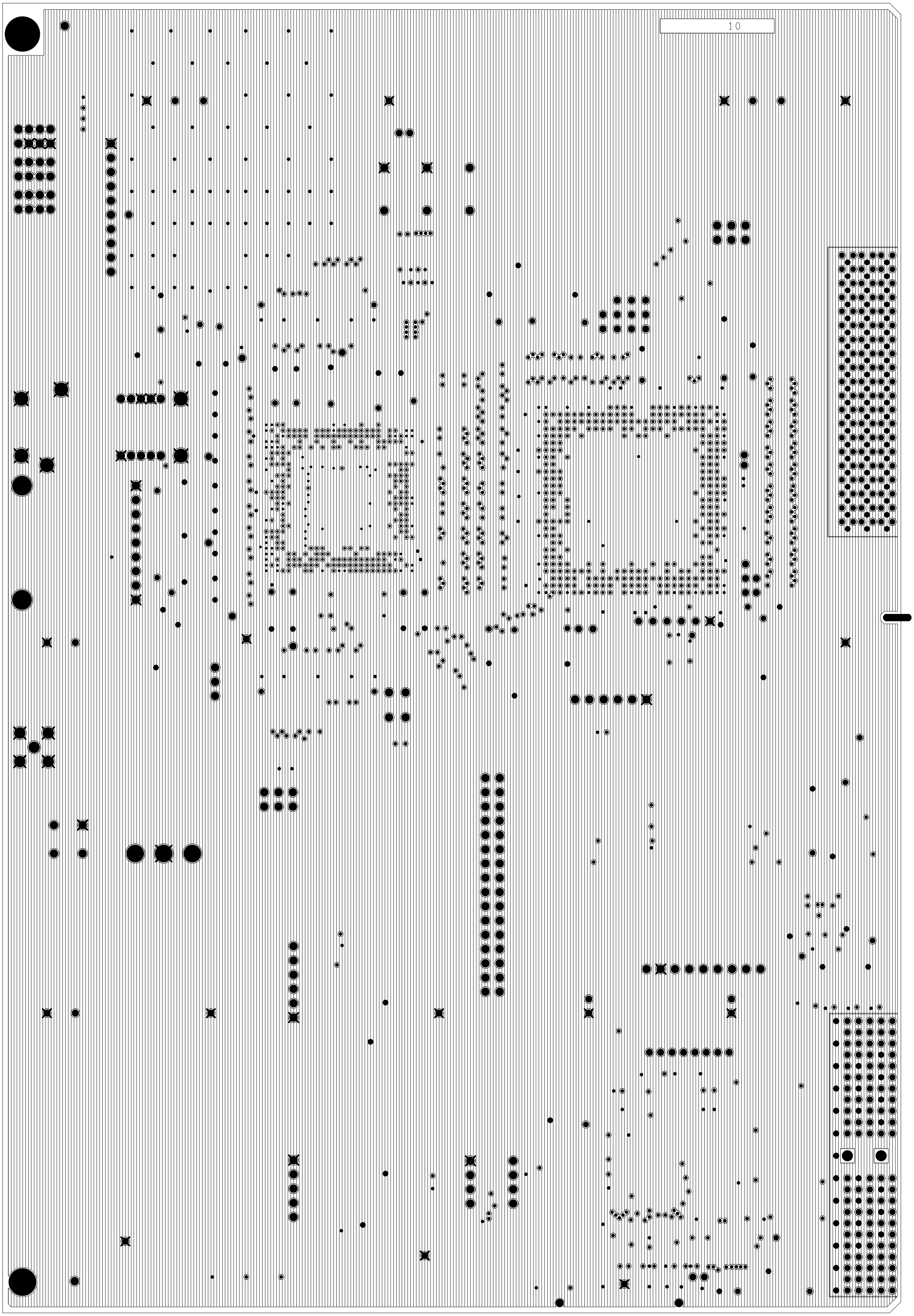
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000



GND2_PLANE

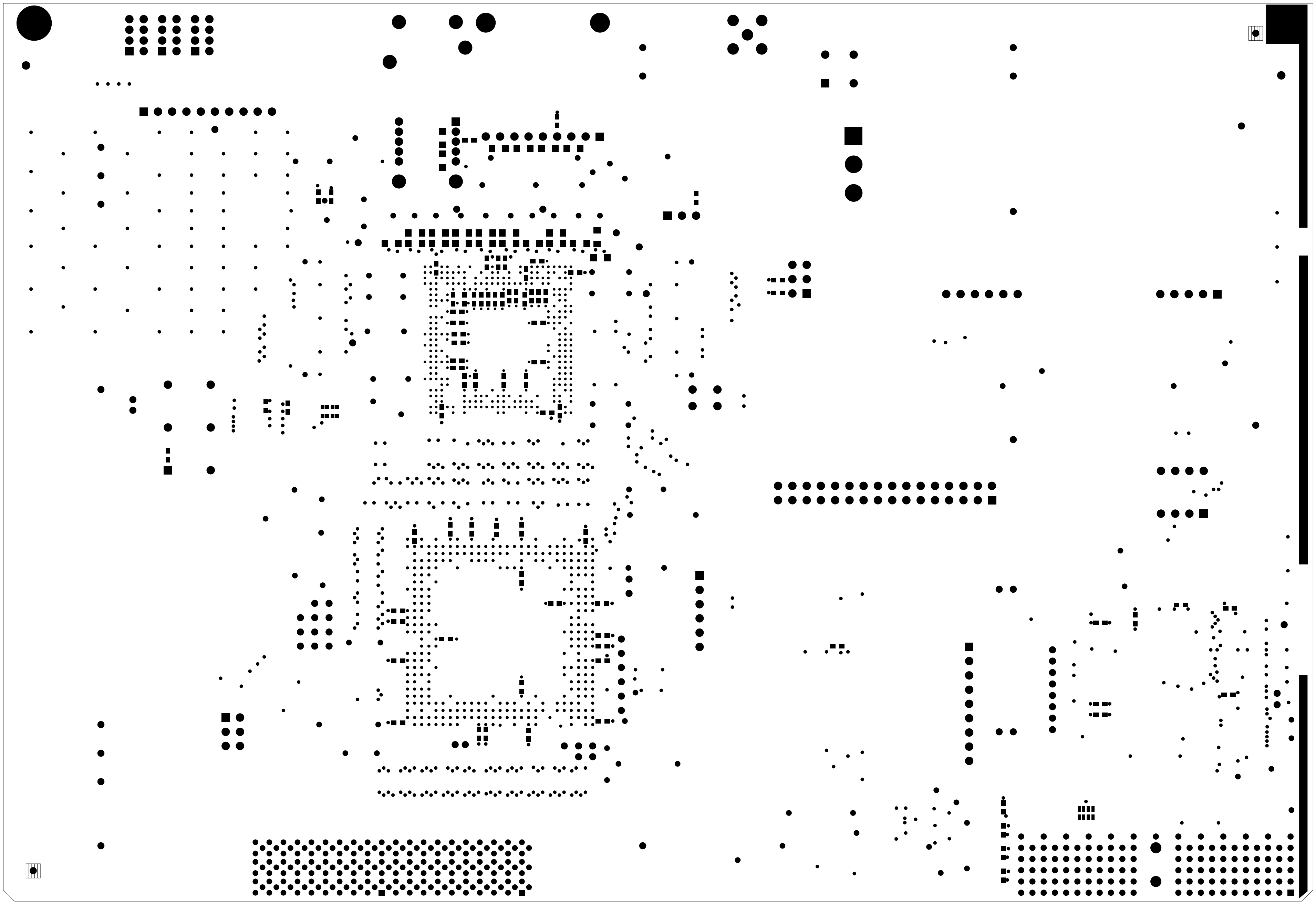
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

GND3_PLANE



PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

SOLDERMASK_BOTTOM



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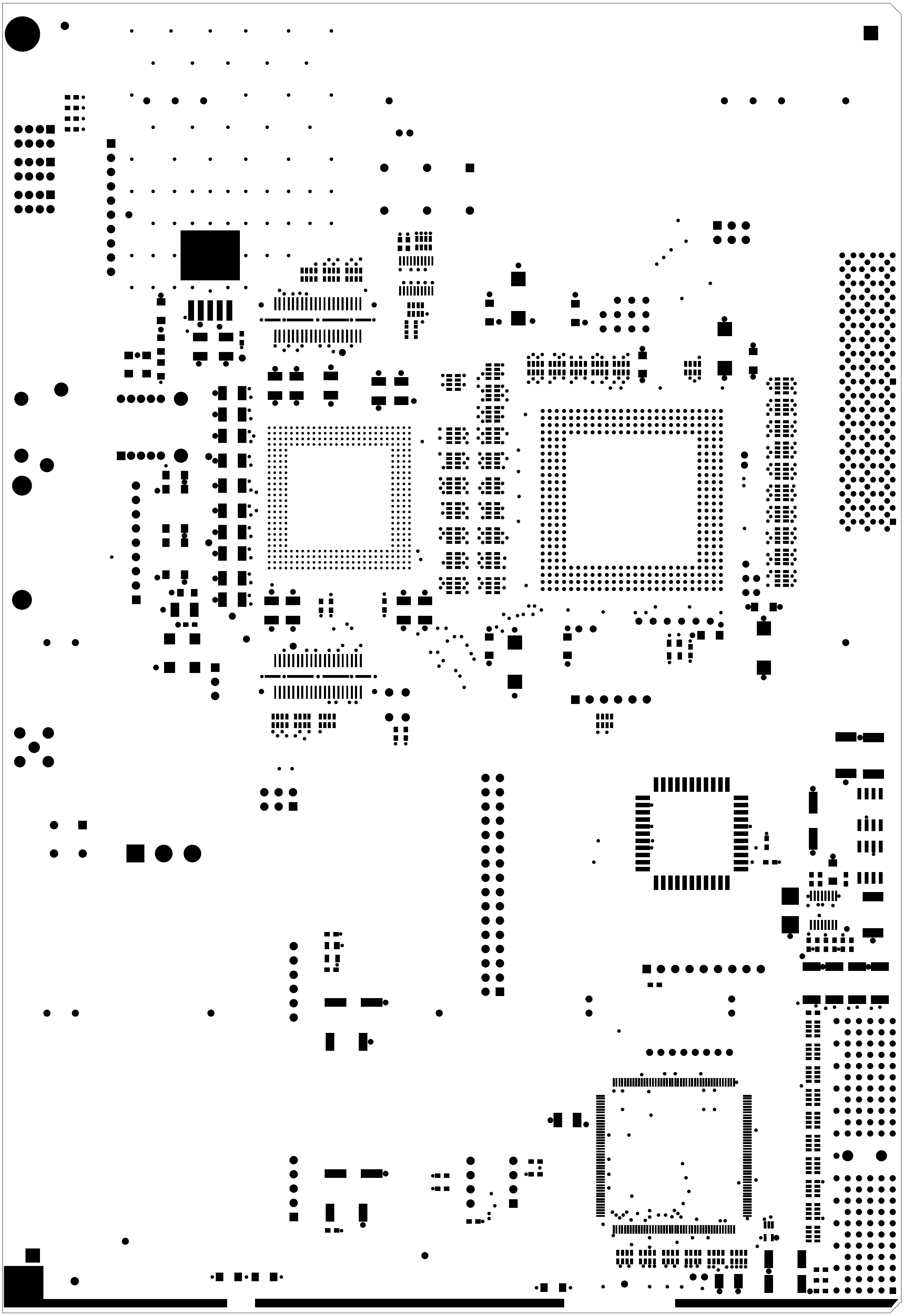


PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

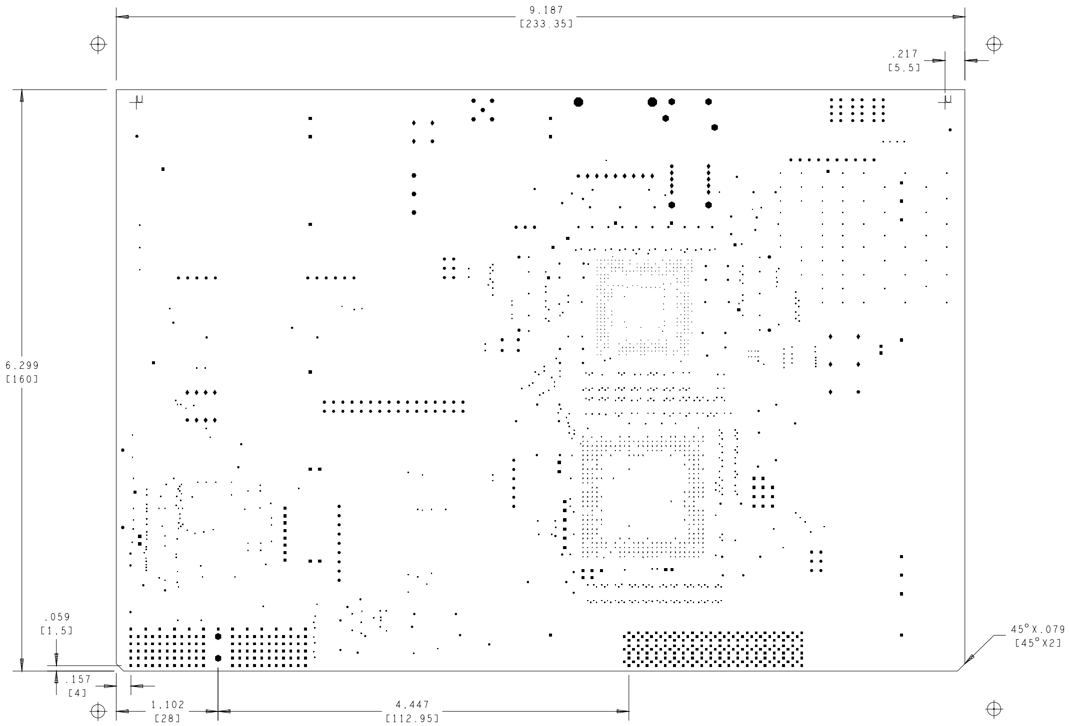
SOLDERMASK_TOP

REV	DESCRIPTION	DATE YY	MM	DD	APPROVED

REVISIONS

	ARTWORK FILM
# 50 & 65 OHM	TOP LAYER
	GND1_PLANE
	1V8_PLANE
# 50 OHM	SIG1 LAYER
# 50 OHM	SIG2 LAYER
	3V3_PLANE
	GND2_PLANE
# 50 OHM	SIG3 LAYER
# 50 OHM	SIG4 LAYER
	GND3_PLANE
	5V_3V3L_PLN
# 50 & 65 OHM	BOTTOM LAYER
	SILKSCREEN TOP
	SILKSCREEN BOTTOM
	SOLDER MASK TOP
	SOLDER MASK BOTTOM
	SOLDER PASTE TOP
	SOLDER PASTE BOTTOM
	MECH DRAWING

	Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
	FR-4	DIELECTRIC	-------	-------	5.0 mil	4.3
	COPPER	CONDUCTOR	GND1_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	3.5 mil	4.5
#	COPPER	CONDUCTOR	1V8_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	6.5 mil	4.5
	COPPER	CONDUCTOR	SIG1	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	8.0 mil	4.5
#	COPPER	CONDUCTOR	SIG2	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	6.5 mil	4.5
	COPPER	CONDUCTOR	3V3_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	3.5 mil	4.5
	COPPER	CONDUCTOR	GND2_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	6.5 mil	4.5
#	COPPER	CONDUCTOR	SIG3	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	8.0 mil	4.5
#	COPPER	CONDUCTOR	SIG4	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	6.5 mil	4.5
	COPPER	CONDUCTOR	GND3_PLANE	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------	-------	3.5 mil	4.5
	COPPER	CONDUCTOR	5V_3V3L_PLN	POSITIVE	1.44 mil	-------
	FR-4	DIELECTRIC	-------		5.0 mil	4.3
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------



PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

FINISHED HOLES SIZE			
All Units are in mils			
FIGURE	SIZE	PLATED	QTY
·	8.0	PLATED	294
·	12.0	PLATED	323
·	13.0	PLATED	8
·	13.0	PLATED	601
·	25.0	PLATED	90
•	26.0	PLATED	123
•	26.0	PLATED	180
•	32.0	PLATED	68
•	36.0	PLATED	113
•	39.37	PLATED	2
•	42.0	PLATED	5
•	42.0	PLATED	32
•	52.0	PLATED	5
•	55.0	PLATED	3
●	79.0	PLATED	6
●	108.0	PLATED	2
⊬	149.606	PLATED	1
⊬	150.0	PLATED	1
·	40.0	NOT PLATED	4
●	78.74	NOT PLATED	2

NOTES:

1. COPPER THICKNESS IS 1/2 OZ ON OUTER LAYER AND 1 OZ ON INNER LAYERS, UNLESS OTHERWISE STATED.
2. TOTAL THICKNESS OF BOARD SHALL BE 78 MIL+/- 10% MIL.
3. MATERIAL: FR4 WITH IMMERSION GOLD SURFACE FINISH.
4. THE OUTLINE DIMENSION ARE SPECIFIED ON THIS DRAWING.
5. ALL HOLES SHALL HAVE 1 MIL MINIMUM COPPER WALL THICKNESS.
6. SOLDER MASK MATERIAL: LIGHT GREEN LIQUID PHOTOIMAGEABLE.
7. DIELECTRIC CONSTANT: SEE BOARD MATERIAL DETAILS ABOVE.
8. SILKSCREEN SHALL BE SCREENED IN MONOCONDUCTIVE WHITE BASE INK AND MUST BE CLIPPED AWAY FROM SOLDER PADS/VIAS.
9. MAXIMUM WARP AND TWIST OF FINISHED PCB SHALL NOT EXCEED 0.010 IN/IN PER IPC-D-300.
10. ALL MATERIAL COMPRISING THE PCB MUST BE RECOGNIZED BY UL TO THE 94V-0 RATING.
11. TEARDROPS MAY BE ADDED FOR INNER LAYER VIAS FOR MANUFACTUREABLITY IF NECESSARY.
12. UNFUNCTIONAL INNER LAYERS VIAS/PADS HAVE TO BE REMOVED FOR MANUFACTUREABILITY.
13. PLATED HOLES MARKED WITH SQUARE R OR P 0.026" SHALL BE WITHIN +0.004"/-0.0" TOLERANCE.
14. CAUTION ALL TRACE WIDTH 9 MIL ON OUTER LAYERS ARE 50 OHM +/-10% CONTROLLED IMPEDANCE.
    ALL TRACE WIDTH 6 MIL ON INNER LAYERS ARE 50 OHM +/-10% CONTROLLED IMPEDANCE.
    ALL TRACE WIDTH 5 MIL ON OUTER LAYERS ARE 65 OHM +/-10% CONTROLLED IMPEDANCE.

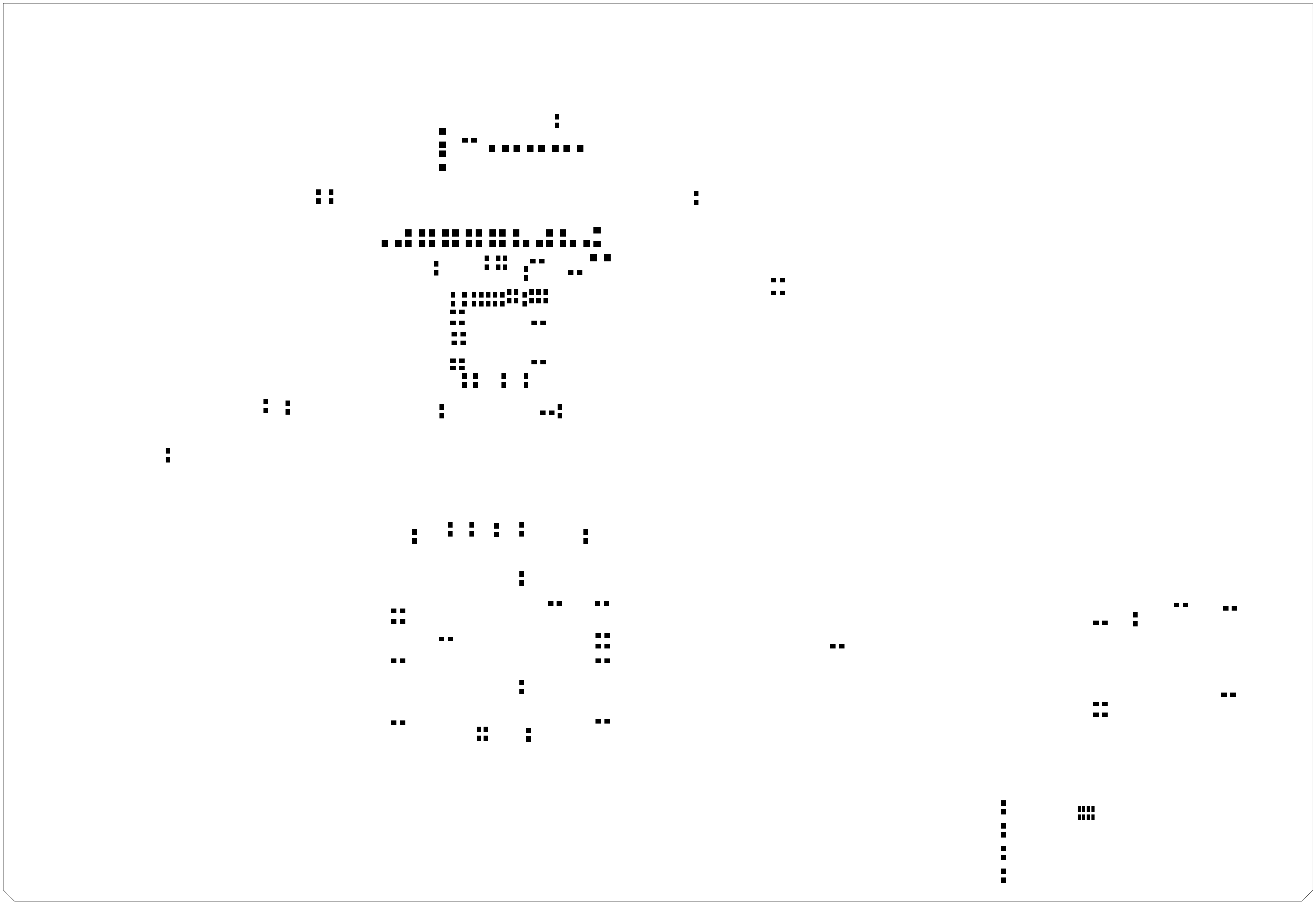
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
2 PL DECIMALS ±
3 PL DECIMALS ±
ANGLES ±
FRACTIONS ±

	DATE YY	MM	DD
DRAWN			
CHECKED			
ENGRG			
ISSUED			

PMC-Sierra, Inc.
105-8555 Baxter Place, Burnaby B.C.
Canada, V5A 4V7
Tel: 604 415-6000 Fax: 604 415-6200

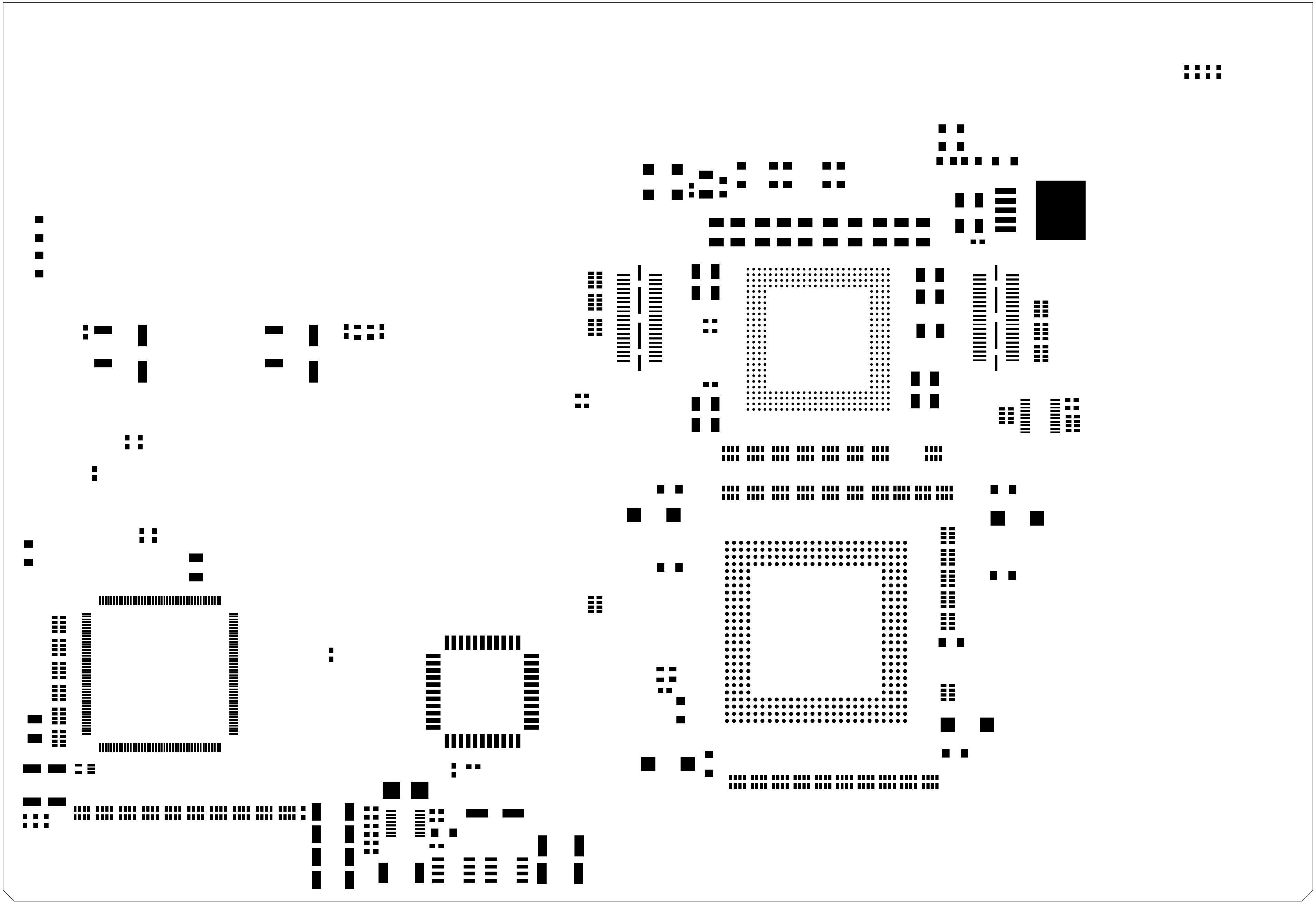
SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET OF

PASTEMASK_BOTTOM



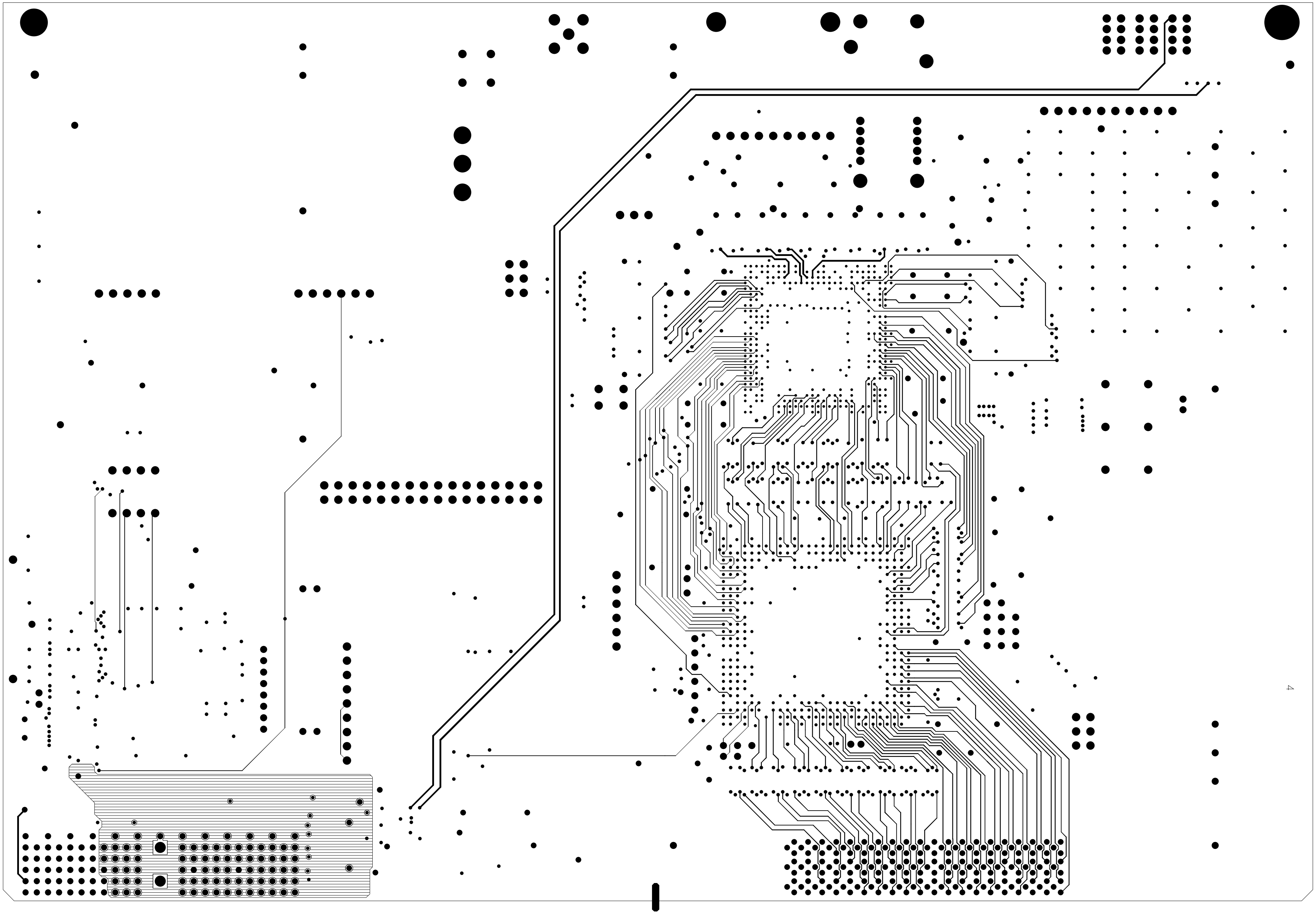
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

PASTEMASK_TOP

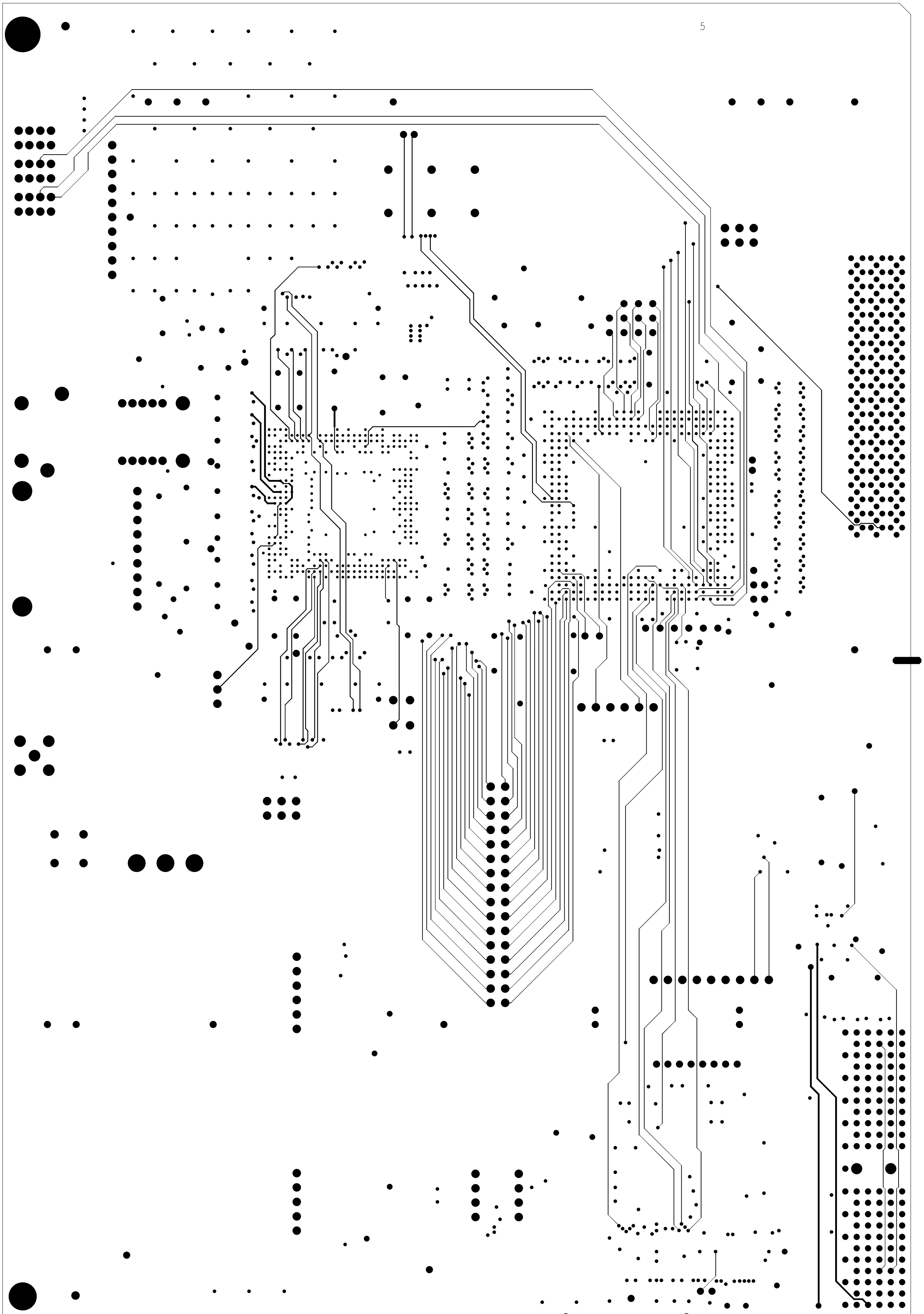


PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

SIG1

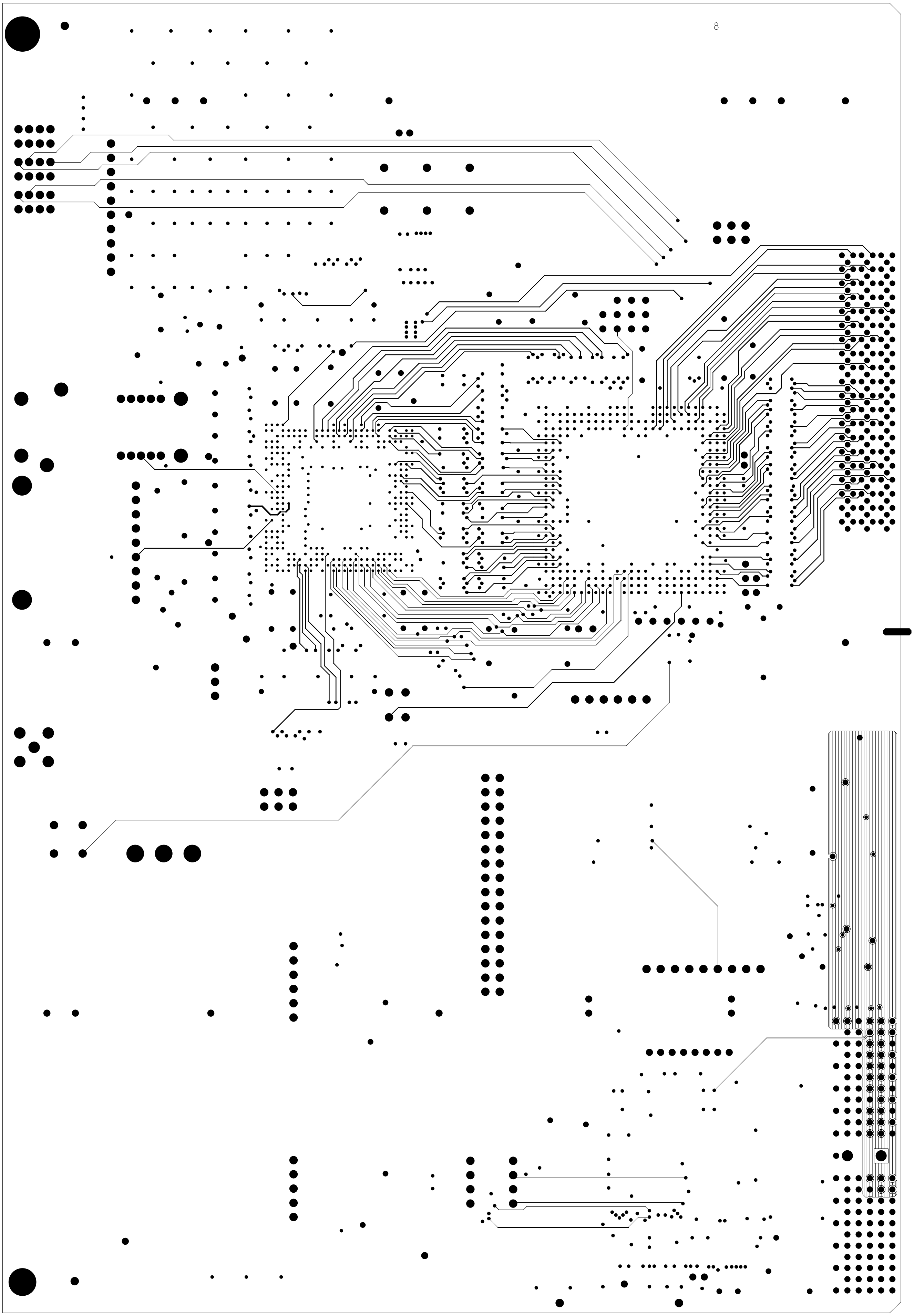


PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000



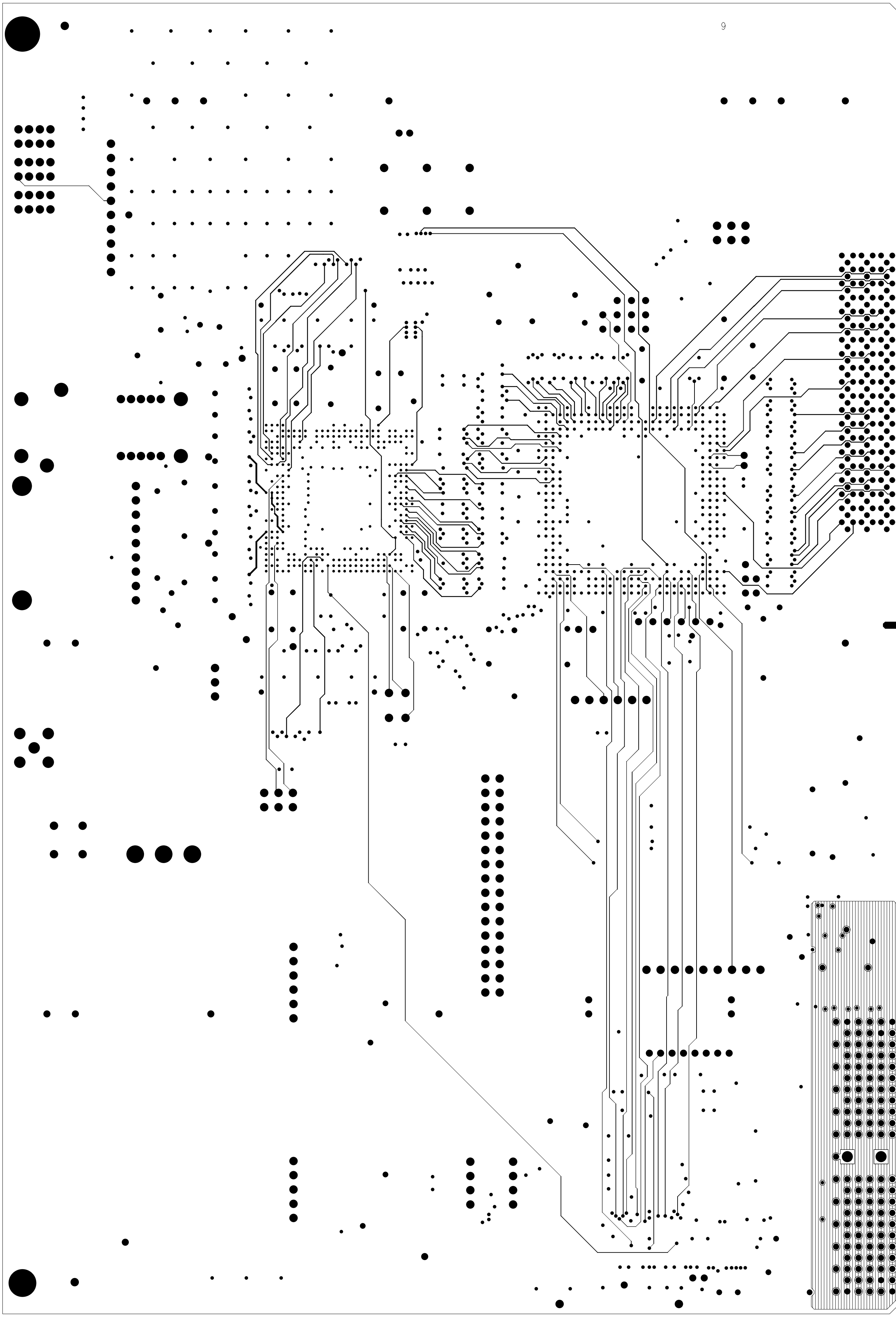
SIG2

PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000



SIG3

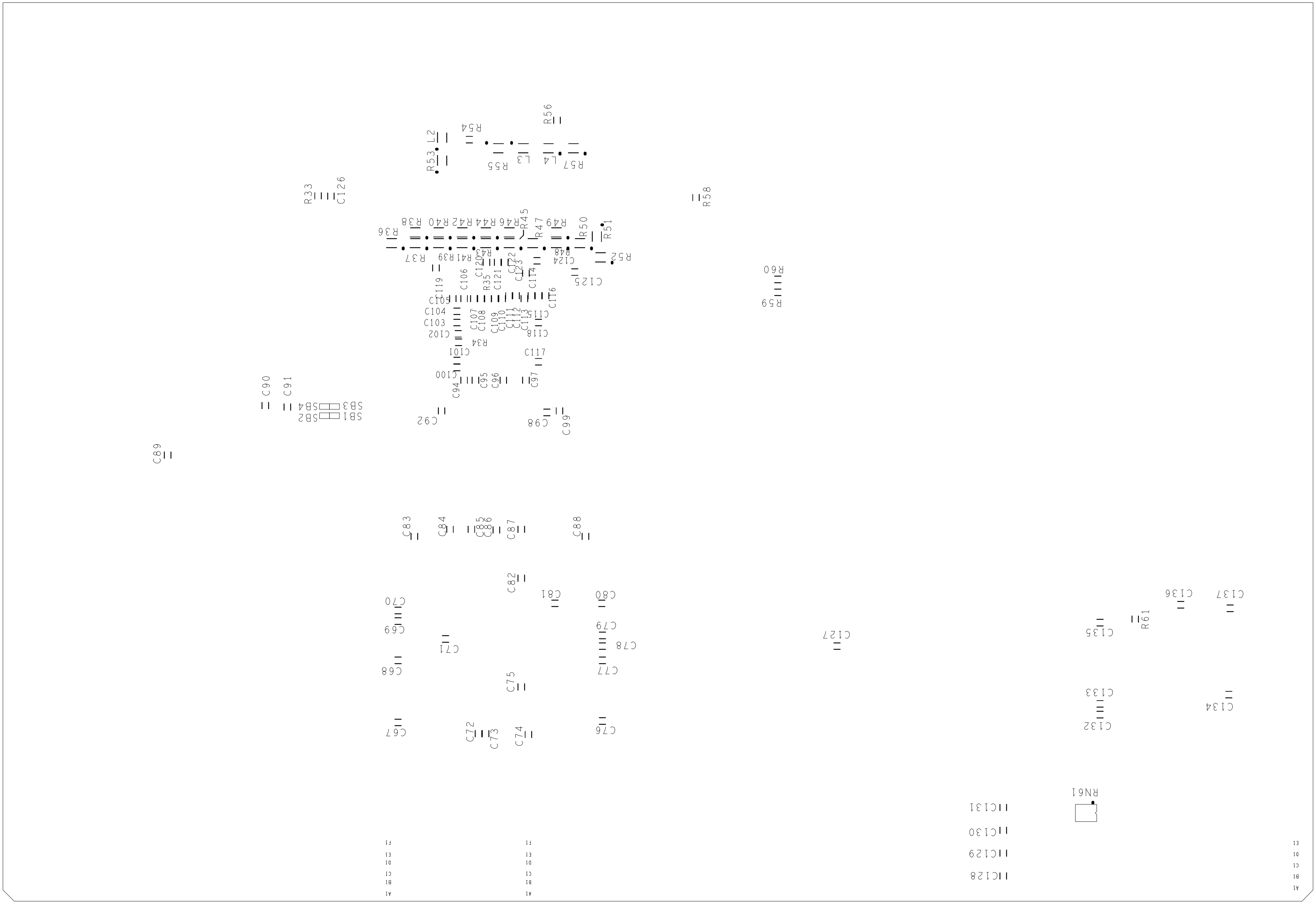
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000



SIG4

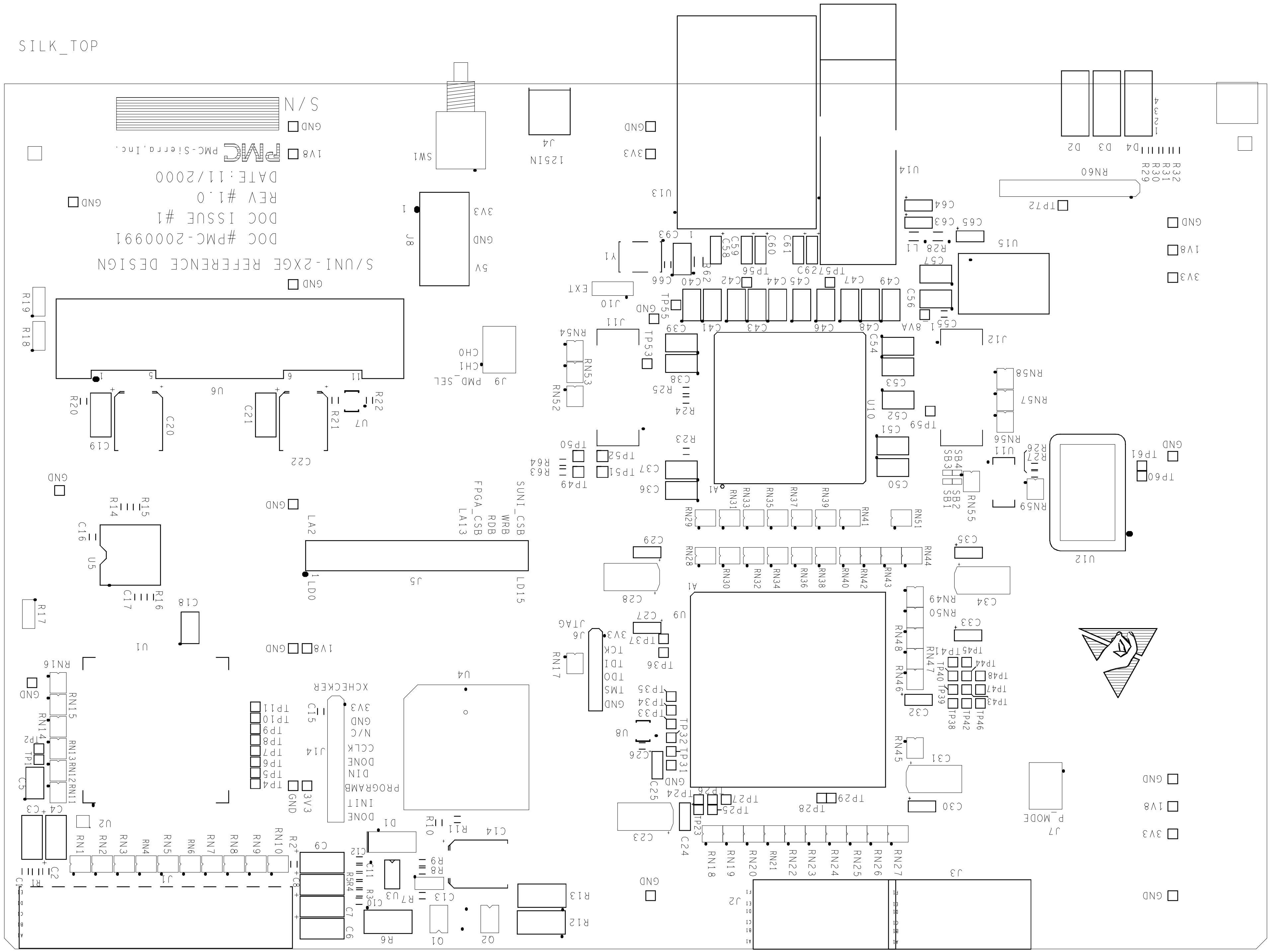
PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

SILK_BOTTOM

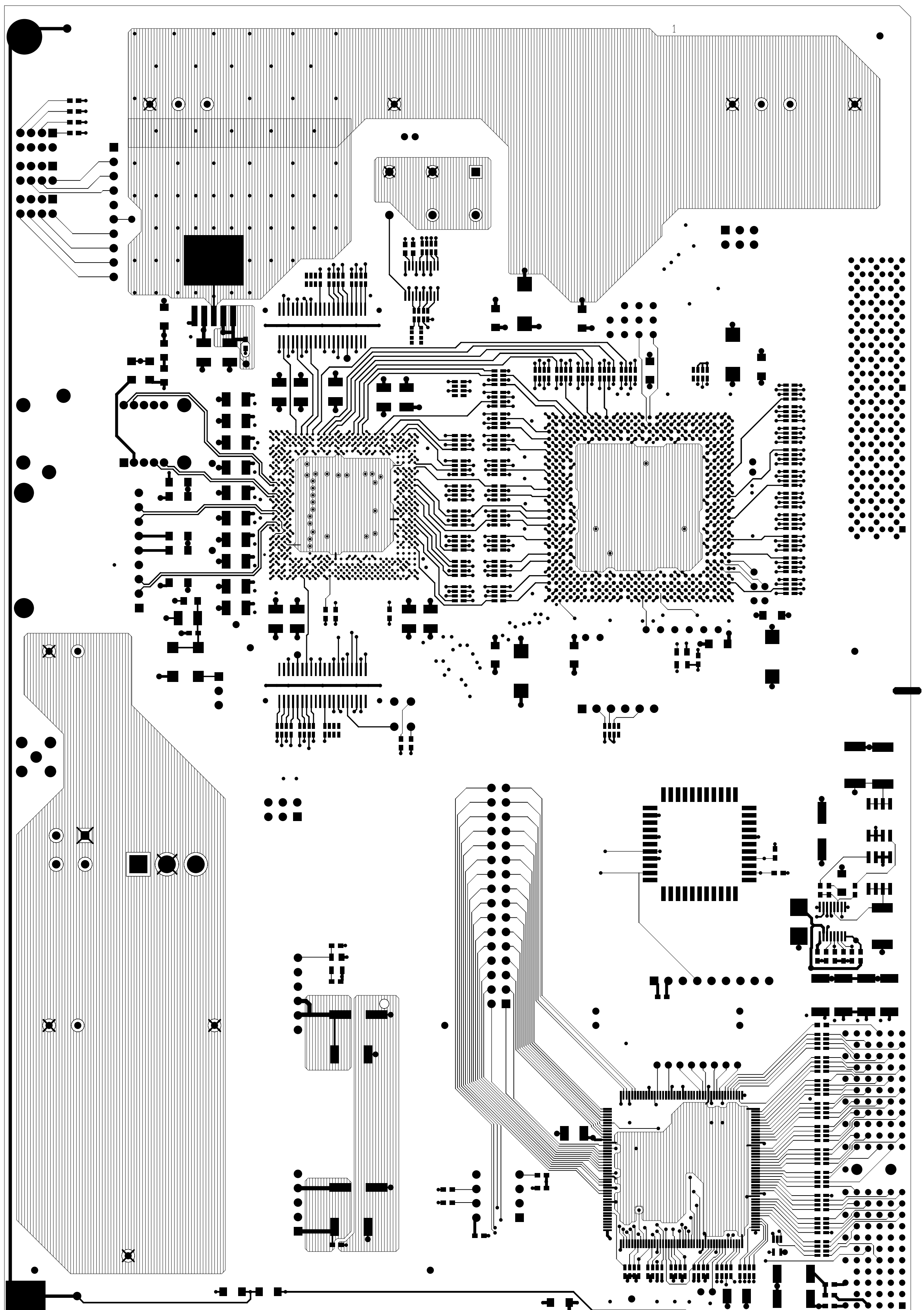


PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

SILK_TOP



PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000



PMC-SIERRA S/UNI-2XGE REFERENCE DESIGN REV. 1.0 2000

TOP LAYER

13 Bill of Materials (BOM) Revision 1

No.	Part Number	Manufacturer	RefDes	Description	Qty
1	PI49FCT3807DQ	PERICOM	U11	IC 3.3V 1:10 CMOS CLOCK DRIVER QSOP20 D GRADE	1
2	SN74AHC1G08DCKR	TI	U2	IC SINGLE 2-INPUT POSITIVE AND GATE	1
3	120673-1	AMP	J2, J3	Z-PACK 6 ROW HS3 BACKPLANE CONNECTOR, RIGHT ANGLE RECEPTACLE	2
4	ECU-V1H103KBV	PANASONIC	C11	CAP CERAMIC X7R 0603 50V 0.01UF	1
5	ECU-V1H473KBW	PANASONIC	C13	CAP CERAMIC X7R 1206 50V 0.047UF	1
6	ECJ-1VB1C104K	PANASONIC	C1, C2, C10, C12, C15-C17, C26, C55, C66-C92, C94-C137	CAP CERAMIC X7R 0603 16V 0.1UF	80
7	GRM42-2X5R106K10	MURATA	C5, C18, C36-C54, C56, C57, C93	CAP CERAMIC X5R 1210 10V 10UF	24
8	ECS-H1CC106R	PANASONIC	C3, C4, C6-C9	CAP TANCAPC 16V 20% 10UF	6
9	ECS-T0JY106R	PANASONIC	C24, C25, C27, C29, C30, C32, C33, C35	CAP TANCAPA 6.3V 20% 10UF	8
10	ECS-H1VC225R	PANASONIC	C19, C21	CAP TANCAPC 35V 20% 2.2UF	2
11	ECE-V1AA221P	PANASONIC	C14, C20, C22	CAP ELECTRO VA SMD 10V 20% 220UF	3
12	ECS-T0JY475R	PANASONIC	C58-C65	CAP TANCAPA 6.3V 20% 4.7UF	8
13	ECS-H0JD476R	PANASONIC	C23, C28, C31, C34	CAP TANCAPD 6.3V 20% 47UF	4
14	PZC36SAAN	SULLINS ELECTRONICS	J10	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	1
15	PZC36SAAN	SULLINS ELECTRONICS	J6	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	1
16	PZC36DAAN	SULLINS	J5	CONN HEADER 2 ROW 0.1"X0.1" 2X16	1
17	PZC36DAAN	SULLINS ELECTRONICS	J7, J9	CONN HEADER STRAIGHT 6POS MALE .1" DUAL ROW 3X2	2
18	DIGI-KEY S1011-36-ND	?	J14	100 MIL SPACING HEADER	1
19	QSE-020-01-F-D	SAMTEC	J11, J12	CONNECTOR, SMD 2ROW, 20 POSITION/ROW, WITH GND	2
20	ELJ-FD1R0KF	PANASONIC	L1-L4	INDUCTOR 1.0UH 10% TYPE FD 0805	4

21	IRF7413	INTERNATIONA L RECTIFIER	Q1, Q2	IC POWER MOSFET	2
22	LP3966ES-1.8	NATIONAL SEMI	U15	3A FAST ULTRA LOW DROPOUT LINEAR REGULATOR 1.8V TO263-5	1
23	LTC1643L1CGN	LINEAR TECHNOLOGY	U3	IC CPCI HOT SWAP CONTROLLER W/ 12V POWERGD DISABLED	1
24	MAX811TEUS-T	MAXIM	U8	IC 4 PIN UP VOLTAGE MONITOR WITH MANUAL RESET INPUT 3.08V SOT143	1
25	MAX812REUS-T	MAXIM	U7	IC VOLTAGE MONITOR WITH MANUAL RESET INPUT 2.63V SOT143	1
26	MOUNTING HOLE	N/A	M1	MOUNTING HOLE .150" DIA	1
27	614-93-308-31-012	MILL MAX	U5	SOCKET FOR PART# NM93CS66LEN	1
28	MB3100H-100.000MH Z	MMD	U12	100.000MHZ HCMOS OSCILLATOR PIN1-NC	1
29	EH2645TTS-125.000 M	ECLIPTEK	Y1	OSCILLATOR 125.000MHZ 3.3V [TOL= 50PPM] [TEMP= 0-70C] [DUTY= 5%]	1
30	DIGIKEY -- CKN4002-ND	?	SW1	RIGHT ANGLE PCB MOUNT SPST PUSH BUTTOM	1
31	PCI9030-AA60PI	PLX TECHNOLOGY	U1	IC 3.3V PCI TARGET INTERFACE(32-BIT, 33MHZ, PQFP PACKAGE)	1
32	ED120/3DS	ONSHORE TECHNOLOGY	J8	CONN TB 3 PIN	1
33	ERJ-6RQFR47V	PANASONIC	R41, R45, R50, R52	RES 0805 1/10W 1% .47 OHM	4
34	ERJ-6RQJR47V	PANASONIC	R62	RES 0805 1/10W 5% .47 OHM	1
35	ERJ-3GSY0R00V	PANASONIC	R34	RES 0603 1/16W 5% ZERO OHM	1
36	ERJ-6GEY0R00V	PANASONIC	R28, R53, R55, R57	RES 0805 1/10W 5% ZERO OHM	4
37	WSL2512-R01-1	VISHAY	R6, R12, R13	RES 2512 1W 1% 0.01 OHM	3
38	ERJ-6RQF1R0V	PANASONIC	R36, R37, R39, R43, R48	RES 0805 1/10W 1% 1.0 OHM	5
39	ERJ-3GSYJ122V	PANASONIC	R5	RES 0603 1/16W 5% 1.2K OHM	1
40	ERJ-3GSYJ100V	PANASONIC	R1, R2, R7, R9, R35	RES 0603 1/16W 5% 10 OHM	5
41	ERJ-3EKF1000V	PANASONIC	R8	RES 0603 1/16W 1% 100 OHM	1
42	ERJ-3GSYJ104V	PANASONIC	R22	RES 0603 1/16W 5% 100K OHM	1
43	ERJ-3GSYJ103V	PANASONIC	R33	RES 0603 1/16W 5% 10K OHM	1

44	ERJ-8GEYJ106V	PANASONIC	R17-R19	RES 1206 1/8W 5% 10M OHM	3
45	ERJ-3GSYJ151V	PANASONIC	R30	RES 0603 1/16W 5% 150 OHM	1
46	ERJ-3EKF1820V	PANASONIC	R20	RES 0603 1/16W 1% 182 OHM	1
47	ERJ-3GSYJ202V	PANASONIC	R3, R4	RES 0603 1/16W 5% 2.0K OHM	2
48	ERJ-6RQF3R3V	PANASONIC	R47	RES 0805 1/10W 1% 3.3 OHM	1
49	ERJ-3GSYJ330V	PANASONIC	R26, R27	RES 0603 1/16W 5% 33 OHM	2
50	ERJ-3GSYJ472V	PANASONIC	R10, R11, R14-R16, R21, R23-R25, R59-R61, R63, R64	RES 0603 1/16W 5% 4.7K OHM	14
51	ERJ-3EKF49R9V	PANASONIC	R58	RES 0603 1/16W 1% 49.9 OHM	1
52	ERJ-3GSYJ561V	PANASONIC	R31, R32	RES 0603 1/16W 5% 560 OHM	2
53	ERJ-3EKF63R4V	PANASONIC	R29	RES 0603 1/16W 1% 63.4 OHM	1
54	EXB-V8V100JV	PANASONIC	RN1-RN12	RES_ARRAY_4_SMD-10	12
55	EXB-V8V330JV	PANASONIC	RN18-RN44, RN46-RN59	RES_ARRAY_4_SMD-33	41
56	EXB-V8V472JV	PANASONIC	RN13-RN17, RN45, RN61	RES_ARRAY_4_SMD-4.7K	7
57	750101R200	CTS	RN60	BUSSED RESISTOR NETWORK 200 OHM SIP10	1
58	SIE501.8R	IPD CONVERTERS	U6	REGULATOR 5.0V TO 1.8V 6A, 100MV MAX RIPPLE CONVERTER	1
59	131-3701-341	JOHNSON COMPONENTS	J4	50 OHM RIGHT ANGLE BULKHEAD JACK RECEPTACLE	1
60	SSF-LXH5147LGD	LUMEX	D2-D4	LED QUAD GREEN HORIZONTAL	3
61	PM3386	PMC SIERRA	U10	IC DUAL GIGABIT ETHERNET CONTROLLER	1
62	V23818-K305-L57	INFINEON	U14	IC LC 2X5 GIGABIT ETHERNET TRANSCEIVER	1
63	V23826-K305-C353	INFINEON	U13	IC 1X9 AC COUPLED GIGABIT ETHERNET TRANSCEIVER	1
64	540-99-044-17-400 000	MILL MAX MANUFACTURING	U4	IC CONFIGURABLE OTP EPROM PLCC44 SOCKETED	1
65	XCV200E-6BG352C	XILINX	U9	IC HIGH DENSITY 1.8V VIRTEX FPGA (352BGA PACKAGE)	1
66	ZM4742A	DIODES INC	D1	ZENER DIODE 12.0V 5% 1.0W SURFACE MOUNT	1
67	352068-1	AMP	J1	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	1

Notes