# PM73487

# QRT

# DATASHEET Errata

**Released**

**Issue 7: February, 2002**

# Legal Information

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**PMC-1980618 (P3)**

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**U.S. Patent No. 5,557,607; 5,570,348; 5,583,861; 6,147,997; 6,151,301; 6,188,690B1**

**6,226,298B1; 6,134,218**

Relevant patent applications and other patents may also exist.

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# Revision History

| Issue No. | Issue Date | Details of Change |
|---|---|---|
| 1 | Sept. 1998 | Creation of document |
| 2 | Jan. 1999 | Added errata items |
| 3 | May 1999 | Added errata items 2.4, 2.5, 2.8, 3.6 – 3.8 |
| 4 | June 1999 | Aligns with Issue 3 Production Release Datasheet |
| 5 | July 1999 | Corrected typo in 3.2 |
| 6 | Aug. 2001 | Added patent award numbers |
| 7 | Feb. 2002 | Added errata items 2.2, 2.3, and 2.4<br>Added a patent number to errata item 2.1 |

# Table of Contents

# 1 Introduction

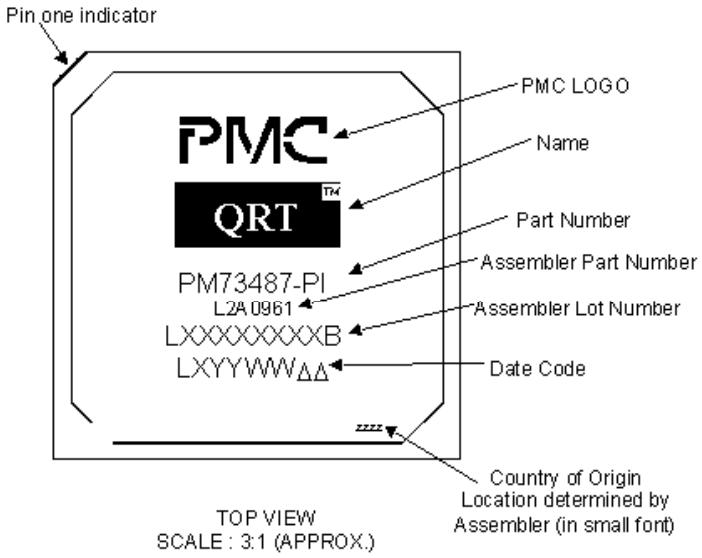
In this document:

- Section 2 lists documentation errors found in Issue 3 of the QRT Data Sheet (PMC-1980618).
- Section3 lists the known functional errata for Revision B of the PM73487 QRT.

## 1.1 Device Identification

The information contained in Section 2 relates to Revision B of the PM73487 QRT only. The device revision code is marked at the end of the Wafer Batch Code on the face of the device.

**Figure 1 PM73487 QRT Branding Format**




## 1.2 References

- Issue 3 of the QRT Data Sheet (PMC-1980618).

# 2 Documentation Deficiency List

This section lists the known documentation deficiencies for Issue 3 of the QRT Data Sheet (PMC-1980618) as of the publication date of this document.

For each *specific* deficiency, the location of the passage in question, the deficient text, and the replacement text are described. New text is shown in bold. Deleted text is shown as underlined.

For more *general* issues, a description of the nature of the error is given, along with a passage that correctly describes the concept or device function. Please report any documentation deficiencies not covered in this errata to PMC-Sierra.

## 2.1 Page 2 - US Patents

The PM73487 is protected by the following patents:

US patent 5,557,607

US patent 5,570,348

US patent 5,583,861

US patent 6,147,997

US patent 6,151,301

US patent 6,188,690B1

US patent 6,226,298B1

**US patent 6,134,218**

## 2.2 UTOPIA Level 2 Mode Description

The description of the UTOPIA Level 2 mode in the datasheet needs some clarification to emphasize that, in the Multi-PHY (MPHY) mode, the interface does not operate with any device with a bandwidth greater than an OC-3.

### 2.2.1 Location

The UTOPIA Level 2 Mode description is found in Section 3.2.2.7, Highest Bandwidth Device Support in UTOPIA Level 2 Mode.

### 2.2.2 Original Wording

The QRT UTOPIA Level-2 50 MHz interface was not designed to operate with any device possessing a bandwidth greater than that of an OC-3. For higher bandwidth requirements, the user must use the single-PHY UTOPIA Level-1 mode of operation.

### 2.2.3 Replacement Wording

The QRT UTOPIA Level-2 50 MHz **MPHY** interface was not designed to operate with any device possessing a bandwidth greater than that of an OC-3. For higher bandwidth requirements, the user must use the single-PHY UTOPIA **Level-2** mode of operation.

## 2.3 RX_DRAM_REGISTER and TX_DRAM_REGISTER Addresses

There is a typo in the addresses for the RX_DRAM_REGISTER and TX_DRAM_REGISTER in the datasheet.

### 2.3.1 Location

The addresses for the RX_DRAM_REGISTER and TX_DRAM_REGISTER are in the table under Section 9.1, External RAM Summary.

### 2.3.2 Original Wording

| Byte Address | Long Address | Name | Description |
|---|---|---|---|
| 800000h | 200000h | Address Lookup RAM (AL_RAM) | Contains the address lookup tables, linked lists, and multicast pointer FIFOs. |
| 1000000h | 400000h | Channel RAM (CH_RAM) | Contains the channel tables. |
| 1800000h | 600000h | AB_RAM | Contains the head and tail pointers for the receive channel queues. |
| 2000000h | 800000h | Receive Cell Buffer SDRAM/SGRAM (RX_DRAM_REGISTER) | Receive buffer SDRAM/SGRAM. |
| 3000000h | C00000h | Transmit Cell Buffers SDRAM/SGRAM (TX_DRAM_REGISTER) | Transmit buffer SDRAM/SGRAM. |

### 2.3.3 Replacement Wording

| Byte Address | Long Address | Name | Description |
|---|---|---|---|
| 800000h | 200000h | Address Lookup RAM (AL_RAM) | Contains the address lookup tables, linked lists, and multicast pointer FIFOs. |

| | | | |
|---|---|---|---|
| 1000000h | 400000h | Channel RAM (CH_RAM) | Contains the channel tables. |
| 1800000h | 600000h | AB_RAM | Contains the head and tail pointers for the receive channel queues. |
| **8000000h** | **2000000h** | Receive Cell Buffer SDRAM/SGRAM (RX_DRAM_REGISTER) | Receive buffer SDRAM/SGRAM. |
| **C000000h** | **3000000h** | Transmit Cell Buffers SDRAM/SGRAM (TX_DRAM_REGISTER) | Transmit buffer SDRAM/SGRAM. |

## 2.4 Latch-up Current and ESD Specification

There is no ESD and latch-up current specification under Section 5, Physical Characteristic, in the current QRT datasheet.

**The qualification data indicates that the QRT meets ±1 kV ESD and ±90 mA latch-up current.**

# 3 Device Functional Deficiency List

This section lists the known functional deficiencies for Revision B of the QRT as of the publication date of this document. For each deficiency, the known workaround and the operating constraints, with and without the workaround, are also described.

Please report any functional deficiencies not covered in this errata to PMC-Sierra.

## 3.1 AB_RAM Microprocessor Access Error

The AB_RAM stores the head and tail queue pointers. Normally, the microprocessor does not access this memory. So this anomaly has no consequence.

However, microprocessor accesses may be used in certain cases (e.g. as a SRAM diagnostic). For any microprocessor accesses, the data from an AB_RAM access may become 00h.

Software Work-around:

WRITE: Do not write 00h value to the AB_RAM. Always check the written value to ensure it is not 00h. If 00h is read back, retry the write.

READ: If the data read back is 00h, retry the read until a non-zero value is obtained. This is assuming 00h is always invalid.

## 3.2 Clock Tolerance Restrictions

For Stand-alone QRT operation and
Single-stage switching operation:

The SYSCLK and the SE_CLK need to be maintained in a specific ratio: 100 : 66.66.

That is, both clocks can be scaled together to different frequencies, but the ratio needs to be maintained. Normal crystal oscillator tolerances apply (+/- 500ps).

For Multi-stage switching operation:

A MNACK'ed cell may not be retransmitted from QRT's Port 3 (SDOUT(3)). The egress QRT will detect a sequence error and invoke resequencing error recovery.

Workaround: Operate SE_CLK within:

118/182 * SYSCLK < SE_CLK < 118/180 * SYCLK.

For ex., if SYSCLK = 100MHz, then:

64.83 Mhz < SE_CLK < 65.55 Mhz

Details on the conditions for the errata to occur in the Multi-stage switching operation:

Conditions required for cell drop to occur:

1) SE_CLK > 65.9 mhz when QRT sysclk=100 Mhz

2) A high priority cell has been MNACKed at QRT port 3 (cell is now occupying in one of the 2 SwEngine ping pong buffer)

3) The QEngine send a low priority cell into PORT 3's other ping pong buffer. In the same cell time, QEngine also sent a cell to the Port 2.

QEngine received inconsistent information about the MNACK'ed high priority cell and treated it as an ACK. The cell is then recycled.

## 3.3 TX and RX UTOPIA Buffer RAM Access Error

The TX and RX UTOPIA Buffer RAM's are 4 cell FIFOs which buffers cells to the TX and RX UTOPIA Interfaces. Read/write access is allowed to the RAMs by a microprocessor but this is only used in initial start up diagnostics. An access to the RAMs may return incorrect values.

It is not recommended for the microprocessor to access these RAM's.

## 3.4 Multicast operation restriction

The MC_LIST entry, offset 0x30, should not be used.

## 3.5 QRT generating incorrect BP_ACK signals due to stuck-at data lines

Normally, in the event of a stuck-at data line from the QSE to the QRT (i.e. at egress), the QRT should withhold backpressure to the QSE (i.e. not acknowledging cell receipt from the QSE).

Due to a metastability issue, in response to a stuck-at data line, the QRT may generate incorrect BPACKs (incorrect bit pattern). This will result in the QSE generating intermittent BP_ACK_FAIL_PRESENT (p.96) interrupts. Please note that the latched interrupt in the QSE (BP_ACK_FAIL_LATCH, p.96) will also be asserted.

## 3.6 Aliasing on microprocessor address bus causes interrupt latch clearing

During a microprocessor access into the QRT, if an address with "24" as least significant digits appears on the microprocessor address bus, the QUEUE_ENGINE_CONDITION_LATCH_BITS register (Reg. 0x2B), is cleared.

Workaround:

A) Ensure software does not read alias addresses when there is actual traffic flow. All alias addresses are listed below. Please note that all of the following addresses do not need to be accessed during traffic flow. They are only read for diagnostic purposes only, which should occur during initialization, before actual traffic flow.

The alias addresses are XXXXXX24 and XXXXXXAC

In the register section:

TX_DIR_STATE, 7C000024 -- Can be access via address 7C0000A4, therefore no aliasing.

In the TSC_RAM section:

TX_SCQ_STATE for all SCQs with SC=2 have alias addresses of 00400XX024 (XX = VO number)
TX_SCQ_TAIL/ TX_SCQ_OUT_FIFO_TAIL for SCQ/outfifo with SC=A have alias addresses of 00400XX0AC (XX = VO number)

In the RSC_RAM section:

All data structures with SC=9 and SC=2B

In the VO_RAM section:

TX_VO_CONFIG for VO=9, address is 00480024
TX_VO_STATE for VO=B, address is 004800AC
TX_VO_CELLS_PRES for VO=9, address is 00480124
TX_VO_SERVICE_STATE_0 for VO=B, address is 004801AC
TX_VO_SERVICE_STATE_1 for VO=9, address is 00480224
TX_SC_STATE for SC=5, address is 004802AC
TX_SC_MC_IN_FIFO_TAIL for SC=8, address is 00480324
TX_SC_MC_NEXT_HEADER_PTR for SC=D, address is 00483AC

In the CH_RAM:

TX_NEW_VPI_RESEQ_PTR for channel XXX6, address is 010XXXXAC

B) If any of the above alias addresses has to be read, before performing the read access, read the QUEUE_ENGINE_CONDITION_LATCH_BITS register first.

# Notes