PM5349

S/UNI-™ 155-QUAD

S/UNI-QUAD

S/UNI-QUAD REFERENCE DESIGN

REFERENCE DESIGN

ISSUE 3

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
3		Updated Filtering Recommendation (Section 7.2) to meet reference design schematics.
2	August 1999	Added Design Consideration Section and Updated the Schematics
1	August 1998	Document created.

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1 INTRODUCTION

The PM5349 S/UNI-QUAD standard product is a Quad SATURN User Network Interface with SONET/SDH processing, and ATM mapping functions at the STS-3c (STM-1) 155.52 Mbit/s rate. The S/UNI-QUAD is intended for use in equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interface (UNI), and ATM Network-Network Interfaces (NNI) interfaces. The S/UNI-QUAD may find application at either end of switch-to-switch links or switch-to-terminal links, both in public network (WAN) and private network (LAN) situations.

The S/UNI-QUAD reference design provides a physical interface implementation of a SONET/SDH line card for the ATM application. It provides four optical interfaces at OC-3 rates and a system side interface of 25MHz to 50MHz for a 16-bit wide bus.

2 FEATURES

- Provides four OC-3 rate 155.52 Mbits/s SONET/SDH Physical Layer Ports
- Provides a Utopia Level 2, 50 MHz, 16-bit ATM Multi-PHY System Interface
- Provides Dropside Loopback for Diagnostic Purposes
- Provides a software package for demonstration and evaluation of the S/UNI-QUAD reference board

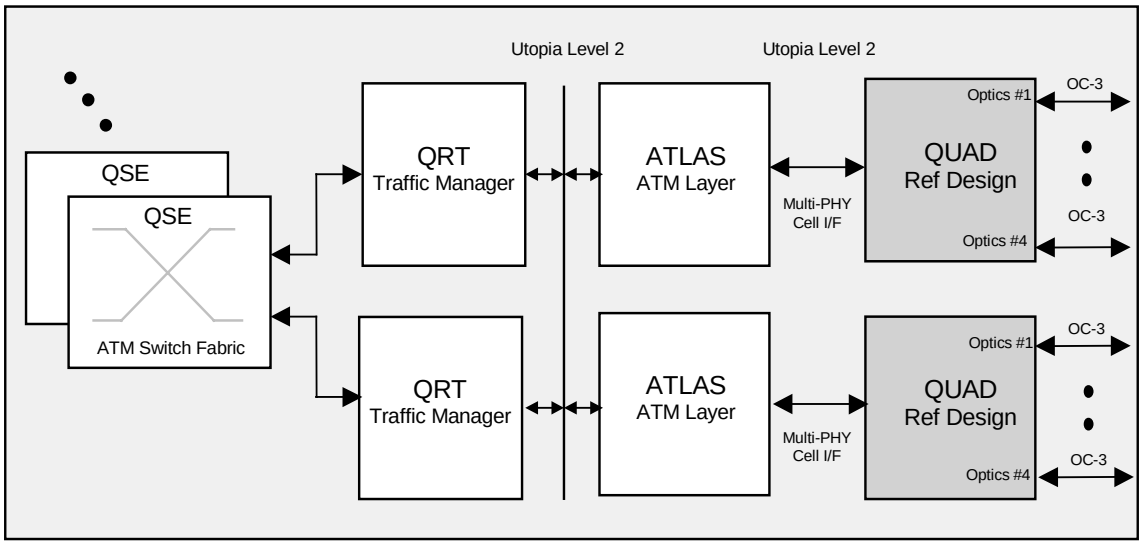
3 APPLICATIONS

The S/UNI-QUAD reference design demonstrates a physical interface implementation for ATM applications. The list below shows the networking equipment that can incorporate the S/UNI-QUAD device:

- WAN and Edge ATM switches physical Interface
- LAN switches and hubs physical Interface

The S/UNI-QUAD reference design interfaces to four OC-3 rate SONET/SDH signals on the line side. On the drop side, the S/UNI-QUAD interfaces directly to ATM layer processors and switching or adaptation functions using a Utopia Level 2 compliant synchronous FIFO style interface. Figure 1 shows an example of the S/UNI-QUAD reference design in a complete ATM switching design using PMC-Sierra's ATM chipsets.

Figure 1 : S/UNI-QUAD Ref Design with PMC-Sierra ATM Chipsets



4 DESIGN OVERVIEW

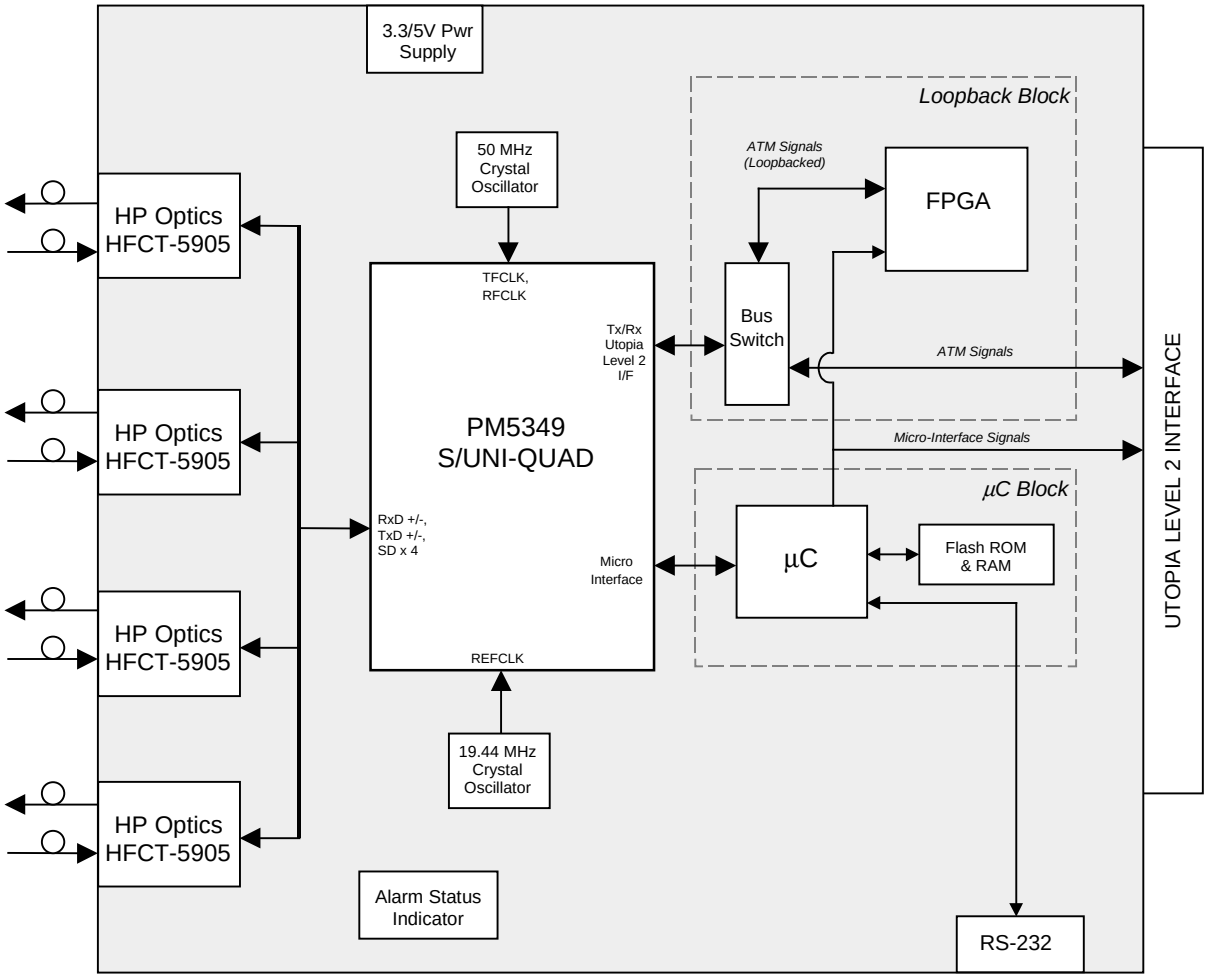
The S/UNI-QUAD reference design consists of a S/UNI-QUAD device and four optical transceivers in a four port optical physical interface for Asynchronous Transfer Mode (ATM) applications. The S/UNI-QUAD reference design contains an on-board microcontroller for accessing and controlling the S/UNI-QUAD device. The dropside Loopback function is provided by an on-board FPGA. The S/UNI-QUAD reference design is capable of a maximum bandwidth of approximately 622 Mbps and can be used as an ATM line card.

The S/UNI-QUAD reference design supports the Utopia level 2 ATM PHY to ATM Layer specification. Since the S/UNI-QUAD is a quad PHY chip, the PHY interface is configured as multi-PHY address polling at 50 MHz over a 16 bit bus.

The loopback feature allows the receive data to be looped back to the transmit stream at the drop side. This allows the evaluation of both the line side and drop side interface. An external Field Programmable Gate Array (FPGA) implements the loopback feature and provides a microprocessor interface to the 68322 microcontroller. This FPGA also provides transmit data reclocking. The FPGA reclocks the transmit data and control signals to meet the setup and hold times of the S/UNI-QUAD device.

The S/UNI-QUAD reference design can be run either as a stand-alone evaluation platform or interfaced to other S/UNI reference designs. As a stand-alone board, the S/UNI-QUAD reference design allows access to on-chip registers, and performs the system side loopback feature for the Utopia interface. When interfaced to other reference boards, cell generation functions are provided by these external boards for further demonstration and evaluation of the S/UNI-QUAD device.

5 BLOCK DIAGRAM

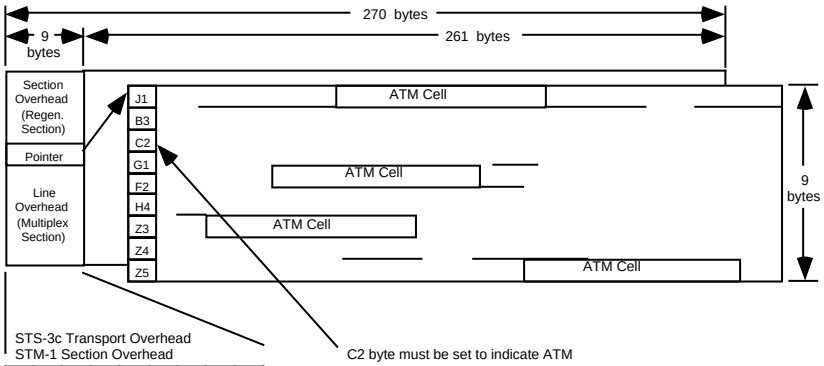


6 FUNCTIONAL DESCRIPTION

6.1 S/UNI-QUAD

The PM5349 S/UNI-QUAD SATURN User Network Interface is a monolithic integrated circuit that implements four channel SONET/SDH processing and ATM mapping functions at the STS-3c (STM-1) 155.52 Mbit/s rate. Figure 2 shows the overhead of a STS-3c frame.

Figure 2 : STS-3c Frame



A1	A1	A1	A2	A2	A2	J0	Z0	Z0
B1			E1			F1		
D1			D2			D3		
H1	H1	H1	H2	H2	H2	H3	H3	H3
B2	B2	B2	K1			K2		
D4			D5			D6		
D7			D8			D9		
D10			D11			D12		
S1	Z1	Z1	Z2	Z2	M1	E2		

The S/UNI-QUAD receives SONET/SDH streams using a bit serial interface, recovers the clock and data and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (M1, G1) are also accumulated. The S/UNI-QUAD interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope which carries the received ATM cell payload.

The S/UNI-QUAD frames to the ATM payload using cell delineation. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled. The ATM cells that are passed are written to a four cell FIFO buffer. The received cells are read from the FIFO using a 16 bit wide Utopia level 2 compliant datapath interface. Counts of

received ATM cell headers that are errored and uncorrectable and also those that are errored and correctable are accumulated independently for performance monitoring purposes.

The S/UNI-QUAD transmits SONET/SDH streams using a bit serial interface and formats section, line, and path overhead appropriately. It synthesizes the transmit clock from a lower frequency reference and performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line, and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (M1, G1) are also inserted. The S/UNI-QUAD generates the payload pointer (H1, H2) and inserts the synchronous payload envelope which carries the ATM cell payload. The S/UNI-QUAD also supports the insertion of a large variety of errors into the transmit stream, such as framing pattern errors, bit interleaved parity errors, and illegal pointers, which are useful for system diagnostics and tester applications.

ATM cells are written to an internal four cell FIFO using a generic 16-bit wide datapath interface. Idle/unassigned cells are automatically inserted when the internal FIFO contains less than one cell. The S/UNI-QUAD provides generation of the header check sequence and scrambles the payload of the ATM cells. Each of these transmit ATM cell processing functions can be enabled or bypassed.

No line rate clocks are required directly by the S/UNI-QUAD as it synthesizes the transmit clock and recovers the receive clock using a 19.44 MHz reference clock. Normally, the S/UNI-QUAD outputs only differential PECL line data (TXD+/-).

6.2 Optical Line Interface

The S/UNI-QUAD reference design provides four optical line interfaces at the 155.52 Mbit/s OC-3 rate. The line interface consists of four optical data links (ODL) and a termination scheme for the PECL signals into and out from the four S/UNI-QUAD transmit and receive signal pairs. The suggested termination scheme is discussed in the design consideration section.

In normal operation, the S/UNI-QUAD performs clock recovery and serial to parallel conversion on the incoming data stream. In a loss of signal condition, indicated on each of the four SD pins, the S/UNI-QUAD will squelch the receive data and the clock recovery unit and will switch to the reference clock (19.44MHz) to keep the recovered clock in range. This technique guarantees that the S/UNI-QUAD will generate an LOS indication when the ODL loses the incoming optical signal.

For this reference design, 3.3V ODL transceivers are used to reduce power consumption and match PECL level signals.

6.3 Microcontroller Block

The S/UNI-QUAD reference design uses a 32-bit Motorola 68332 microcontroller running at 16.7MHz as its on-board processor. The microcontroller block contains separate flash ROM and RAM for program data storage and run-time program execution, respectively. The S/UNI-QUAD registers are accessed through a 10-bit address and a 8-bit data bus microprocessor interface by the 68322.

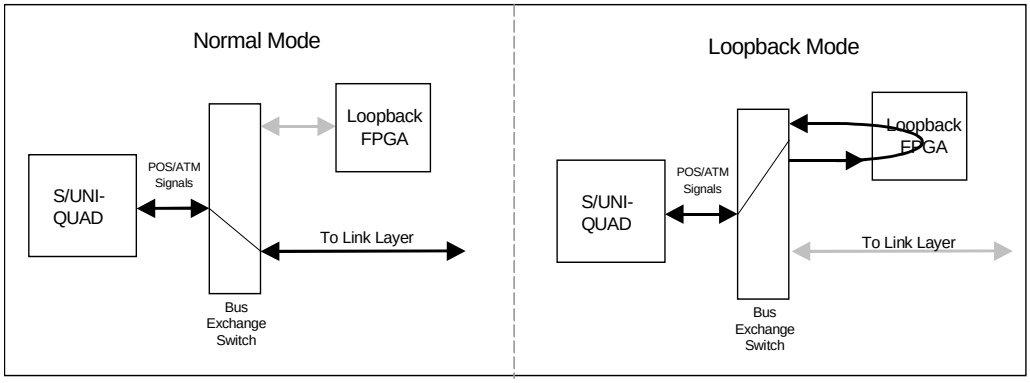
The microcontroller can be accessed through either the RS-232 port or the Background Debug Monitor (BDM) connector sitting on the reference board. The RS-232 port allows access to the serial port on the 68332.

The microcontroller also provides additional control to external adapter cards through the Utopia interface connector. This allows the microcontroller to access external devices.

6.4 System Side Loopback

The Loopback block consists of an FPGA and a bus exchange switch. The Bus exchange switch allows the S/UNI-QUAD's system side to be either connected to an external FPGA for loopback functionality or to a link layer interface board. The bus exchange switch adds minimum delay and presents low capacitance and impedance to the line. The loopback setup is shown in Figure 4 below.

Figure 3 : Loopback Diagram



In normal mode, the S/UNI-QUAD's Dropside data and control signals are connected to the system interface connector. In loopback mode, the receive data and control signals are input into and loopbacked out of the FPGA as transmit signals. The FPGA loopback supports multi-PHY direct status addressing mode with each PHY.

In loopback mode, the FPGA polls for receive cells available signals. The FPGA starts to receive and transmit cells only when PHY received data is available. This prevents the need for implementing a FIFO inside the FPGA.

6.5 External Connector

The S/UNI-QUAD reference design contains two Molex connectors for interfacing to a link layer or the HP ATM tester adapter card. The Molex connectors have been measured with a network analyzer and showed adequate results for running at 50MHz.

The first connector is used for microprocessor communication between the two microcontrollers on the S/UNI-QUAD reference and MB1503 boards. It supplies both 3.3V and 5V power supply to the S/UNI-QUAD board. It is also used for the FIFO clock signals for the Utopia interface. The second connector is used for interfacing Utopia data and control signals.

Table 1 : Interface Connector One

Pin Name	Type	Pin No.	Function
SCK	Input / Output	D17	Serial Clock. Clock for the microcontroller's QSPI module
MISO	Input / Output	D19	Master In Slave Out. Serial Data for the microcontroller's QSPI module.
MOSI	Input / Output	D18	Master Out Slave In. Serial Data for the microcontroller's QSPI module.
CS_MICRO	Input / Output	D20	Chip select for communication between the microcontrollers on the S/UNI-QUAD and link layer boards.

Pin Name	Type	Pin No.	Function
M/S_MICRO	Input	D21	Signal to indicate if the link layer board is the master or slave for the QSM bus. For M_MICRO = 0, the micro on the QUAD board is the master. For M_MICRO = 1, MB1503 acts as the master.
INTB	Output	D27	Interrupt signal from the S/UNI-QUAD device
RFCLK-	Output	D35	Negative differential receive clock signal. This signal, along with RFCLK+ comprise the differential RFCLK clock signal sent across the connector. RFCLK is to be used as a reference to sample RDAT.
RFCLK+	Output	D36	Positive differential receive clock signal. This signal, along with RFCLK- comprise the differential RFCLK clock signal sent across the connector. RFCLK is to be used as a reference to sample RDAT.
TFCLK+	Input	D39	Positive differential receive clock signal. This signal, along with TFCLK- comprise the differential TFCLK clock signal sent across the connector. TFCLK is used as a reference to sample TDAT.
TFCLK-	Input	D40	Negative differential receive clock signal. This signal, along with TFCLK+ comprise the differential TFCLK clock signal sent across the connector. TFCLK is used as a reference to sample TDAT.

Pin Name	Type	Pin No.	Function
NC	NC	A20 - A38, B17 - B30, C1 - C30, D1 - D16, D20 - D22, D28 - D34, D37, D38	Not Connected.
VCC1 (+5V)	Input	A1, A2, B1, B2	+ 5 Volt supply
+ 3.3V	Input	A3-A9, B3-B9,	+ 3.3 Volt supply
GND	Input	A10 - A19, B10 - B16, B31 - B40, C31 - C40	Ground

Table 2 : Interface Connector Two

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15]	Output	A1 D1 A2 D2 A3 D3 A4 D4 A5 D5 A6 D6 A7 D7 A8 D8	Receive Cell Data Bus This bus carries the ATM cell octets that are read from the selected receive FIFO.
RPRTY	Output	A9	Receive bus parity The receive parity signal indicates the parity of the RDAT bus.
DRCA[1] DRCA[2] DRCA[3] DRCA[4]	Output	A10 A11 A12 A13	Direct Receive Cell Available These signals indicate available cells to be transferred across the UTOPIA bus.
RADDR[0] RADDR[1] RADDR[2] RADDR[3] RADDR[4]	Input	D9 D10 D11 D12 D13	Receive PHY port address These signals are used to select the PHY port to be read from or polled.
RENB	Input	A14	Receive Multi-Phy Write Enable The RENB signal is an active low input which is used to initiate reads from the receive FIFOs.
RCA	Output	A15	Receive Multi-PHY Cell Available This signal indicates an available cell during receive PHY port polling
RSOC	Output	D14	Receive Start of Cell This signal marks the start of cell on the RDAT bus.

Pin Name	Type	Pin No.	Function
TENB	Input	A27	Transmit Multi-Phy Write Enable The TENB signal is an active low input which is used to initiate writes to the transmit FIFOs
TCA	Output	D26	Transmit cell available signal This signal is used to indicate available cell FIFO space by polled PHY ports.
TSOC	Input	A28	Transmit Start of Cell The transmit start of cell signal marks the start of cell on the TDAT bus.
TADDR[0] TADDR[1] TADDR[2] TADDR[3] TADDR[4]	INPUT	D27 D28 D29 D30 D31	Transmit Address The TADR[4:0] bus is used to select the port that is to be written to or being polled.
DTCA[1] DTCA[2] DTCA[3] DTCA[4]	Output	A29 A30 A31 A32	Direct Receive Cell Available These signals indicate available cells to be transferred across the UTOPIA.
TPRTY	INPUT	D32	Transmit bus parity The transmit parity signal indicates the parity of the TDAT bus.
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15]	INPUT	A40 D40 A39 D39 A38 D38 A37 D37 A36 D36 A35 D35 A34 D34 A33 D33	Transmit Cell Data Bus This bus carries the ATM cell octets that are written to the selected transmit FIFO.

7 DESIGN CONSIDERATIONS

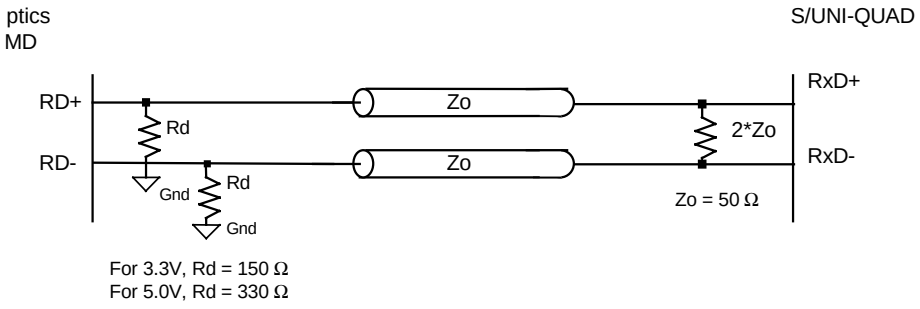
7.1 PECL INTERFACE

7.1.1 RECEIVE INPUTS

The S/UNI-QUAD's receive RxD+/- inputs are true differential PECL receivers. The receive signals are high-speed signals and must be properly terminated to reduce reflection. Unlike previous generation S/UNI products, the S/UNI-QUAD RxD+/- pair are not self-biased to the PECL Vbb level. Given that the RxD+/- inputs have wide common mode operating voltage, the receive inputs can be directly DC-coupled from the optics.

Most of the commercially avaliable optics on the market today provide PECL level RxD+/- outputs. The emitter on these PECL outputs need to be biased through a series resistor ground to provide adequate signal levels on the outputs. For 3.3V PECL drivers, a 150 Ohm series resistor is recommended. For 5V PECL drivers, a 330 Ohm series resistor is recommeded. The bias resistor location and value is shown in Figure 4. The RxD+/- differential signals require termination at the S/UNI-QUAD's input . With 50 ohm controlled impedence lines, a 100 ohm resistor connected across the RxD+/- pair can properly terminate the signal with minimum current draw.

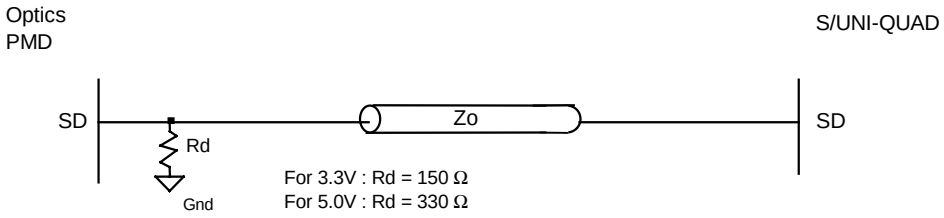
Figure 4 : Receive RxD+/- Interface



The SD detect input can also be DC-coupled from the SD output from an Optics. Similar to the optics RxD+/-'s outputs, the optic's SD output needs a emitter biasing resistor. Since SD is a relative slow signal, termination is not required at the S/UNI-QUAD. The SD input on the S/UNI-QUAD can also be supplied from

a TTL or CMOS source as long as the input signal level doesn't exceed the receiver voltage reference(3.3V or 5V).

Figure 5 : Receive SD Interface



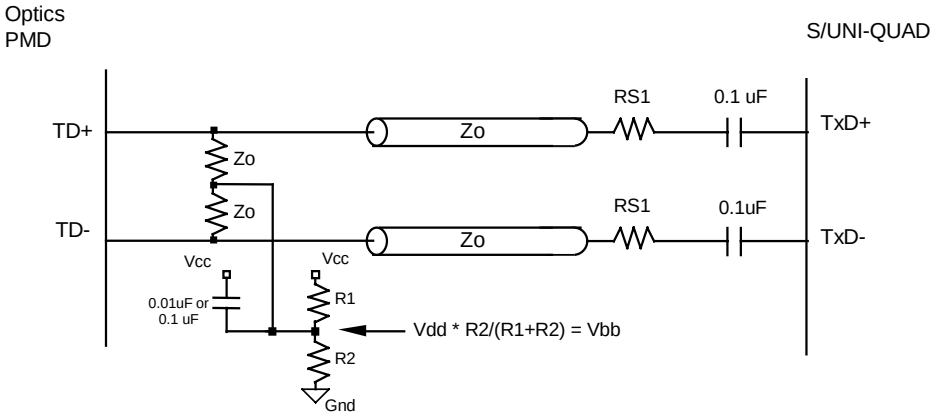
7.1.2 TRANSMIT OUTPUTS

The S/UNI-QUAD's transmit TxD+/- outputs are 3.3V CMOS rail to rail outputs. Since most of the optics have PECL level TxD+/- inputs, the TxD+/- signal from the S/UNI-QUAD needs to be converted to PECL level.

The PECL level conversion is done by first AC-coupling the TxD+/- outputs and attenuating the output voltage swing to PECL level. The PECL voltage swing is typically 800mV where as the S/UNI-QUAD outputs provide 3.3V swing. The 800mV swing can be attained by inserting a series resistor between the 50 Ohm impedance line and the AC-coupled resistor. The exact calculation of this attenuation resistor value is shown in figure 6. At the optics TxD+/- inputs, the 800mV voltage level needs to swing around the PECL bias point. For 5V PECL, the bias point is 3.7V and for 3.3V LVPECL, the bias point is 2.0V. A simple voltage divider network is shown in figure 6 for biasing the TxD+/- inputs to the PECL center point. The Vdd reference for the resistor and capacitor should be the same as the optics Vdd. Two 50 ohm resistors between the TxD+/- line and the PECL bias point provide the proper termination

The S/UNI-QUAD's transmitter and external termination circuity have been designed and throughly tested to meet Bellcore and ANSI jitter generation requirements. Using single-ended transmit output is not recommended due to duty-cycle distortion and poor jitter performance.

Figure 6 : Transmit TxD+/- Interface



Notes: Vpp is minimum input swing required by the optical PMD device.

Vbb is the switching threshold of the PMD device (typically Vdd - 1.3 volts)

Vpp is Voh - Vol (typically 800 mVolts)

Vpp = (Zo/((RS1+Rs)+Z0) * Vdd
- Vdd (S/UNI-QUAD's analog transmit power) 3.3V
- Zo (trace impedance) typically 50Ω
- Rs (TxD source impedance) typically 15-20Ω
- RS1 : ~ 158Ω

Vcc = Optics Power (5.0V or 3.3V)
For interfacing to 5.0V ODL, R1 : 237Ω , R2 : 698Ω
For interfacing to 3.3V ODL, R1 : 220Ω, R2: 330Ω

7.2 FILTERING AND DECOUPLING

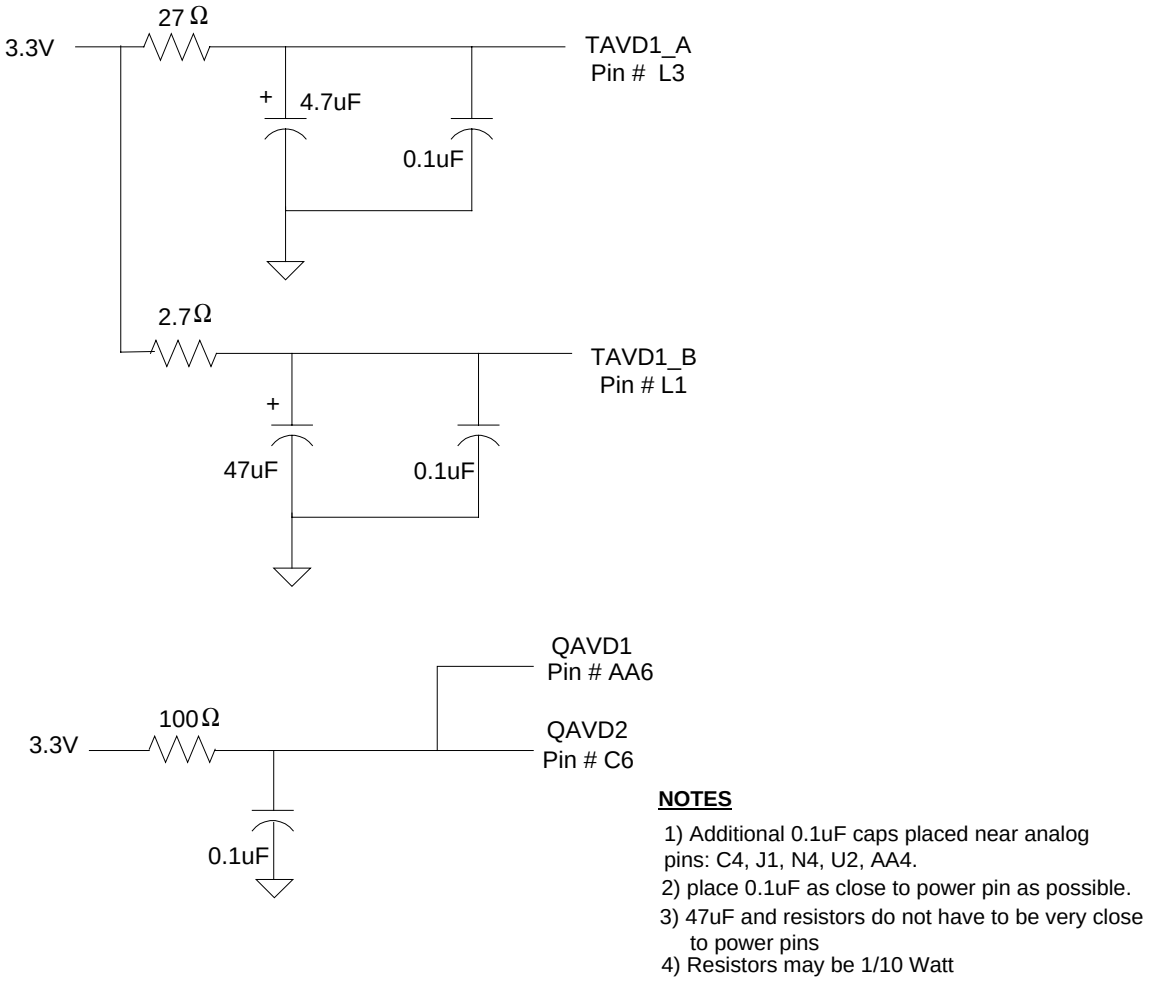
High speed analog circuitry is generally sensitive to any broadband noise on its power supply. The S/UNI-QUAD transmit CSU circuitry is sensitive to both low and high frequency noise. Care should be taken to reduce the noise at the CSU power pins, TAVD1_A and TAVD2_B. Since each board design can have different noise levels on the power rail, the transmit filtering circuit shown in figure 7 is recommended to ensure that the S/UNI-QUAD will be within 10% of its optimal jitter performance even when powered in a noisy environment.

~~The RC filtering circuitry provides a pole of around 1.25KHz for the purpose of filtering out low frequency noise. Additional 0.1µF decoupling capacitors should be placed near the following analog pins: C4, J1, N4, U2, and AA4. A single~~ The RC filtering circuitry provides a pole of around 1.25KHz for the purpose of filtering out low frequency noise. Additional 0.1µF decoupling capacitors should

be placed near the following analog pins: C4, J1, N4, U2, and AA4. A single uncut ground plane can be used for all S/UNI-QUAD board designs for both digital and analog circuitry. Ferrite beads are not recommended as a very small ferrite value will be needed to have a pole at the same location as an RC circuit and because LC circuity self-resonates at certain frequencies.

~~For the digital power pins, place 0.1µF caps near the following VDD pins: B2.~~ For the digital power pins, place 0.1µF caps near the following VDD pins: B2, B22, D9, D15, F20, J4, M20, R4, V20, Y9, Y15, AB2, and AB22.

Figure 7 : S/UNI Quad Analog Filtering~~S/UNI-Quad Analog Filtering~~



A 100 Ohm resistor should be added in series with a 0.1uF capacitor to ground on the quiet analog pins QAVD1 and QAVD2. This will protect the device from latching-up during power up.

7.3 UNUSED INPUT PINS AND CHANNEL

All unused input pins on the S/UNI-QUAD must be tied to their inactive state. If the inputs are left floating, noise can coupled into the CMOS gates and cause the S/UNI-QUAD device to malfunction. For tying an used input to 3.3V/5V, a 4.7K Ohm pull-up resistor can be used to prevent latchup during power up.

If one of the four channels is not being used, the analog differential inputs, RxD+/-, should be also be tied to ground to avoid chattering the receiver. For any unused channel, power still needs to be supplied to the analog power pins due to S/UNI-QUAD internal power structure.

7.4 JTAG PORT

When the JTAG is unused for boundary scan, the TRSTB on the S/UNI-QUAD should be tied to RSTB. This will reset the JTAG port as the same time as system reset. TMS, TCK, and TDI should all be tied high. In addition, TCK can be optionally tied to a free-running clock to ensure that the JTAG port logic is continuously put back to the correct initial state.

7.5 ROUTING

Routing is based on the design considerations as well as manufacturability. Several suggestions are listed below:

- Allow at least 10 mil clearance between vias, traces, and pads to prevent shorts and reduce crosstalk. If possible, allow 20 mil or more clearance around vias as manufacturers may have minimum clearance requirements.
- The differential signal pairs should be of equal length so that both signals arrive at the inputs at the same time. They should also run parallel and close to one another for as long as possible so that noise will couple onto both lines and become common mode noise which is ignored by the differential inputs.
- All power and ground traces should be made as wide as possible to provide low impedance paths for the supply current as well as to allow quick noise dissipation.
- Since vias have an impedance, avoid them where possible, especially on critical traces such as TXD± and RXD±. Also where decoupling is critical, try to place capacitors at the pins (component side) and not have vias in series with the capacitors.

8 IMPLEMENTATION DESCRIPTION

The S/UNI-QUAD reference design schematics were captured using Cadence software, Concept Schematics Capture Tool.

8.1 ROOT DRAWING, Sheet 1

This sheet provides an overview of the major functional blocks of the S/UNI-QUAD schematics. It shows interconnections between the QUAD_BLOCK, LOOPBACK_BLOCK, MICRO_BLOCK, SYS_INTEFACE, and OPTICS_BLOCK.

8.2 QUAD_BLOCK, Sheet 2 & 3

The QUAD_BLOCK shows the S/UNI-QUAD's signals and the power circuitry. Series resistors are used to source terminate the Utopia bus lines. The 51 Ohm termination resistors combined with the output impedance of the Utopia pads matches the impedance of the trace at 75 Ohms.

Four LEDs are provided to display alarm status from each of the four channels in the S/UNI-QUAD. A 1K Ohm resistor is also placed in series to limit the Vbias current to prevent Vbias latchup.

For analog power, RC filtering is provided for the transmit analog power pins as recommended in the design consideration. ~~Refer to Section 7.2 for additional details on decoupling recommendations.~~ Refer to Section 7.2 for additional details on decoupling recommendations.

8.3 LOOPBACK_BLOCK, Sheet 4 & 5

These sheets show the loopback function implemented for the QUAD's Utopia/ Level 2 interface signals. P15C16212 bus exchange switches are connected to Utopia signals from and to both the S/UNI-QUAD and the loopback FPGA. These bus switches are controlled by the loopback enable, LB_EN, signal. When in loopback, the signals driving the board connector are tied low by the resistor arrays connected through the bus switches.

The 74FCT807 3.3V clock driver supplies receive clocks to both the S/UNI-QUAD and the board connector for the ATM/POS layer devices. The transmit clock is supplied from the board connector during regular mode. When in loopback mode, both the transmit and receive clocks are supplied by the 74FCT807 clock driver. The Xilinx XC4020XL FPGA has 3.3V outputs to meet with the Utopia interface.

8.4 SYS_INTERFACE, Sheet 6 & 7

The SYS_INTERFACE block contains the board connectors and the power supply circuitry. On Sheet 6, two MOLEX 160 pin connectors are shown. Balun transformers are used to transform differential transmit and receive clock signals to a single-ended signal for the S/UNI-QUAD.

Sheet 6 shows power to the reference board may be supplied either from an external power supply or through the board connectors. Solder bridges are used to select the desired power source. Fuses and transils are provided to protect the board from over-voltage and over-current.

8.5 MICRO_BLOCK, Sheet 8

The MICRO_BLOCK sheet shows the 68322 microcontroller and its external circuitry. The 68322 operates at 16.337 MHz using a 32.768MHz crystal. 1 MB (128K x 8) Flash and SRAM are provided for program storage and run-time execution. The BDM header allows the microcontroller to run in background debug mode for downloading the program to the FLASH and debugging purposes. The MC33064 low voltage sensing circuit puts the 68322 in reset mode when the voltage supply drops below 4.5V.

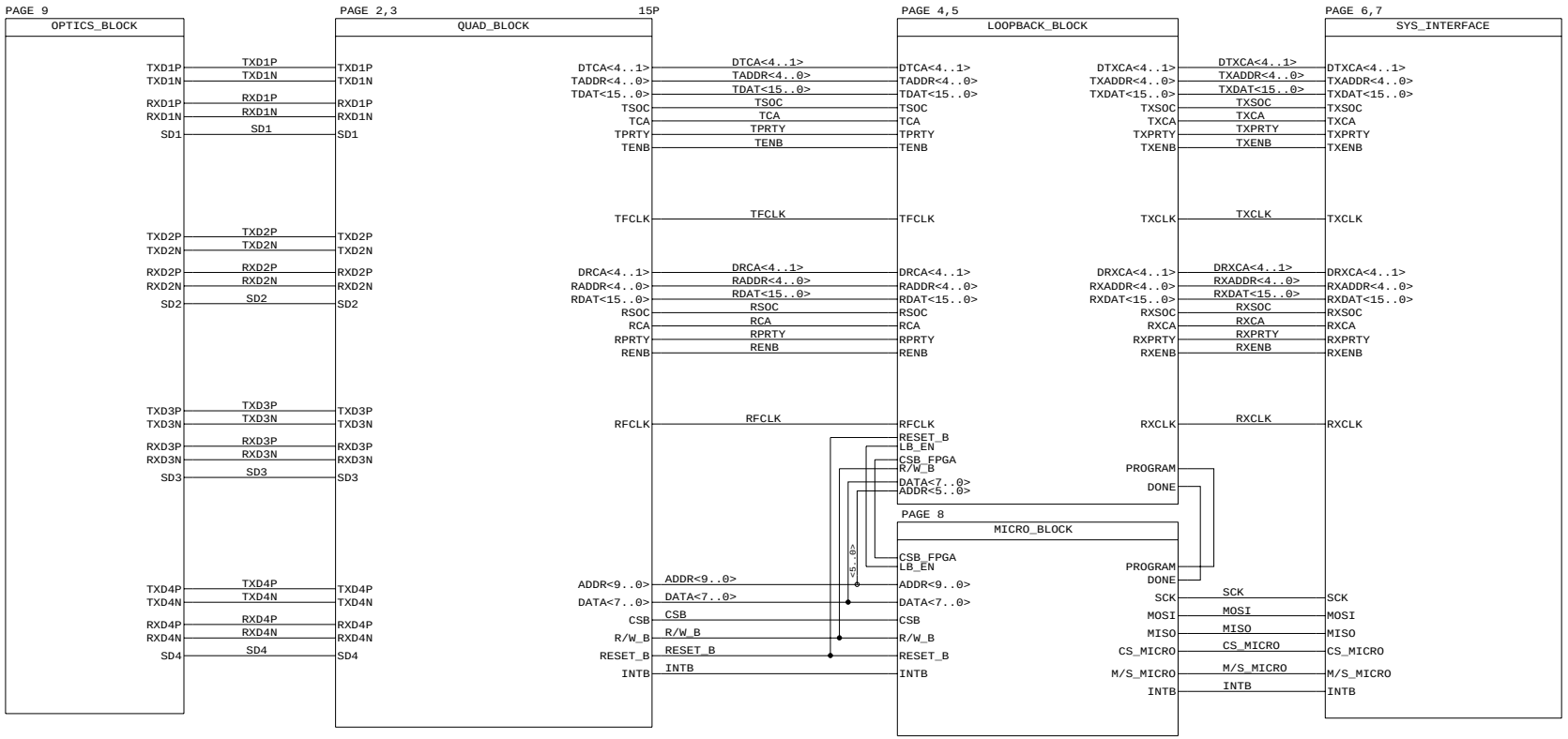
8.6 OPTICS_BLOCK, Sheet 9

This sheet shows the four Optical Data Links (ODLs) that provide the optical to electrical (O/E) function for the S/UNI-QUAD device. The PECL signals run on 50 Ohm controlled impedance signal lines and are properly terminated at the ODL and at the S/UNI-QUAD device.

The S/UNI-QUAD device interfaces to four HP HFCT-5905 Singlemode Fiber Transceivers. The HFCT-5905 can also be replaced with HFBR-5905 Multimode from HP. The HFBR-5905 transceivers are in a 2x5 DIP package with a MT-RJ connector interface. The smaller footprint MT-RJ interface allows higher optical port density on a typical ATM line card.

9 SCHEMATICS

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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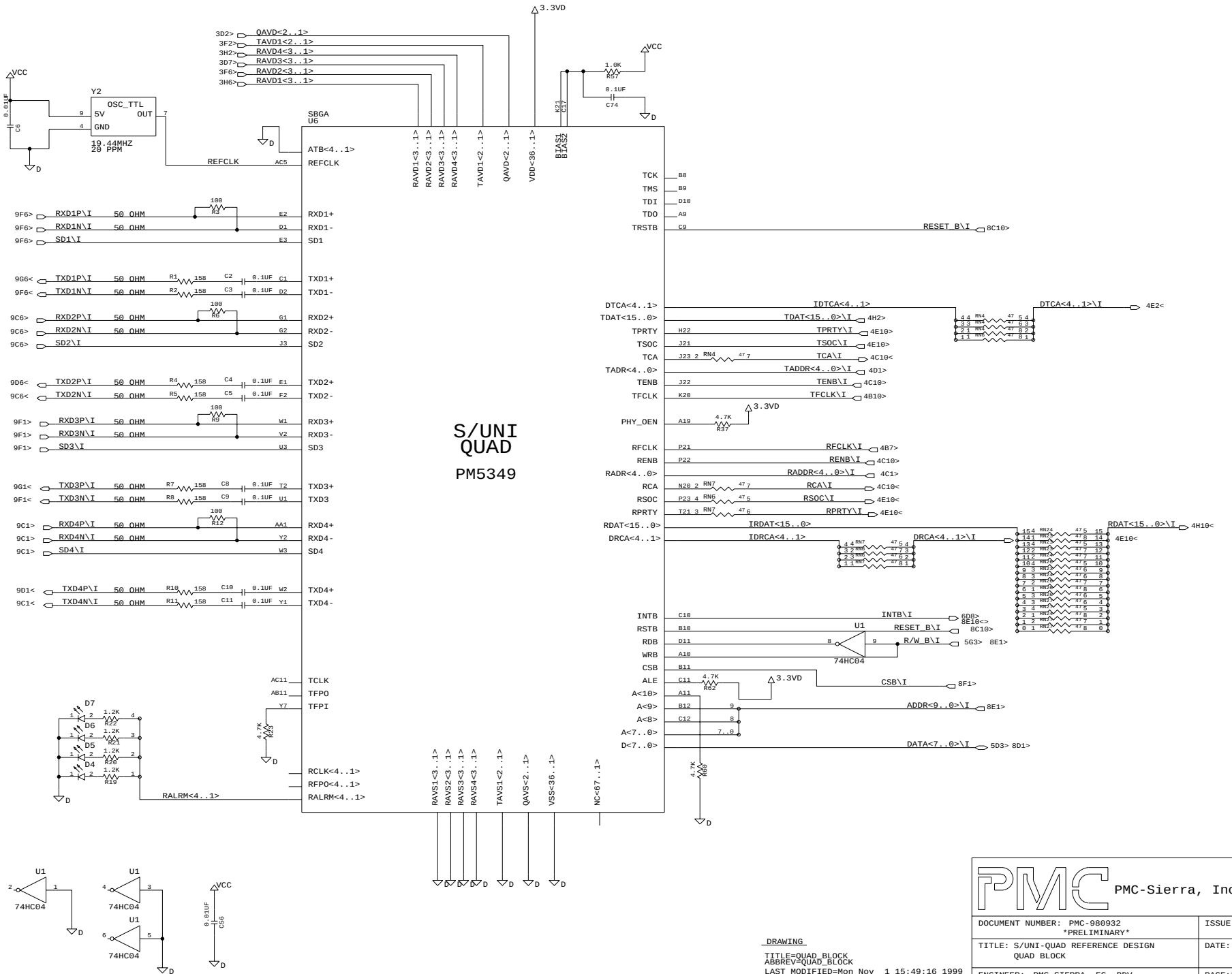
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980932 *PRELIMINARY*	ISSUE: 2.0
TITLE: S/UNI-QUAD REFERENCE DESIGN ROOT DRAWING	DATE: 99/08/04
ENGINEER: PMC-SIERRA EC BDV	PAGE:1 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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ENGINEER: PMC-SIERRA EC BDV	PAGE:2 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

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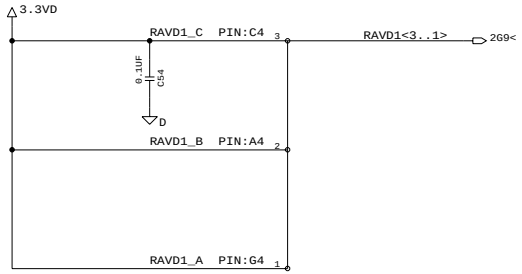

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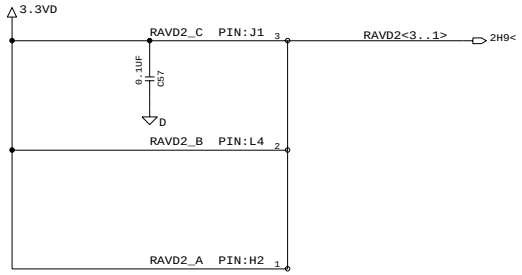

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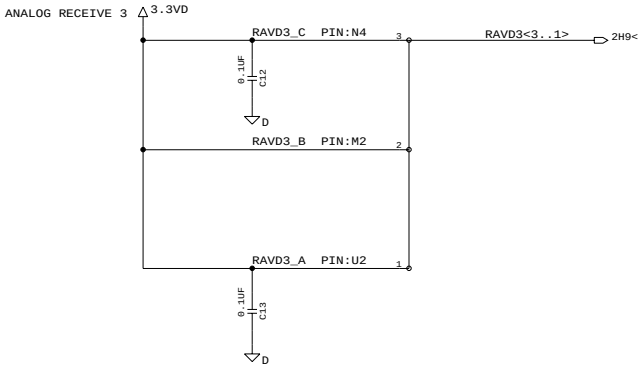
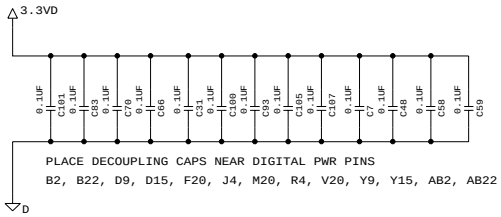
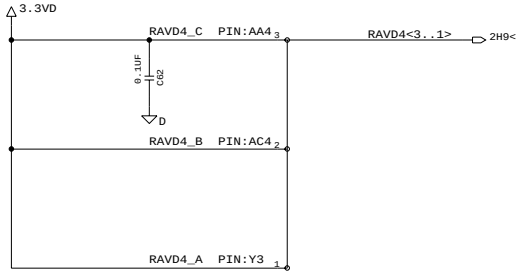




PLACE DECOUPLING CAPS NEAR DIGITAL PWR PINS
B2, B22, D9, D15, F20, J4, M20, R4, V20, Y9, Y15, AB2, AB22

ANALOG RECEIVE 4



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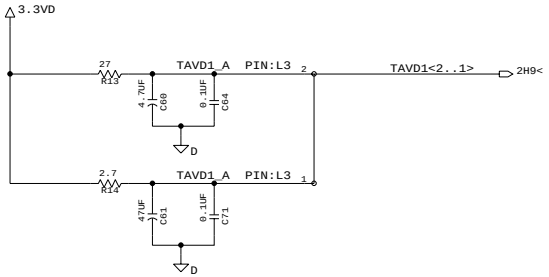

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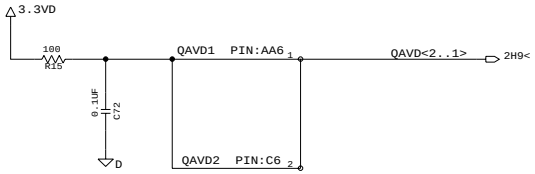

NOTES

PLACE 0.1UF CAPS AS CLOSE TO POWER PINS AS POSSIBLE.

47UF AND 4.7UF CAPACITORS ARE 6.3V TANTALUMS

TANTALUM CAPS AND RESISTORS (ON TAVD PINS) DO NOT NEED TO BE PLACED CLOSE TO POWER PINS

RESISTORS CAN BE 1/10 WATT

SINGLE GROUND PLANE RECOMMENDED

DRAWING

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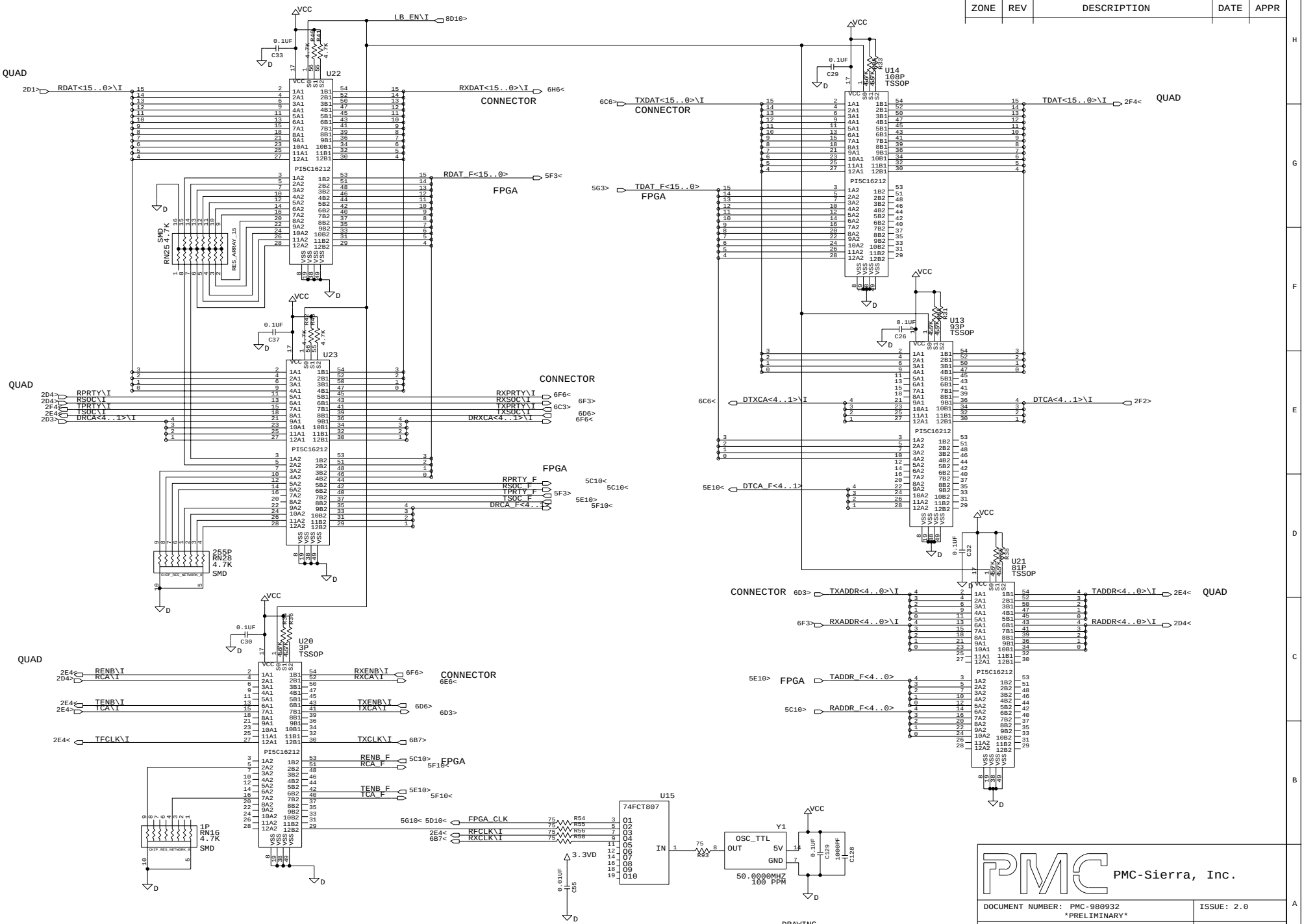
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980932 *PRELIMINARY*	ISSUE: 2.0
TITLE: S/UNI-QUAD REFERENCE DESIGN QUAD BLOCK	DATE: 99/08/04
ENGINEER: PMC-SIERRA EC BDV	PAGE:3 OF 9


REVISIONS
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U23
U14 108P TSSOP
U13 93P TSSOP
U21 81P TSSOP
U20 3P TSSOP
U15 74FCT807
PI5C16212
CONNECTOR
FPGA
LB_EN\I
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RXDAT<15..0>\I
RDAT_F<15..0>
TXDAT<15..0>\I
TDAT<15..0>\I
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TCA\I
TFCLK\I
RXENB\I
RXCA\I
TXENB\I
TXCA\I
TXCLK\I
RENB_F
RCA_F
TENB_F
TCA_F
FPGA_CLK
RFCLK\I
RXCLK\I
255P RN28 4.7K SMD
1P RN16 4.7K SMD
SMD RN25 4.7K
OSC_TTL
50.0000MHZ 100 PPM
3.3VD
PMC-Sierra, Inc.
DOCUMENT NUMBER: PMC-980932 *PRELIMINARY*
ISSUE: 2.0
TITLE: S/UNI-QUAD REFERENCE DESIGN LOOPBACK BLOCK
DATE: 99/08/04
ENGINEER: PMC-SIERRA EC BDV
PAGE:4 OF 9
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REVISIONS				
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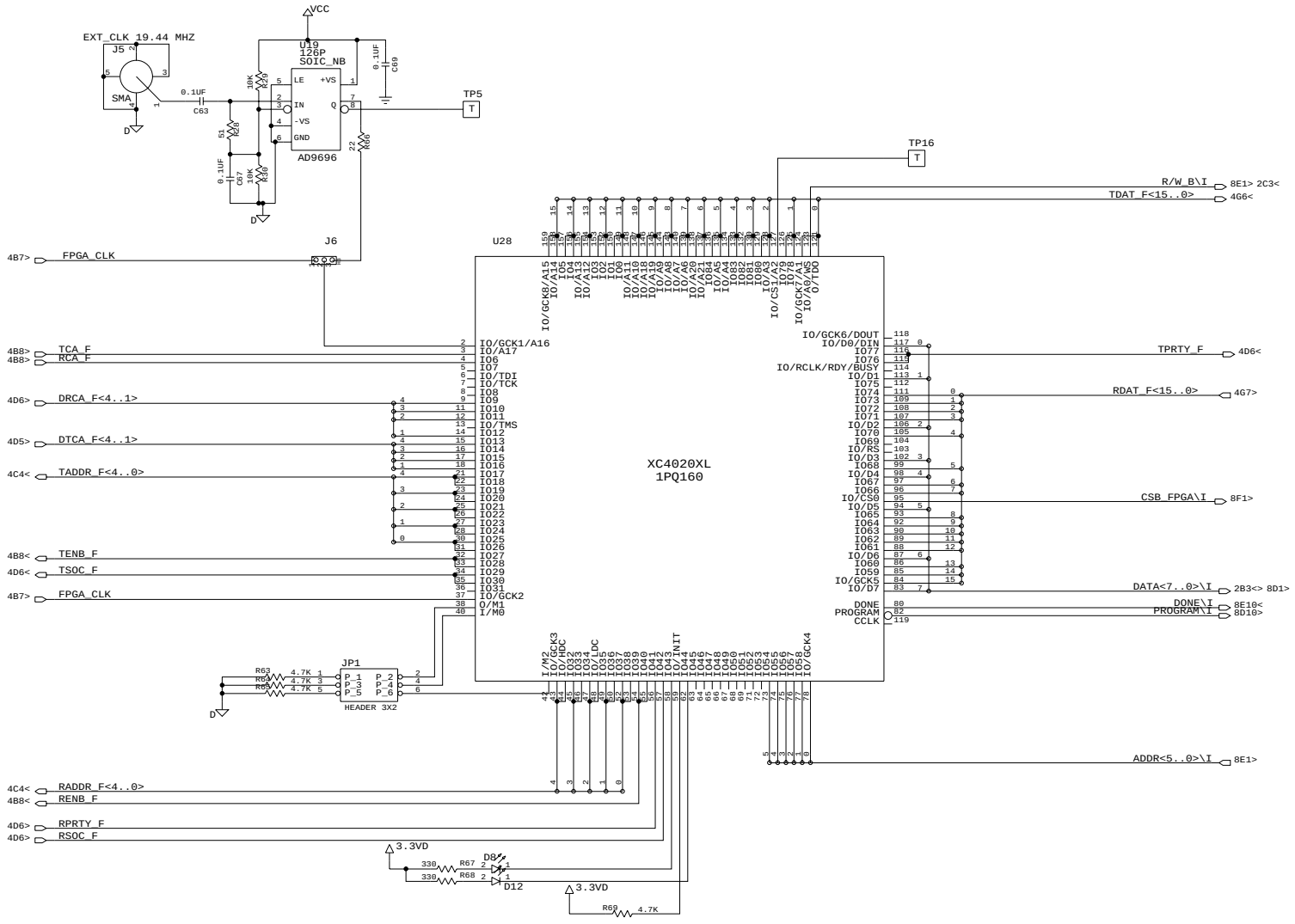

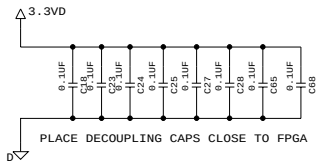

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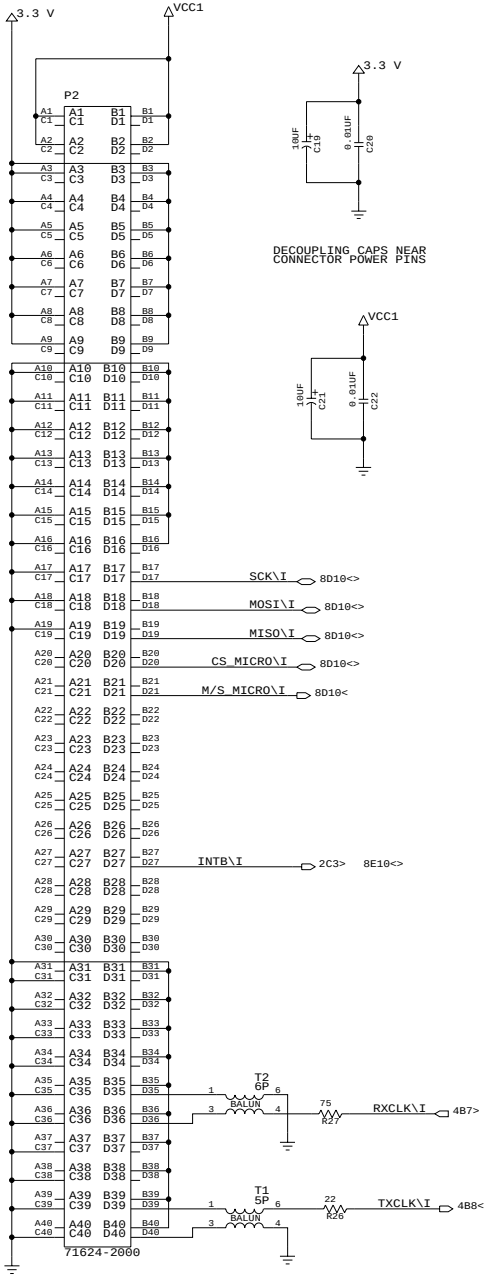
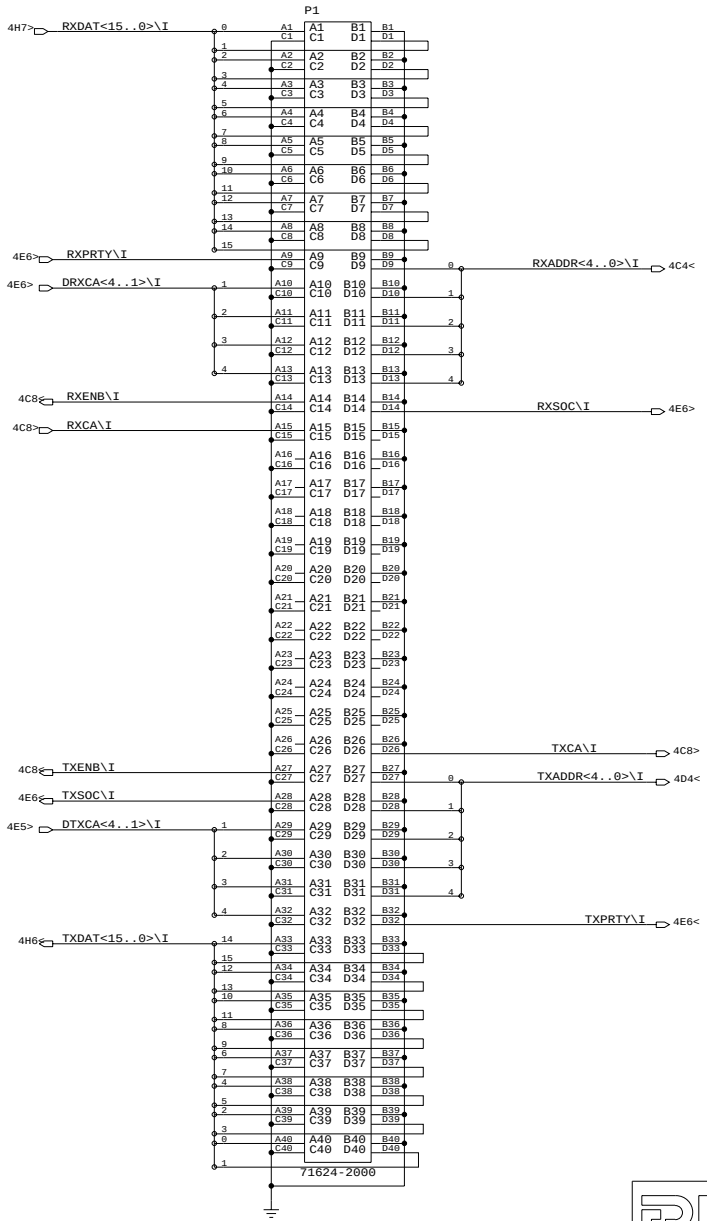
DOCUMENT NUMBER: PMC-980932 *PRELIMINARY*	ISSUE: 2.0
TITLE: S/UNI-QUAD REFERENCE DESIGN LOOPBACK BLOCK	DATE: 99/08/04
ENGINEER: PMC-SIERRA EC BDV	PAGE:5 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





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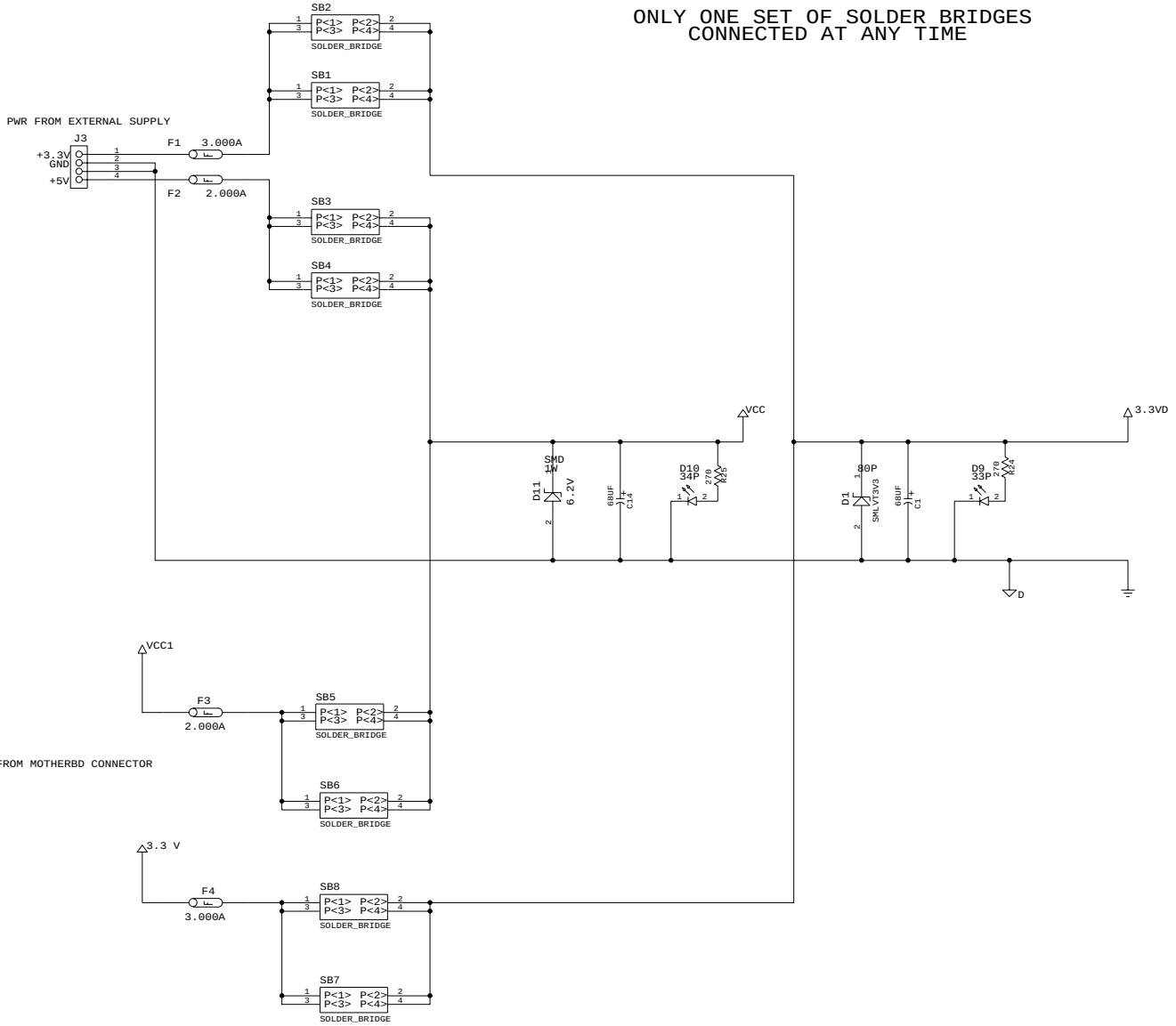
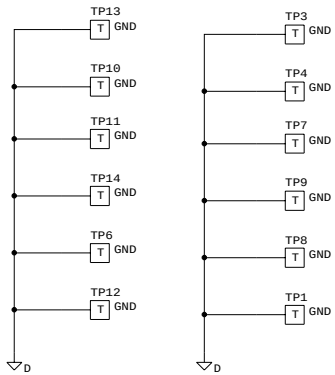
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980932 *PRELIMINARY*	ISSUE: 2.0
TITLE: S/UNI-QUAD REFERENCE DESIGN SYSTEM INTERFACE	DATE: 99/08/04
ENGINEER: PMC-SIERRA EC BDV	PAGE:6 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

ONLY ONE SET OF SOLDER BRIDGES
CONNECTED AT ANY TIME





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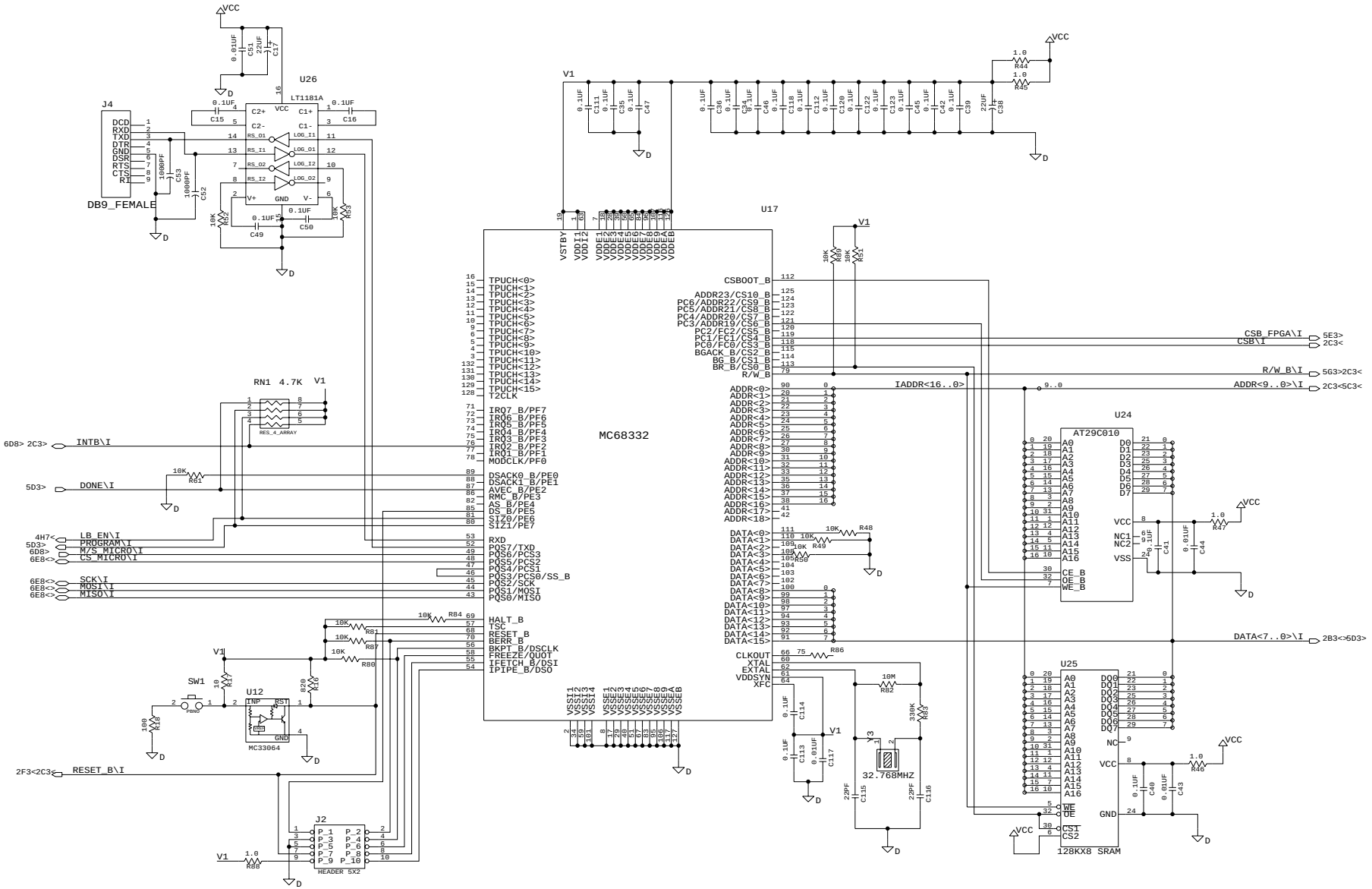
TITLE: S/UNI-QUAD REFERENCE DESIGN SYSTEM INTERFACE	DATE: 99/08/04
ENGINEER: PMC-SIERRA EC BDV	PAGE:7 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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ENGINEER: PMC-SIERRA EC BDV	PAGE:8 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

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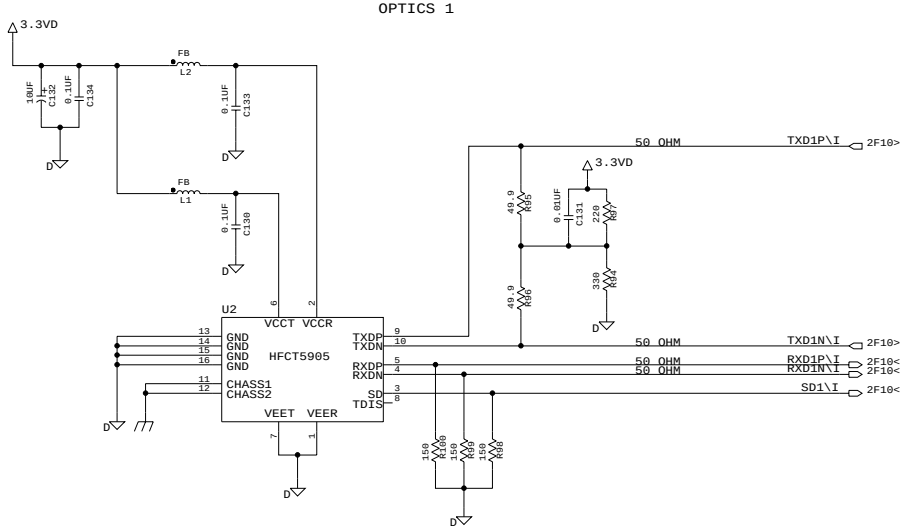

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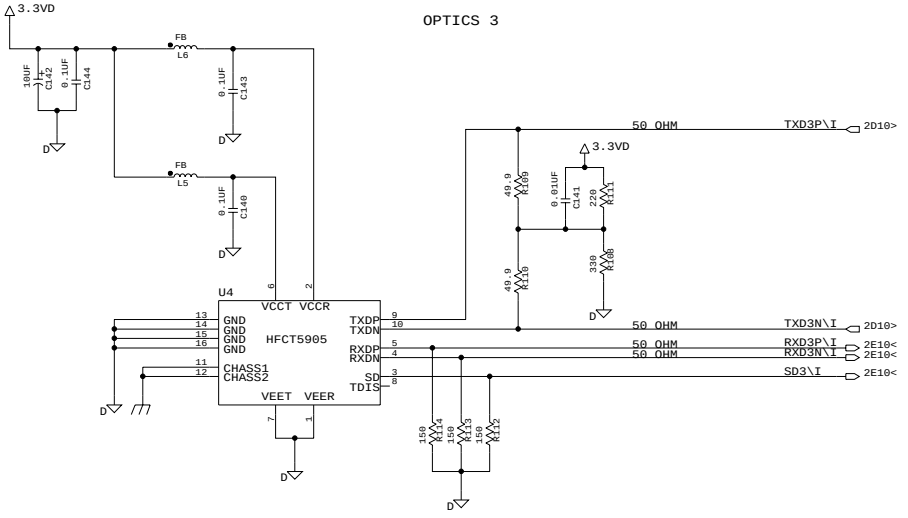

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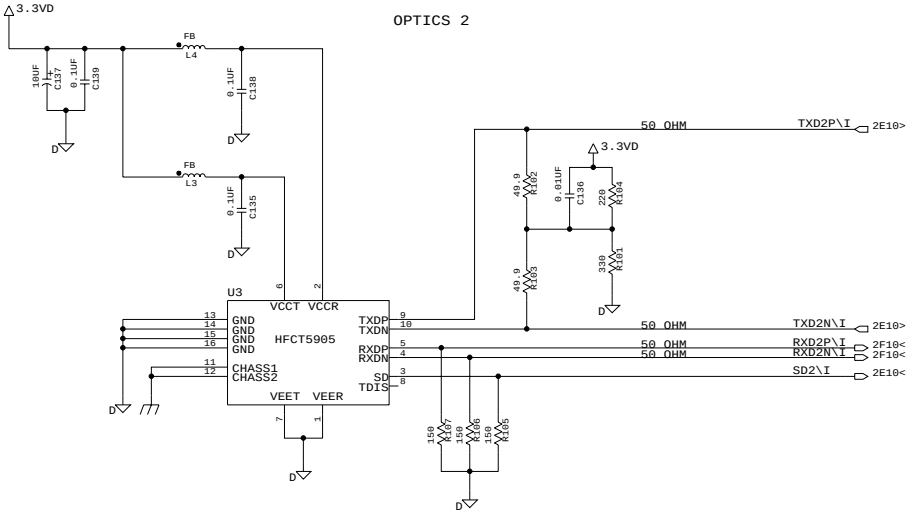

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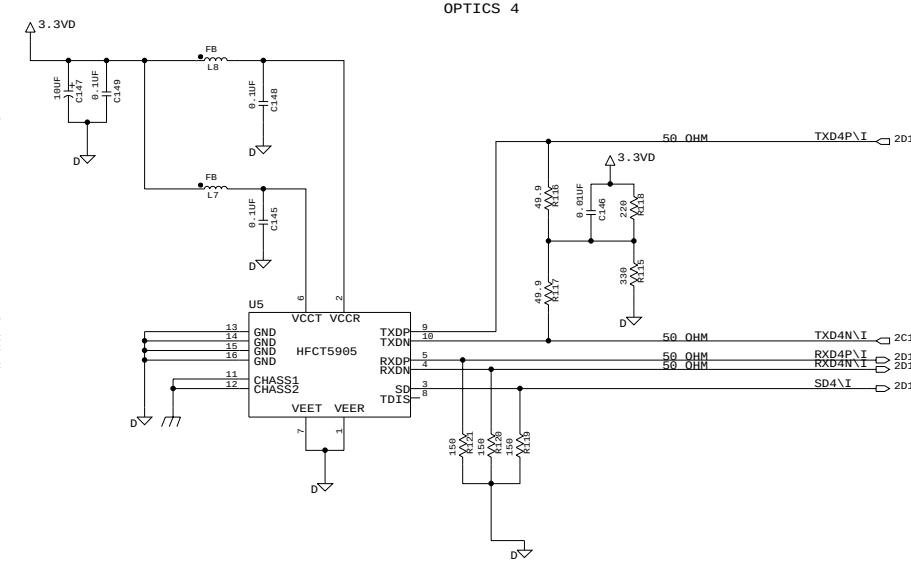

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TITLE: S/UNI-QUAD REFERENCE DESIGN OPTICS_BLOCK	DATE: 99/08/04
ENGINEER: PMC-SIERRA EC BDV	PAGE:9 OF 9

9.1 Bill of Materials

Table 3 : Major Components List

Ref. No	Component Description	Package Type	Quantity
U6	PMC-Sierra, Inc. PM5349 S/UNI-QUAD	SBGA304	1
U2-U5	Hewlett Packard Co. Tel: 1-800-235-0312 Fiber transceivers Singlemode: HFCT-5905 Multimode: HFBR-5905	2x5 DIP Style	4
U12	Motorola undervoltage sensor MC33064	SOIC8	1
U13, U14, U20-U23	Pericom 24 bit bus switch PI5C16212	TSSOP 54	6
U15	Pericom clock driver 74FCT807	SOIC20	1
U17	Motorola 32 bit microcontroller MC68332	PQFP 100	1
U24	Atmel FLASH memory AT29C010A	TSOP 32	1
U25	Cypress SRAM CY62128	TSOP 32	1
U26	Linear Technology RS232 driver LT1181A	SOIC16	1
U28	Xilinx FPGA XC4020XL	PQFP160	1
Y1	MMD Clock Oscillator 50.00 MHz, 100 PPM	4 Pins	1

Ref. No	Component Description	Package Type	Quantity
Y2	Connor-Winfield Clock Oscillator ASM54 19.44 MHz, 20 PPM	SMT	1
D1	SGS-Thomson Transil SMLVT3V3	SMB	1

~~11~~10 REFERENCES

- PMC-Sierra, Inc., PM5349 S/UNI-QUAD Data Sheet, Issue 2, March 1998
- Bell Communication Research – SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, December 1995
- Hewlett Packard, HFBR-5905 ATM Multimode Fiber Transceivers for SONET OC-3/SDH STM-1 in low cost 2x5 package style, Technical Data, July 1998
- Hewlett Packard, HFCT-5905 MT Duplex Single Mode Transceiver, Preliminary Technical Data, April 1998

NOTES

CONTACTING PMC-SIERRA, INC.

PMC-Sierra, Inc.
105-8555 Baxter Place Burnaby, BC
Canada V5A 4V7

Tel: (604) 415-6000

Fax: (604) 415-6200

Document Information: document@pmc-sierra.com
Corporate Information: info@pmc-sierra.com
Application Information: apps@pmc-sierra.com
(604) 415-4533
Web Site: http://www.pmc-sierra.com

PMC-980932 (R3) Issue date: September 1999