PM4351

COMET

COMET EVALUATOR BOARD DESIGN REV. 2.0

RELEASED

ISSUE 4: JUNE 2000

REVISION HISTORY

Issue No.	Issue Date	Originator	Details of Change
1	Nov. 1998	Fayaz Khaki	Document created.
2	Feb. 1999	Fayaz Khaki	Detailed information added Schematics and layout information added
3	Mar 1999	Fayaz Khaki	Updated BOM
4	Jun 2000	Marko Batic	The part number of a transformer TG261205N1 was exchanged by TG231505N1.

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1 FEATURES

General

- PCI Interface – allows for microprocessor access to the COMET via a host PC
- Provides a platform for the demonstration of the COMET's functions and performance.
- Provides software-selectable E1, T1, J1 rate selection.

T1 Mode

- Interface to short haul and long haul T1 lines
- Frames to D4, ESF, SF and SLC-96™ formats
- Integral HDLC controller for Facilities Data Link Support
- Per channel payload loopback
- Automatic gain control to accommodate cable lengths from 0 to 6000 feet
- Programmable Line buildouts of DSX-1 as well as CSU of –7.5dB, -15dB and –22dB
- Line interface capable of generating G.703 wave shapes for 100Ω T1 lines
- Provides a programmable PRBS test patter generator, receiver and analyzer.

E1 Mode

- Frames to FAS, CAS and CRC-4 formats
- Integral HDLC controller for Facilities Data Link Support
- Per channel payload loopback
- Automatic gain control to accommodate cable lengths from 0 to 2 km
- Line interface capable of generating G.703 wave shapes for both 75Ω and 120Ω E1 lines

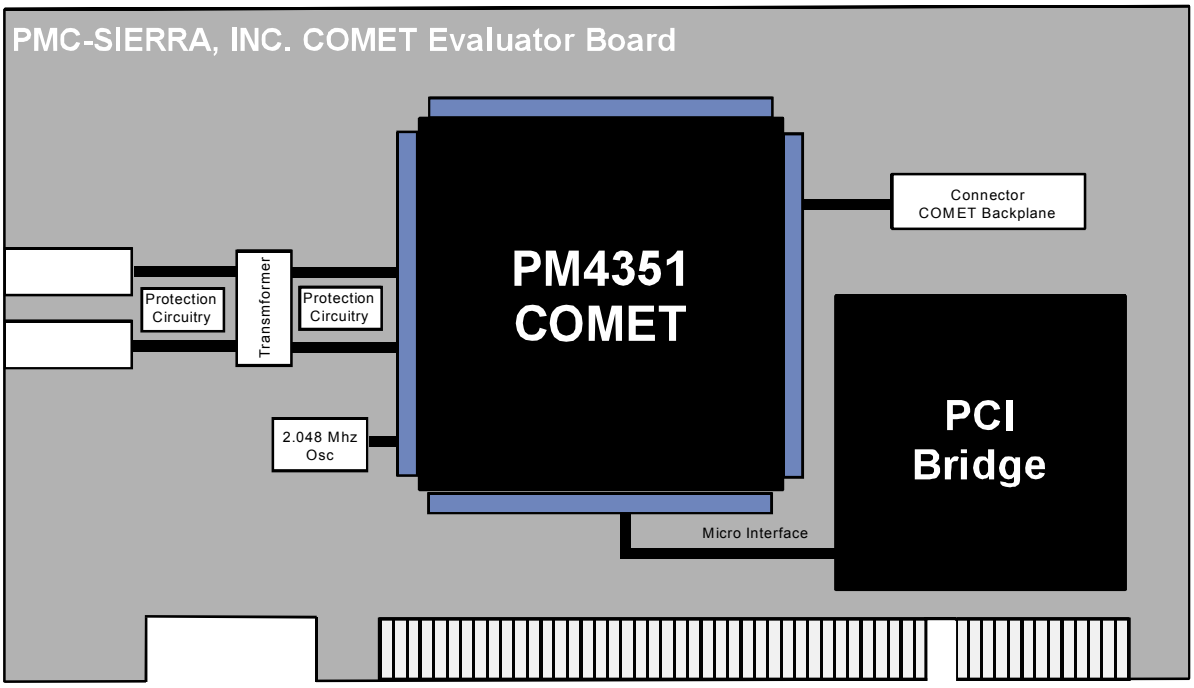
- Provides a programmable PRBS test patter generator, receiver and analyzer.

2 OVERVIEW

The COMET Evaluator board is part of the COMET Evaluation Kit and allows for the evaluation and demonstration of PMC-Sierra's PM4351 COMET device. It also provides a platform for the development and integration of software.

The COMET evaluator board is configured, monitored, and powered through the PCI edge connector. Software drivers are available from PMC-Sierra, Inc. to fully control and utilize the COMET evaluator board.

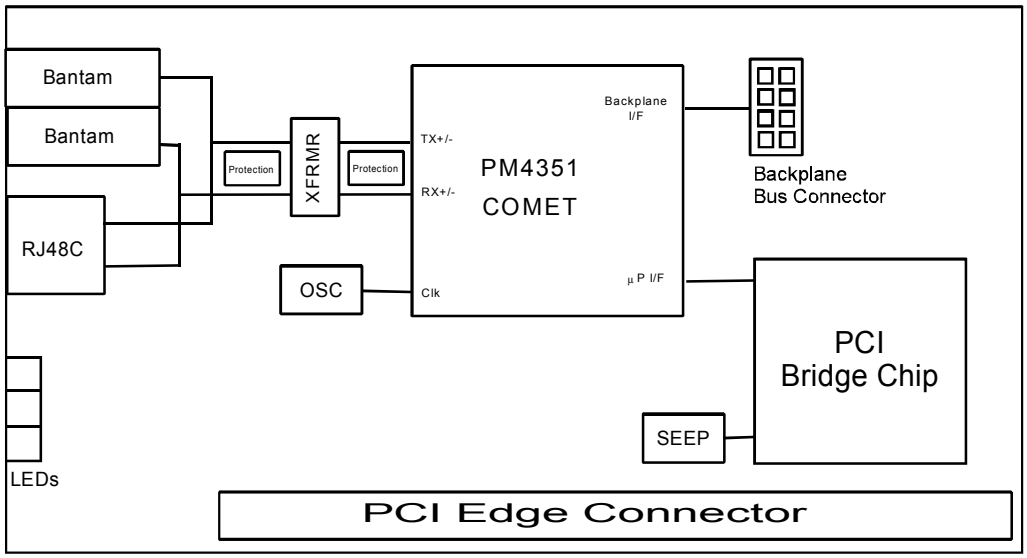
Figure 1: COMET Evaluator Board



3 FUNCTIONAL DESCRIPTION

3.1 Block Diagram

Figure 2: Block Diagram



3.2 COMET

The PM4351 Combined E1/T1/J1 Transceiver (COMET) is a feature-rich monolithic integrated circuit suitable for use in long haul and short haul T1, E1, and J1 systems with a minimum of external circuitry. The COMET is software configurable, allowing feature selection without changes to external wiring.

Analog circuitry is provided to allow direct reception of long haul E1 and T1 compatible signals with up to 43 dB cable loss (at 1.024 MHz in E1 mode) or up to 36 dB cable loss (at 772 kHz in T1 mode) using a minimum of external components. Typically, only line protection, a transformer and a line termination resistor are required. Digital line inputs are provided for applications not requiring a physical T1 or E1 interface.

The COMET recovers clock and data from the line and frames to incoming data. In T1 mode, it can frame to several DS-1 signal formats: SF, ESF, T1DM (DDS) and SLC®96. In E1 mode, the COMET frames to basic G.704 E1 signals and CRC-4 multiframe alignment signals, and automatically performs the G.706 interworking procedure. In J1 mode, the COMET can frame to the TTC JT-G704 J1 signal. AMI, HDB3 and B8ZS line codes are supported.

The COMET supports detection of various alarm conditions such as loss of signal, pulse density violation, Red alarm, Yellow alarm, and AIS alarm in T1 mode and loss of signal, loss of frame, loss of signaling multiframe and loss of CRC multiframe in E1 mode. The COMET also supports reception of remote alarm signal, remote multiframe alarm signal, alarm indication signal, and time slot 16 alarm indication signal in E1 mode. The presence of Yellow and AIS patterns in T1 mode and remote alarm and AIS patterns in E1 mode is detected and indicated. In T1 mode, the COMET integrates Yellow, Red, and AIS alarms as per industry specifications. In E1 mode, the COMET integrates Red and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events is provided in T1 mode. In E1 mode, CRC-4 errors, far end block errors, framing bit errors, and line code violation are monitored and accumulated.

Dual (transmit and receive) elastic stores for slip buffering and rate adaptation to backplane timing are provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

In T1 mode, the COMET generates framing for SF, ESF and T1DM (DDS) formats. In E1 mode, the COMET generates framing for a basic G.704 E1 signal. The signaling multiframe alignment structure and the CRC multiframe structure may be optionally inserted. Framing can be optionally disabled.

Internal analog circuitry allows direct transmission of long haul and short haul T1 and E1 compatible signals using a minimum of external components. Typically, only line protection, a transformer and an optional line termination resistor are required. Digitally programmable pulse shaping allows the transmission of DSX-1 compatible signals up to 655 feet from the cross-connect, E1 short haul pulses into 120 ohm twisted pair or 75 ohm coaxial cable, E1 long haul pulses into 120 ohm twisted pair as well as long haul DS-1 pulses into 100 ohm twisted pair with integrated support for Line Build Out (LBO) filtering as required by the FCC rules. In addition, the programmable pulse shape extending over 5-bit periods allows customization of short haul and long haul line interface circuits to application requirements. Digital line inputs and outputs are provided for applications not requiring a physical T1 or E1 interface.

In the transmit path, the COMET supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. Zero code suppression may be configured to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side

data and signaling trunk conditioning is also provided. Signaling bit transparency from the backplane may be enabled.

The COMET provides three transmit HDLC controllers. These controllers may be used for the transmission of messages on the ESF data link (T1) or national use bits (E1) and in any time slot. In T1 mode, the COMET can be configured to generate in-band loop back codes and ESF bit oriented codes. In E1 mode, transmission of the 4-bit Sa codewords defined in ETSI 300-233 is supported.

The COMET provides optional jitter attenuation in both the transmit and receive directions.

The COMET provides both a parallel microprocessor interface for controlling the operation of the device and serial PCM interfaces that allow backplane rates from 1.544 Mbit/s to 8.192 Mbit/s to be directly supported. Up to four COMET devices can be multiplexed on a byte-interleaved basis on a common bus with no additional arbitration logic. The COMET supports the Mitel ST® bus, AT&T CHI® and MVIP standards.

For a complete description of the COMET, please refer to PMC-Sierra's COMET databook, PMC-970624 [1].

3.3 PCI Bridge

The PCI Bridge used is PLX Technology's PCI9050 PCI Bus Target Interface Chip. The PCI9050 provides a target only interface, and as such does not initiate PCI bus transactions.

The local address space is configured to be 32-bit non-multiplexed, big endian, non-burst, and non-prefetchable. Even thought the COMET has only an 8-bit data bus, the PCI9050 is configured as a 32-bit data bus. This was done to simplify the hardware design. Prefetching is not possible in this application because the COMET has a number of registers with read side affects (e.g. interrupt status registers).

The local bus is clocked at 33MHz by looping the buffered PCI clock output (BCLKO) available from the PCI9050 back to the local bus clock input.

Please refer to the PCI9050 datasheet [4] for more information.

3.4 SEEP

The NM93CS46 Serial EEPROM from National Semiconductor is used to store configuration information for the PCI9050 bridge. This specific SEEP (or

equivalent) is required by PCI9050 because it supports sequential read operations.

The SEEP is 1Kbit deep, 800 bits of which are occupied by the PCI9050 configuration data, leaving 224 bits (28 bytes) unused.

Refer to the PCI9050 datasheet [4] for information on the format of the configuration data stored in the SEEP.

3.5 Oscillators

The COMET can run in either T1 or E1 mode. In T1 mode, oscillator Y1 should be populated with a 1.544 MHz oscillator. In E1 mode, oscillator Y1 should be populated with a 2.048 MHz oscillator.

3.6 Transmit and Receive Line Interface

The transmit and receive line interface consists of line connectors, line protection circuitry and magnetics.

The magnetics used on this design is a dual package that contains both a receive and transmit transformer. Both the receive and transmit transformers have a 1:2.42 turns ratio with the “1” always on the chip side. Please refer to Table 9 for a list of manufacturers.

The evaluator board provides two types of line interface connectors, a mini-bantam (J1 and J2) and RJ-48C (J3). Only one set of connectors can be used at anytime, either J1 & J2 or J3.

The mini-bantam connectors, J1 (Receive) and J2 (Transmit) are standard connectors used in T1/E1 interfaces.

The RJ48C has been provided according to the ANSI T1.403 standard for a Universal Service Ordering Code (USOC) connector. Table 1 below details the pinout for the RJ-48C connector.

Table 1: RJ-48C Pinout

Pin	Signal
1	RXRING
2	RXTIP
3	N.C.
4	TXRING
5	TXTIP
6	N.C.
7	N.C.
8	N.C.

3.7 Line Termination

The line interface provides one termination scheme for both T1 and E1 rates. A termination of 110Ω is used to allow the interface to be compatible with both 100Ω T1 and 120Ω E1. This provides a software switchable reference board for both T1 and E1 by simply configuring the COMET device.

3.8 Protection Circuitry

The protection circuitry prevents overvoltage and overcurrent power surge due to lighting strikes or other power impairments. This circuitry is intended to provide the necessary protection from both longitudinal (common mode) and metallic (differential) surges as well as for power cross.

This circuit has not undergone formal compliance testing however an identical circuit used on the COMET Reference Design [2] has passed both FCC Part 68 and ETSI 300 046.

The protection network employs PTC thermistors from Raychem. These devices exploit the positive thermal coefficient of polymer thermistors to provide relatively fast acting over-current protection. In this circuit they take the place of the series line resistors and fuses typically used in CSU protection circuits. Compared with

fuses, PTC thermistors have the advantage that they reset themselves after an over-current event. Unfortunately the resistance after the thermistors reset, referred to as the post-trip resistance, is often somewhat higher than the original resistance of the device. This could potentially unbalance the line and prevent the unit from returning to service.

The LC01-6 transient voltage suppressor (TVS) from Semtech serves to very quickly clamp any over-voltage transients on the transmit line. The device will zener during which the voltage drop across the device is typically less than 10V. When the voltage is interrupted or falls below the reverse standoff voltage of the device (6.0 V), the LC01-6 will return to a high impedance state.

The SRDA3.3-4 TVS diode array serves to further clamp any voltages above or below the power supply rails.

The transformers provide 1500Vrms line isolation and serve to impedance match the lines to the transceiver line interface. The transformer chosen for this application is a dual package that contains both a receive and transmit transformer.

Please refer to Table 9 for a list of manufacturers.

3.9 Power Supply

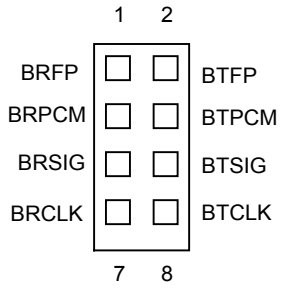
The COMET evaluator design contains components that operate at either 3.3V or 5V, referenced to ground. The 5V supply is provided to the board through the PCI connector. The 3.3V supply is generated on the board via a DC-DC voltage regulator.

It is recommended that 5.0V power is provided before 3.3V power to avoid device latchup. Please refer to the COMET datasheet [1]for further details of powering up the COMET device.

3.10 Backplane Bus Connector

The Backplane bus connector provides an interface to the COMET backplane signals. This is provided to allow for easy access to the backplane signals. By simply connecting across the jumpers (connecting pins 1 to 2, 3 to 4, etc), the backplane connector also allows for easy configuration of external payload loopback.

Figure 3: Backplane Connector



3.11 PCI Edge Connector

The PCI Edge Connector has been implemented as a standard 5.0V, 32 bit PCI connector.

4 SOFTWARE INTERFACE

4.1 Memory Map

Table 2: System Memory Map

PCI9050 Local Address Space	Address	Device	R/W	Description
CS_0	0000-00FF	PM4351 COMET	R/W	COMET Registers

4.2 PCI 9050 Configuration

The following sets of tables specify the values that should be programmed into the SEEP. These values will be loaded into the PCI9050 registers on power-up. Please refer to the PCI9050 datasheet [4] for further details.

NOTE: The checksum of the SEEP is 0x230D.

Table 3: PCI Local Address Space Register

Register	Address	Description	Value
PCIIDR	0x000	Device_ID|Vendor_ID	0x905010B5
PCIREV	0x004	Class_Code	0x06800000
PCISVID	0x008	Subsystem_ID|Subsystem_Vendor_ID	0x00000000
PCIILAR	0x00C	Maximum Latency MinimumGrant IntPin Routing	0x00000000

Table 4: PCI Local Address Space

Register	Address	Description	Value
LAS0RR	0x010	Local_Address_Space_0_Range	0x0FFFFC00
LAS1RR	0x014	Local_Address_Space_1_Range	0x00000000
LAS2RR	0x018	Local_Address_Space_2_Range	0x00000000

LAS3RR	0x01C	Local_Address_Space_3_	0x00000000
EROMRR	0x020	Expansion_ROM_Range	0x00000000

Table 5: PCI Local Address Space Re-Map

Register	Address	Description	Value
LAS0BA	0x024	LocalAddressSpace_0_Base_Address(Re-Map)	0x00000001
LAS1BA	0x028	LocalAddressSpace_1_Base_Address(Re-Map)	0x00000000
LAS2BA	0x02C	LocalAddressSpace_2_Base_Address(Re-Map)	0x00000000
LAS3BA	0x030	LocalAddressSpace_3_Base_Address(Re-Map)	0x00000000
EROMBA	0x034	Expansion_ROM_Base_Address(Re-Map)	0x00000000

Table 6: PCI Local Address Space Region Descriptors

Register	Address	Description	Value
LAS0BRD	0x038	LocalAddressSpace0_Bus_Region_Descriptors	0x1681A1A0
LAS1BRD	0x03C	LocalAddressSpace1_Bus_Region_Descriptors	0x00000000
LAS2BRD	0x040	LocalAddressSpace2-Bus_Region_Descriptors	0x00000000
LAS3BRD	0x044	LocalAddressSpace3_Bus_Region-Descriptors	0x00000000
EROMBRD	0x048	Expansion_ROM_Bus_Region_Descriptors	0x00000000

Table 7: PCI Chip Select Base

Register	Address	Description	Value
CS0BASE	0x04C	Chip_Select_0_Base	0x00010001
CS1BASE	0x050	Chip_Select_1_Base	0x00000000

CS2BASE	0x054	Chip_Select_2_Base	0x00000000
CS3BASE	0x058	Chip_Select_3_Base	0x00000000

Table 8: PCI Local Address Space Registers

Register	Address	Description	Value
INTCSR	0x05C	Interrupt_Control/Status	0x00000041
CNTRL	0x060	User_I/O| EEPROM|Init_Control	0x00024492
NULL	0x064	Null_data	0xFFFFFFFF
NULL	0x068	Null_data	0xFFFFFFFF
NULL	0x06C	Null_data	0xFFFFFFFF
NULL	0x070	Null_data	0xFFFFFFFF
NULL	0x074	Null_data	0xFFFFFFFF
NULL	0x078	Null_data	0xFFFFFFFF
NULL	0x07C	Null_data	0xFFFFFFFF

5 IMPLEMENTATION DESCRIPTION

The COMET Evaluator board schematics were captured using Cadence software Concept Schematics Capture tool.

5.1 ROOT DRAWING, Sheet 1

This sheet provides an overview of the major functional blocks of the COMET Evaluator board. It shows interconnections between the COMET_BLOCK, PCI_INTERFACE_BLOCK, LINE_INTERFACE and POWER blocks.

5.2 COMET BLOCK, Sheet 2

This sheet shows the COMET device and its power circuitry. The power circuitry includes a schottky diode for powering up the COMET device and separate filtering circuitry for the analog and digital power pins. A LED is connected to the INTB pin to allow for visual indication of interrupts being generated by the COMET.

5.3 LINE INTERFACE, Sheet 3

This sheet shows the termination, magnetics and protection circuitry for the line interface. A single dual package 1:2.42 transformer is used to couple the COMET transmit and receive line to the connectors. The LC01-6 transient voltage suppressor (TVS), the PTC and the SRD3.3-4 provide over voltage and lightning protection. Connection to both bantam and RJ48C connectors are provided.

5.4 PCI INTERFACE, Sheet 4

This sheet shows the PCI connector and the PCI bridge chip. The PLX PCI-9050 PCI bridge chip is compliant to PCI Specification 2.1.

5.5 POWER, Sheet 5

The LM3940 drop-out voltage regulator supplies 3.3V to the COMET device. Two LED's are provided to display the status of power to the COMET board, one for 5.0V and one for 3.3V.

6 LAYOUT DESCRIPTION

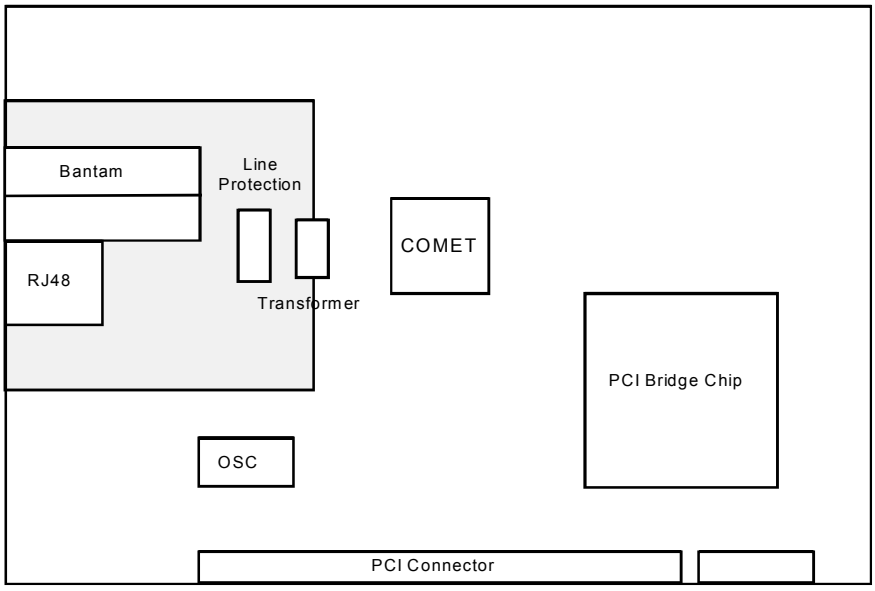
6.1 Component Placement

The overall placement strategies of the components are:

- Place the analog circuitry away from the digital circuitry.
- The PCI Bridge device is placed such that all the PCI interface traces are within the specified length limits of the PCI Rev. 2.1 Specification.
- The oscillator is placed in a quiet digital section as noise on its power supply will cause jitter on the output, and the oscillator itself generates noise that may affect sensitive analog circuits.
- All source termination resistors are placed near the outputs and load termination resistors are placed near the inputs.
- All pull up/down resistors are placed near the output pins.
- All decoupling capacitors are placed near the power supply pins.

The overall placement is as follows:

Figure 4: Main Component Placement Diagram



6.2 Layer Stacking and Transmission Line Impedance Control

The COMET Evaluator card has four layers: (from the top down) layer 1 and 4 for signals, layer 2 for ground, and layer 3 for power. The dimension of the card conforms to the 5V PCI Raw Short Card, with custom mounting hole locations. The layer configurations are shown below:

Figure 5: Layer Stack

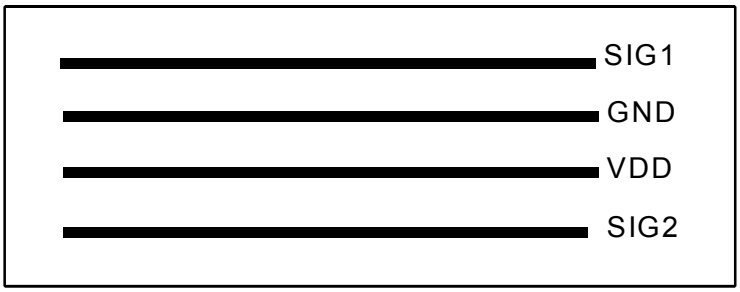
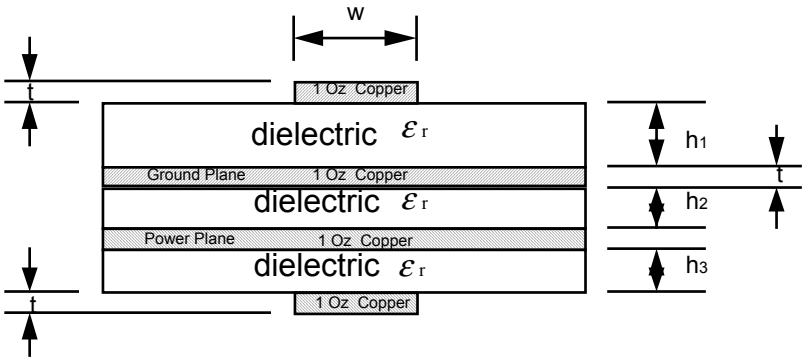


Figure 6: PCB Cross Section



where

ε_r = relative dielectric constant, nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected. For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric.

w = width of copper

The PCB related parameters are shown in the following table:

Parameters	Nominal
Board Thickness (mil)	62 (including copper thickness)
dielectric thickness between layers 1 and 2 (mil) (h1)	7
dielectric thickness between layers 2 and 3 (mil) (h2)	44
dielectric thickness between layers 3 and 4 (mil) (h3)	7
Relative dielectric constant	4.2

6.3 Power and Ground

One ground/Vdd pair is used for the whole board. The following diagrams illustrates the power and ground plane distribution:

Figure 7: GND Plane

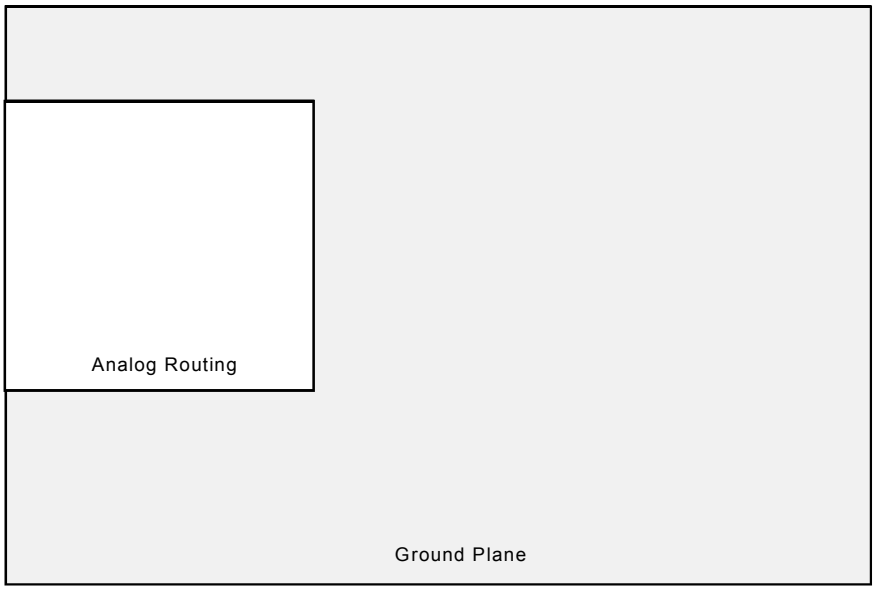
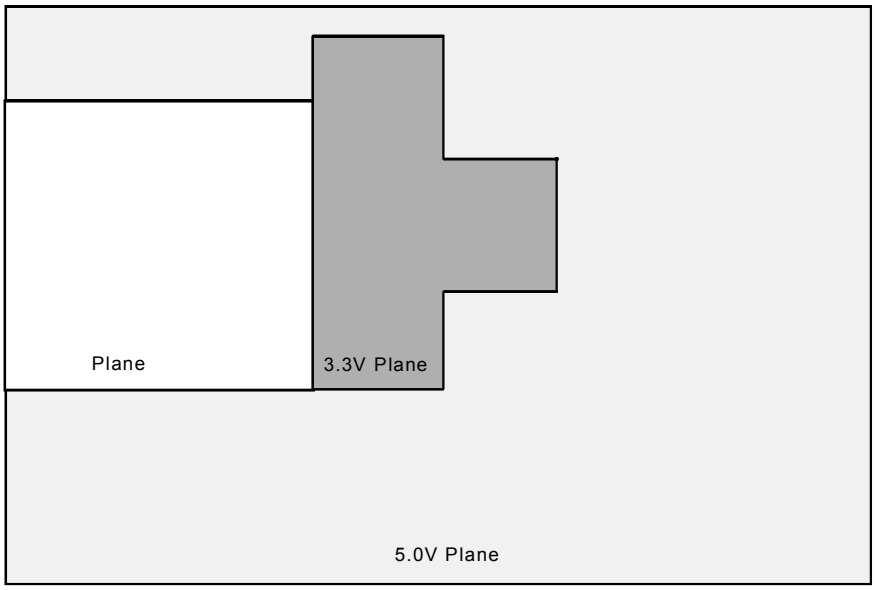


Figure 8: VDD Plane



A single ground is provided for all circuitry, except the transformer and RJ48 and Bantam connectors.

6.4 COMET Decoupling

All of the analog power supply pins of the COMET employ a RC Network to filter out low frequency Vdd noise. The analog power pins associated with the transmit circuitry also have fairly large capacitors connected to them to provide the large currents required to generate the transmit pulses.

A 0.1uF/0.01 uF decoupling capacitor is also placed as close to each VDDI/VDDO digital power pin as possible. Ferrite beads are not used on the digital power pins because they add series inductance which limits the current that is required to recharge the decoupling capacitors. If noise attenuation is required, a small surface mount series resistor (1 to 10 Ohms) can be added in series with the power pin.

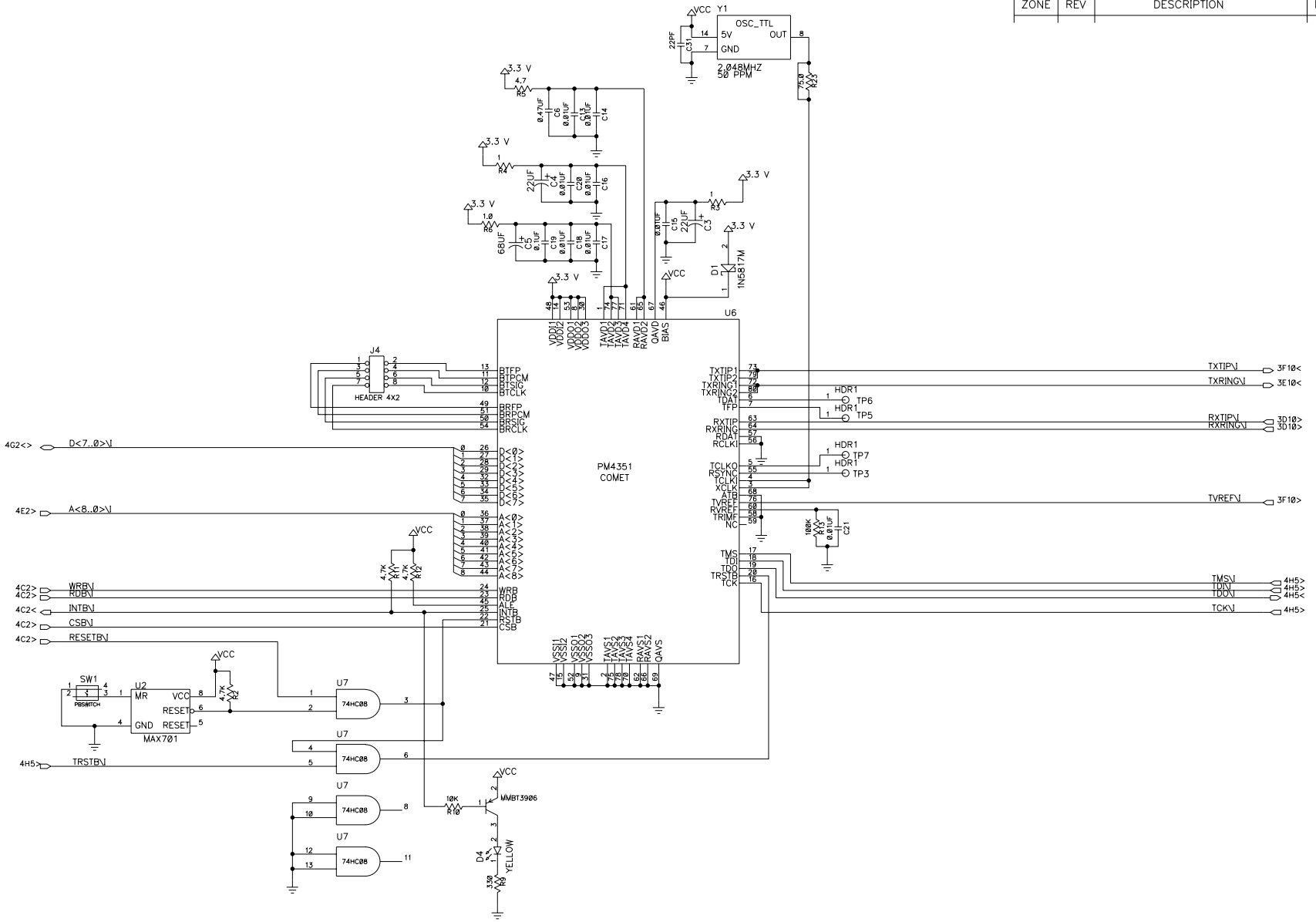
6.5 PCI Bus Signal Specification

This layout follows the PCI Rev. 2.1 Specification layout restrictions. **The PCI SIG specification has stringent and detailed rules on decoupling, power consumption, trace length limits, routing, trace impedance, as well as signal loading. Therefore, it is essential to check the latest PCI specification before proceeding with new designs and layouts**.

The COMET Evaluator design board conforms to the following PCI Specification/Recommendations:

- Component height on the component side does not exceed 0.570 inches, and on the solder side does not exceed 0.105 inches.
- PCI CLK signal trace is 2.5 inches +/- 0.1 inches and is connected to only one load.
- All 32-bit interface signals have the maximum trace length of 1.5 inches.
- Trace impedance for shared PCI signals are within 60 - 100 Ohm range, and trace velocity is between 150 and 190 ps/inch.
- 20 mil wide traces are used to connect the power and ground pins on PCI connector to their respective planes and the trace lengths are limited to 250 mil.
- Route all traces over continuous image planes.

7 SCHEMATICS



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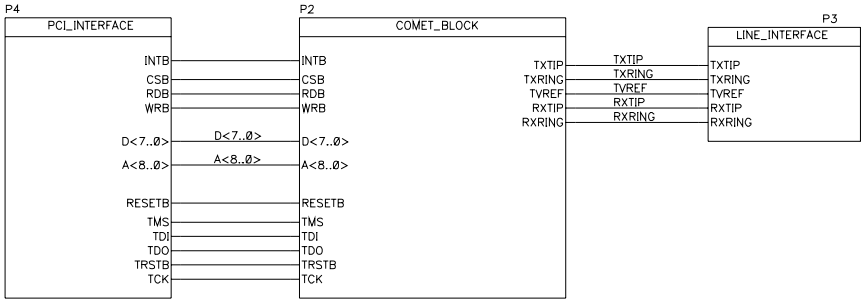

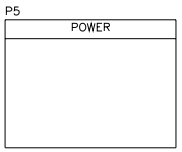

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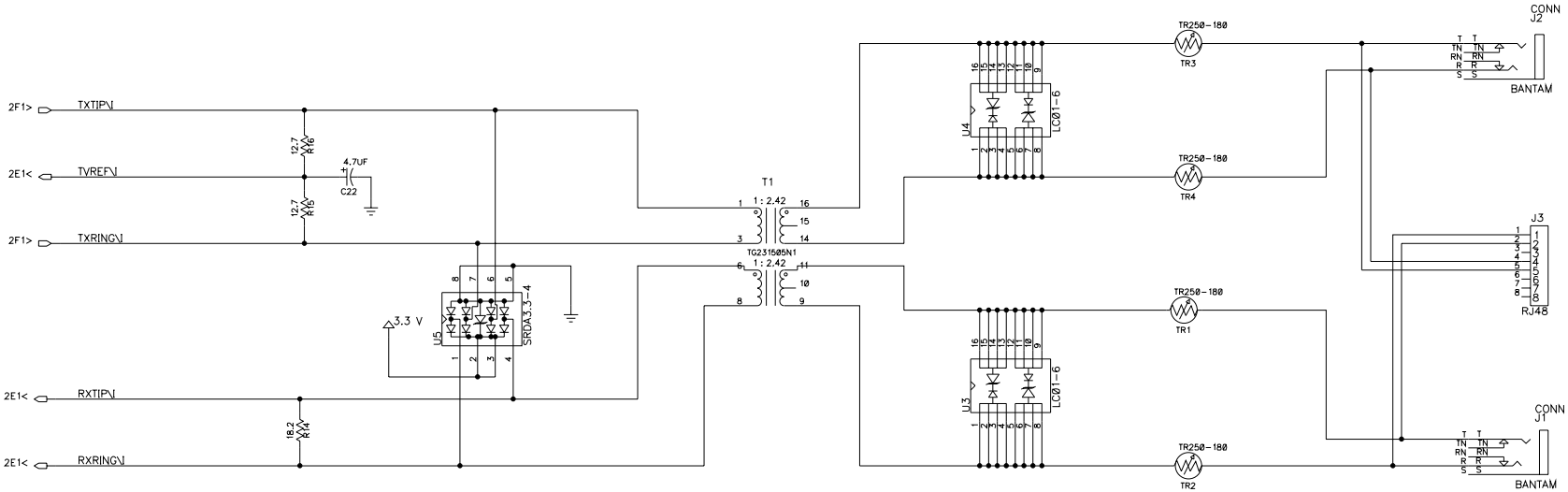

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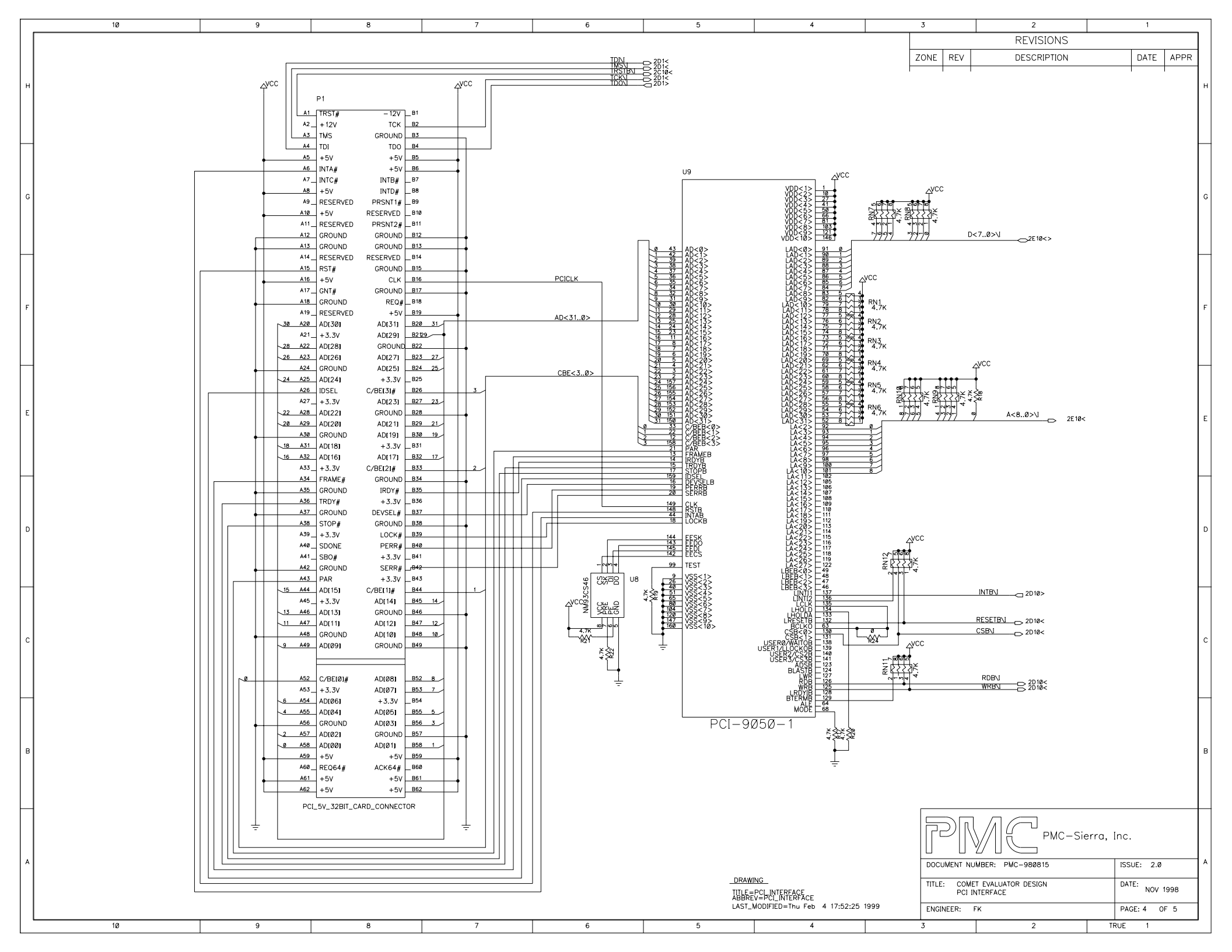
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REVISIONS				
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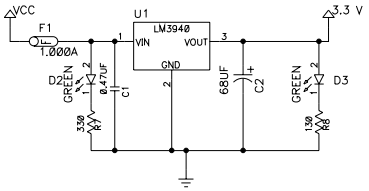
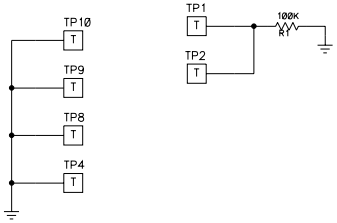
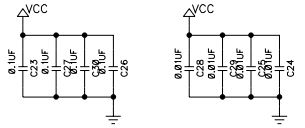
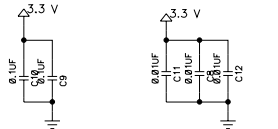






PLACE ONE CAP ON EACH SIDE OF THE PCI9050 DEVICE

PLACE ONE CAP ON EACH SIDE OF THE PCI9050 DEVICE



PLACE ONE CAP ON EACH VDDI PIN OF THE COMET

PLACE ONE CAP ON EACH VDDO PIN OF THE COMET

DRAWING

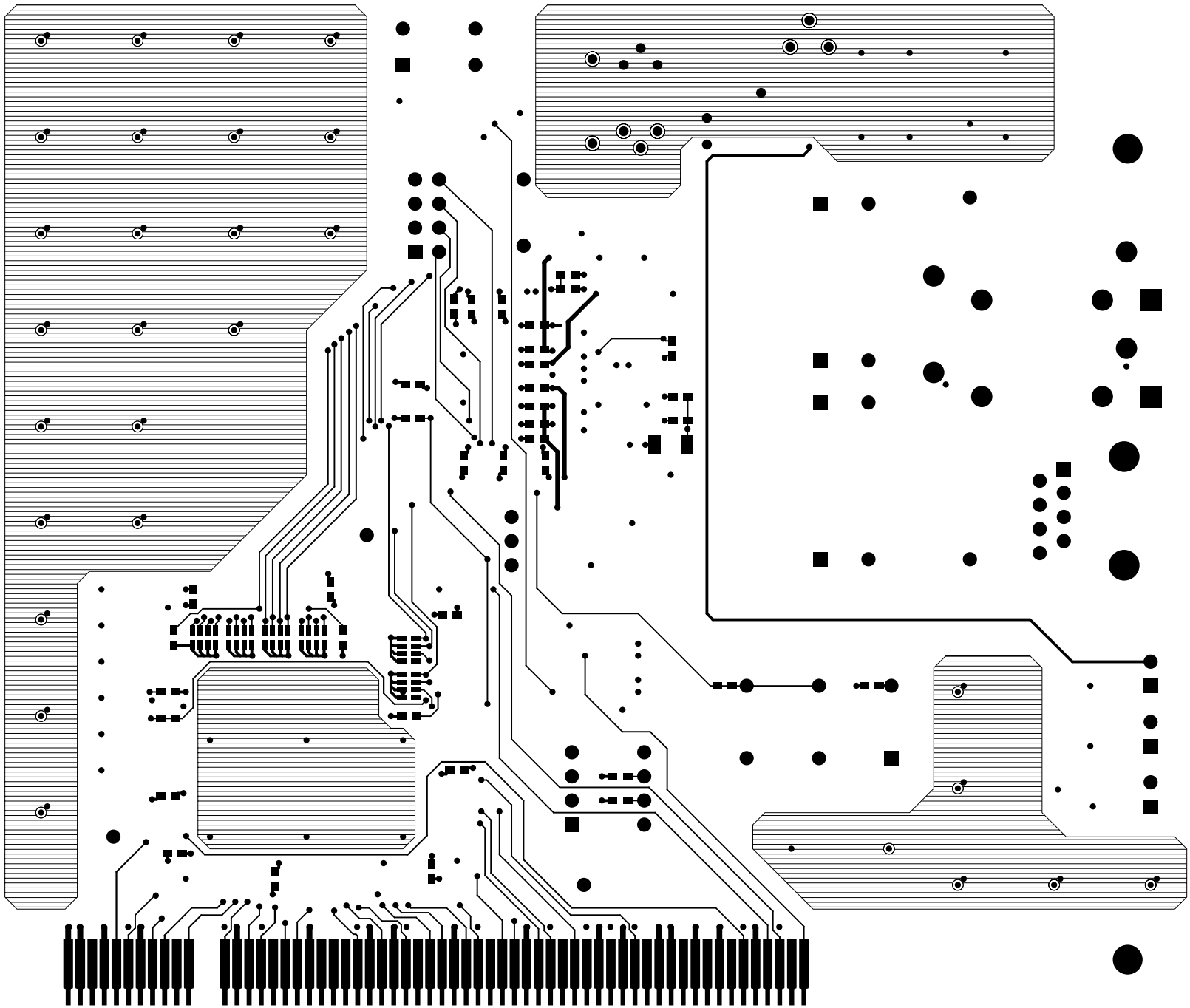
TITLE=POWER
ABBREV=POWER
LAST_MODIFIED=Thu Feb 4 17:52:20 1999

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980815	ISSUE: 2.0
TITLE: COMET EVALUATOR DESIGN POWER	DATE: NOC 1998
ENGINEER: FK	PAGE: 5 OF 5

8 LAYOUT

BOTTOM LAYER



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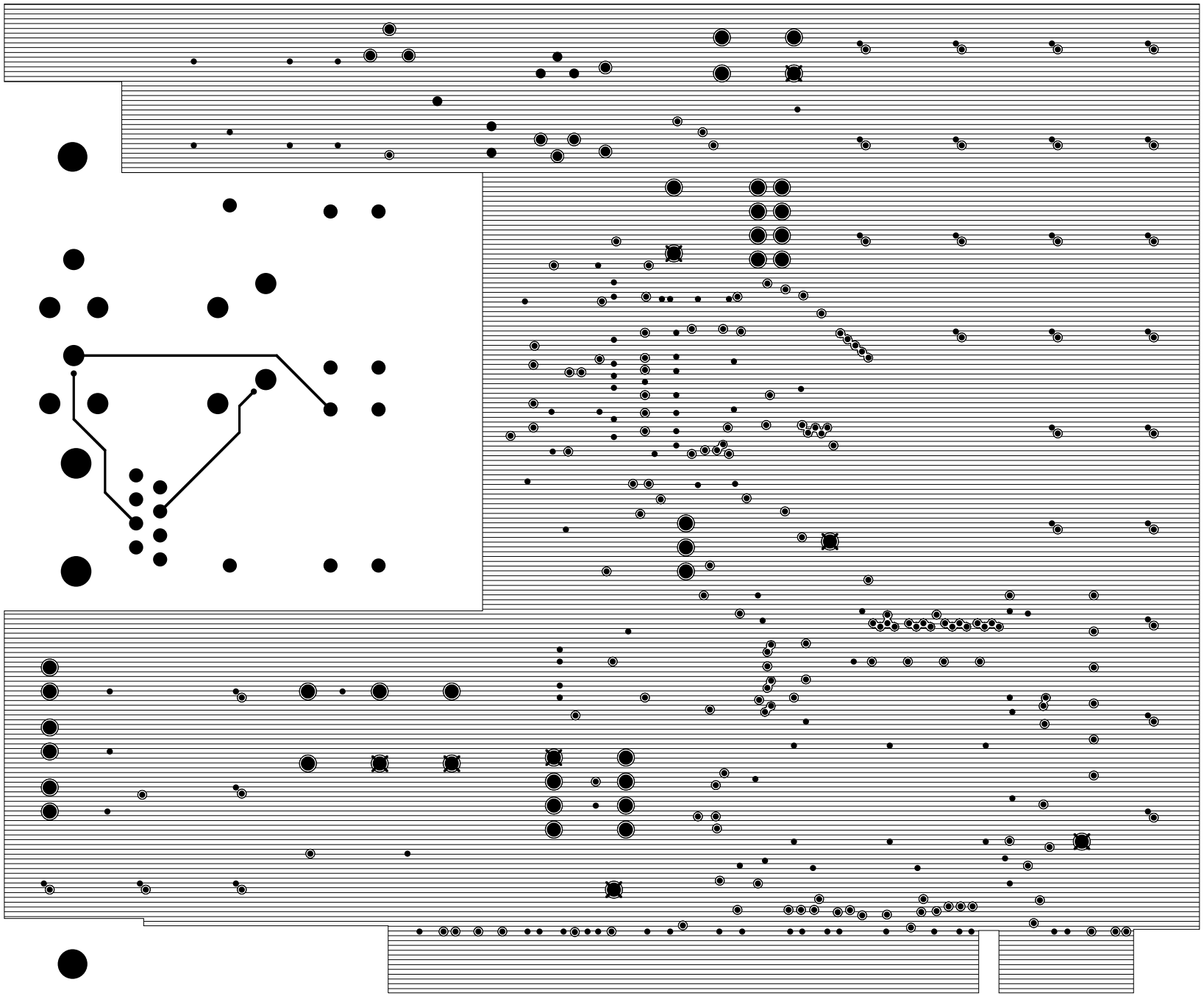
GND PLANE



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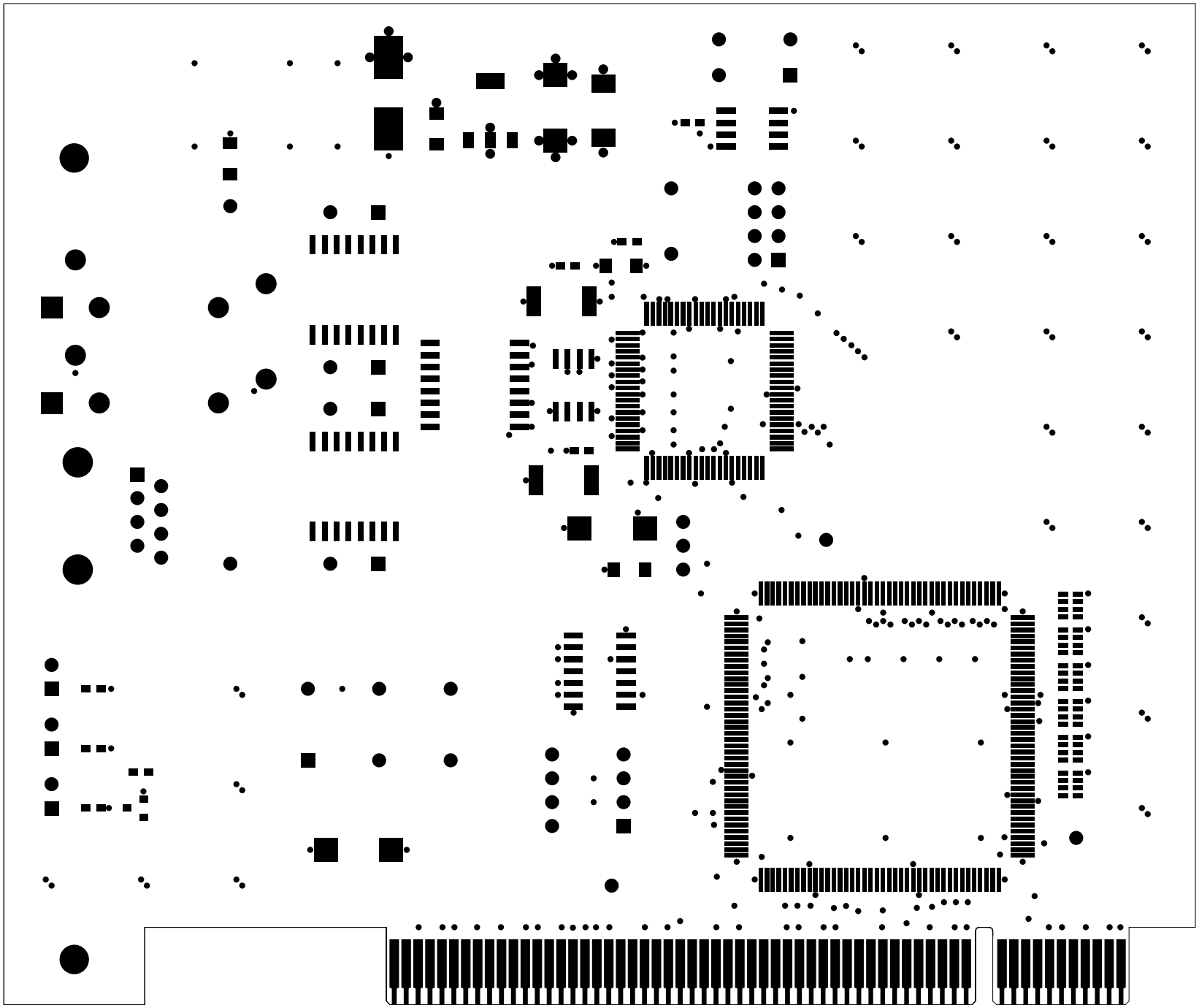
SOLDERMASK BOTTOM

SOLDERMASK TOP



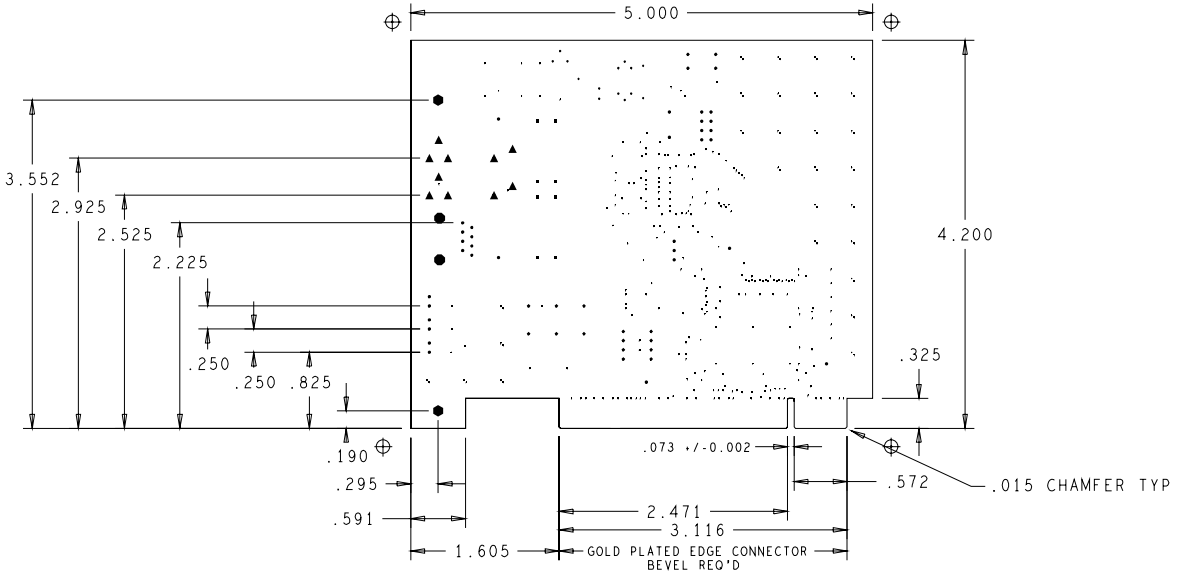
PMC-SIERRA COMET EVALUATOR BOARD REV.2.0 1998

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED

Material	Layer Type	Etch Name	Film Type	Thickness	Dielectric Constant
COPPER	CONDUCTOR	TOP	POSITIVE	0.72 mil	-------
FR-4	DIELECTRIC	-------	-------	7.0 mil	
COPPER	CONDUCTOR	GND_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	44.0 mil	
COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	1.44 mil	-------
FR-4	DIELECTRIC	-------	-------	7.0 mil	
COPPER	CONDUCTOR	BOTTOM	POSITIVE	0.72 mil	-------

Notes:

1. Copper thickness is 1/2 oz. on outer layers and 1 oz. on internal layers. All track width shown under Gerbr files are final trace width.
2. Total thickness of board shall be 62 mil +/- 7 mil. The stackup shown above is the final stackup of this board.
3. The outline dimension are spedified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil minimum copper wall thickness.
   All holes size shown are final hole size.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white base ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in/in per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.



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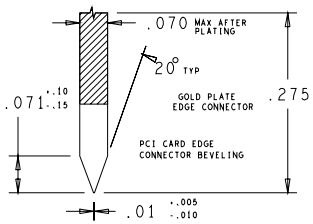
DRILL CHART			
FIGURE	SIZE	PLATED	QTY
·	13.0	PLATED	303
·	25.0	PLATED	14
▪	32.0	PLATED	8
•	36.0	PLATED	32
•	42.0	PLATED	18
▲	50.0	PLATED	10
⬢	125.0	NOT PLATED	2
●	128.0	NOT PLATED	2

ARTWORK FILM
TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
SOLDER PASTE TOP
SOLDER PASTE BOTTOM
MECH DRAWING



UNLESS OTHERWISE SPECIFIED		DATE YY	MM	DD
DIMENSIONS ARE IN INCHES	DRAWN			
TOLERANCES ON:	CHECKED			
2 PL DECIMALS +/- .03	ENGRG			
3 PL DECIMALS +/- .003	ISSUED			
ANGLES °				
FRACTIONS °				

PMC-Sierra, Inc.

105-8555 Baxter Place, Burnaby B.C. Canada, V5A 4V7

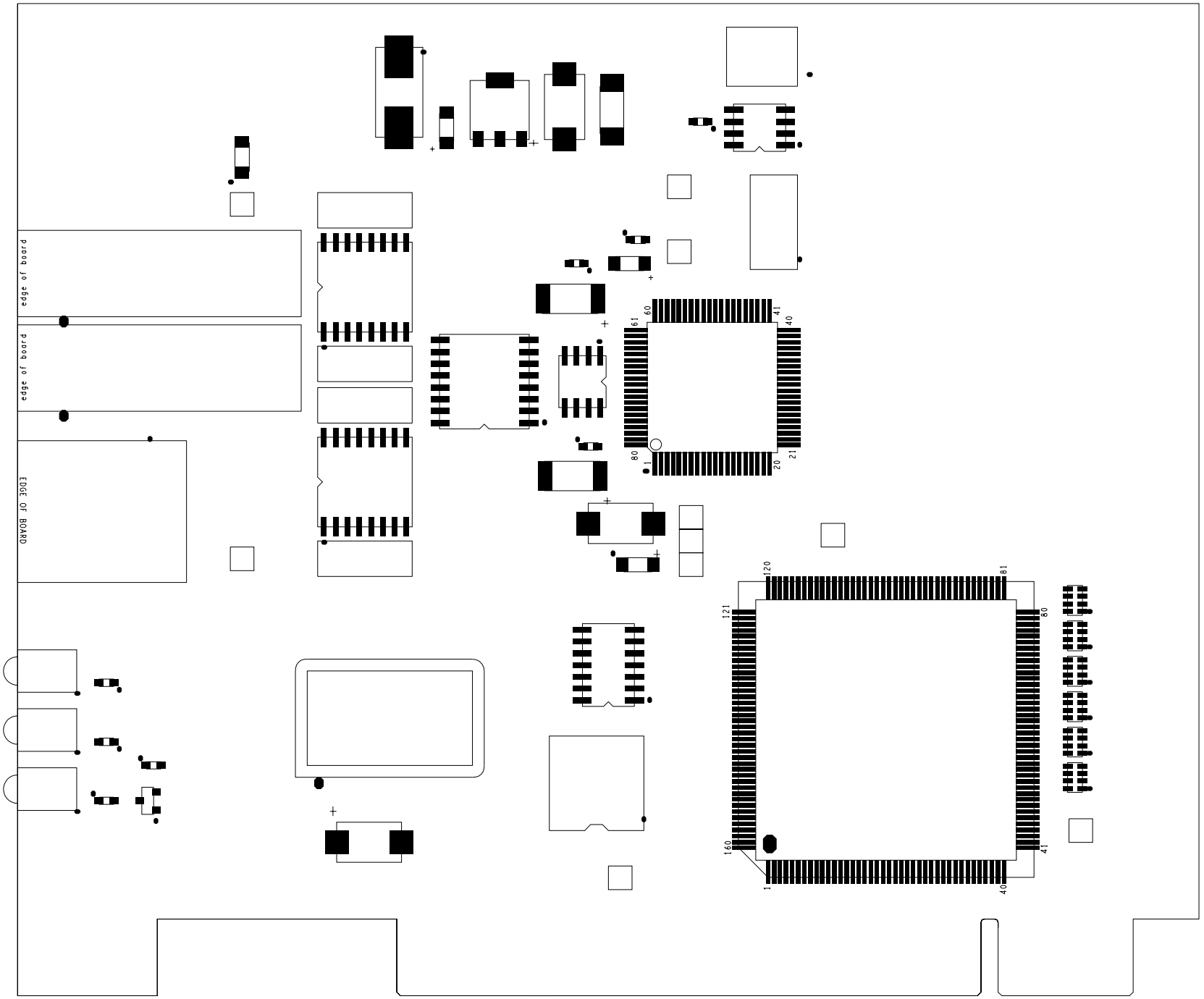
Tel: 604 415-6000 Fax: 604 415-6200

SIZE	FSCM NO	DWG NO
B		
SCALE	NTS	SHEET 1 OF 1

PMC-SIERRA COMET EVALUATOR BOARD REV.2.0 1998

COMP BOTTOM

COMP TOP



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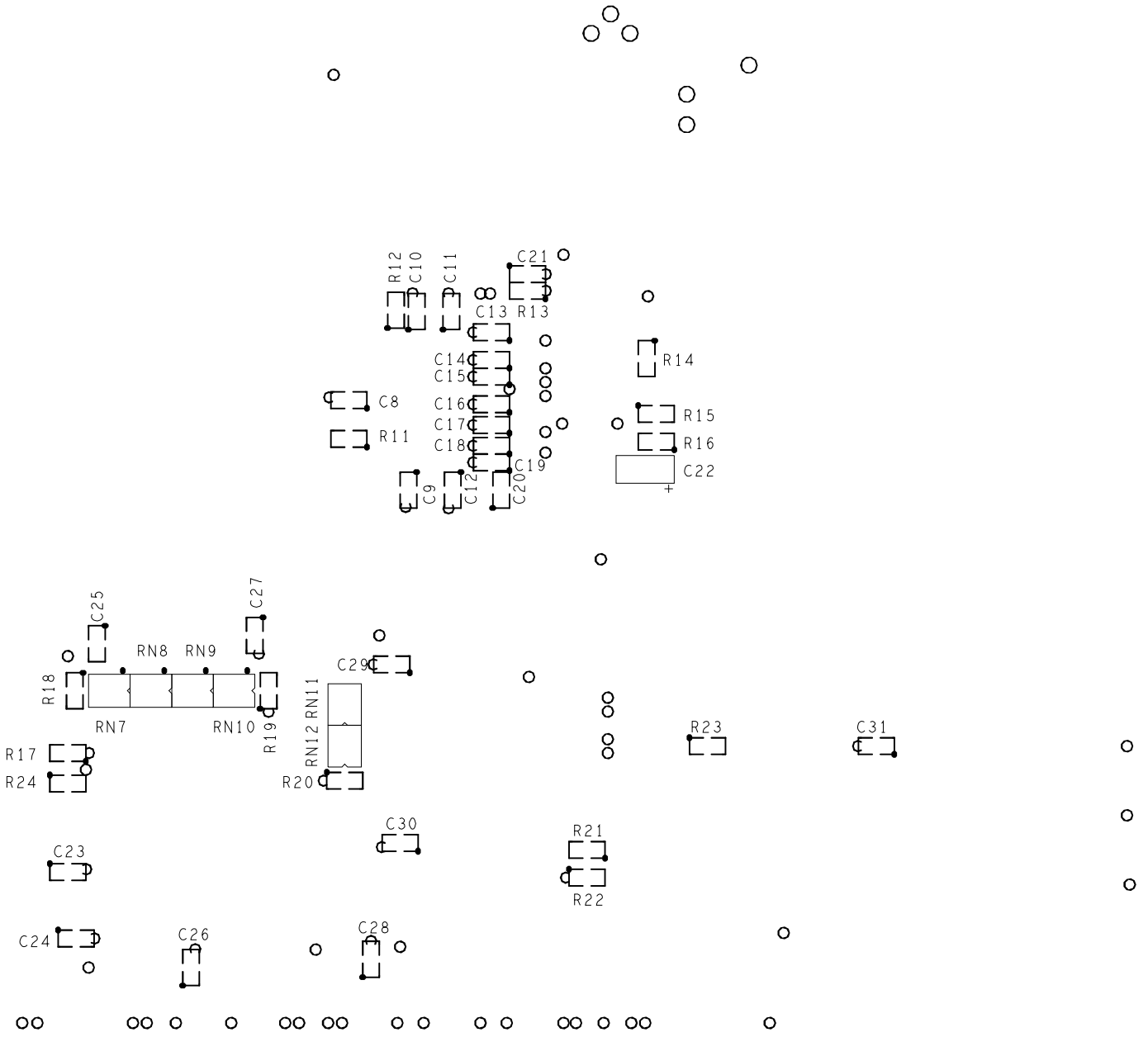
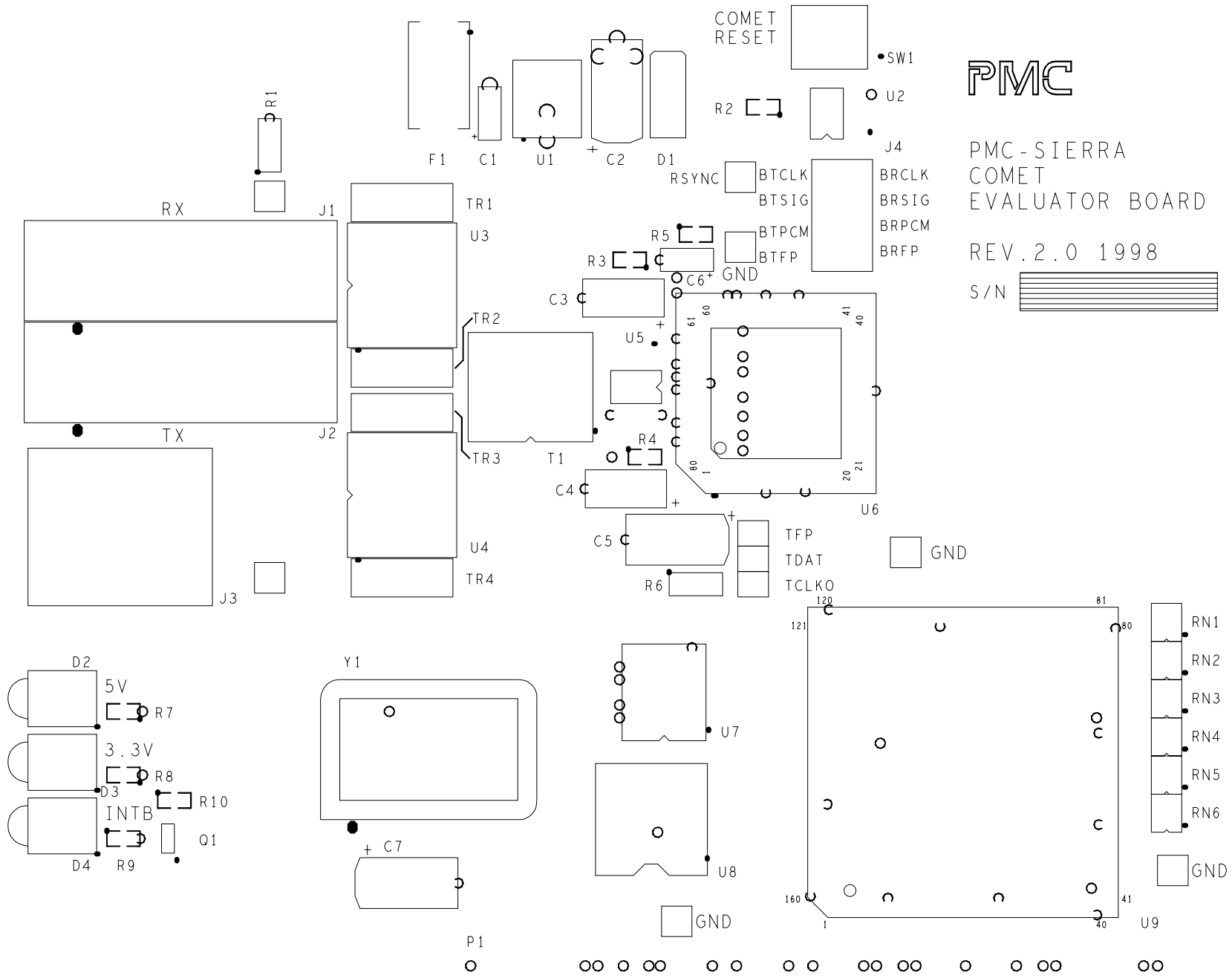
SILK SCREEN BOTTOM



PMC-SIERRA COMET EVALUATOR BOARD REV.2.0 1998

SILK SCREEN TOP



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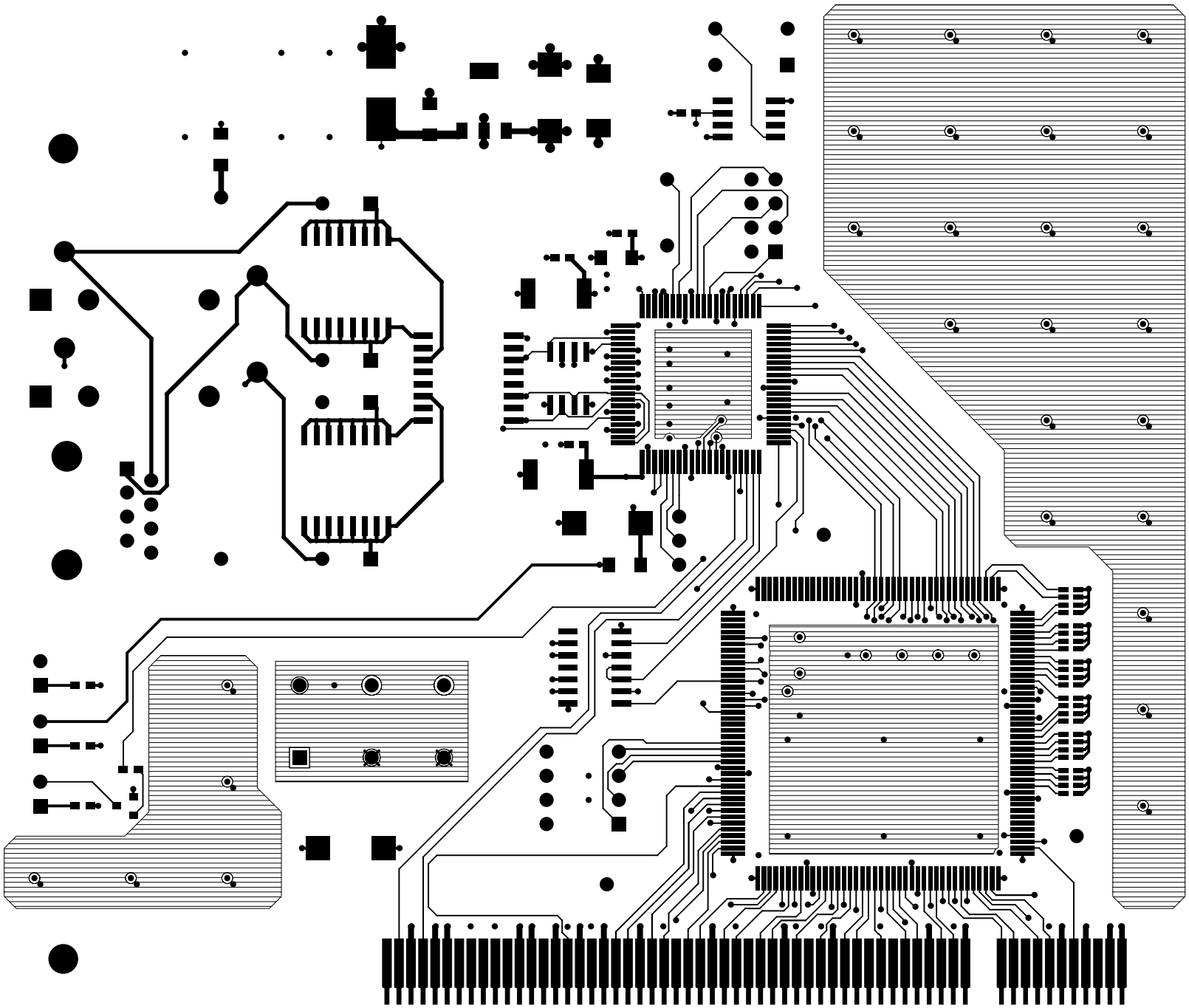
TOP LAYER



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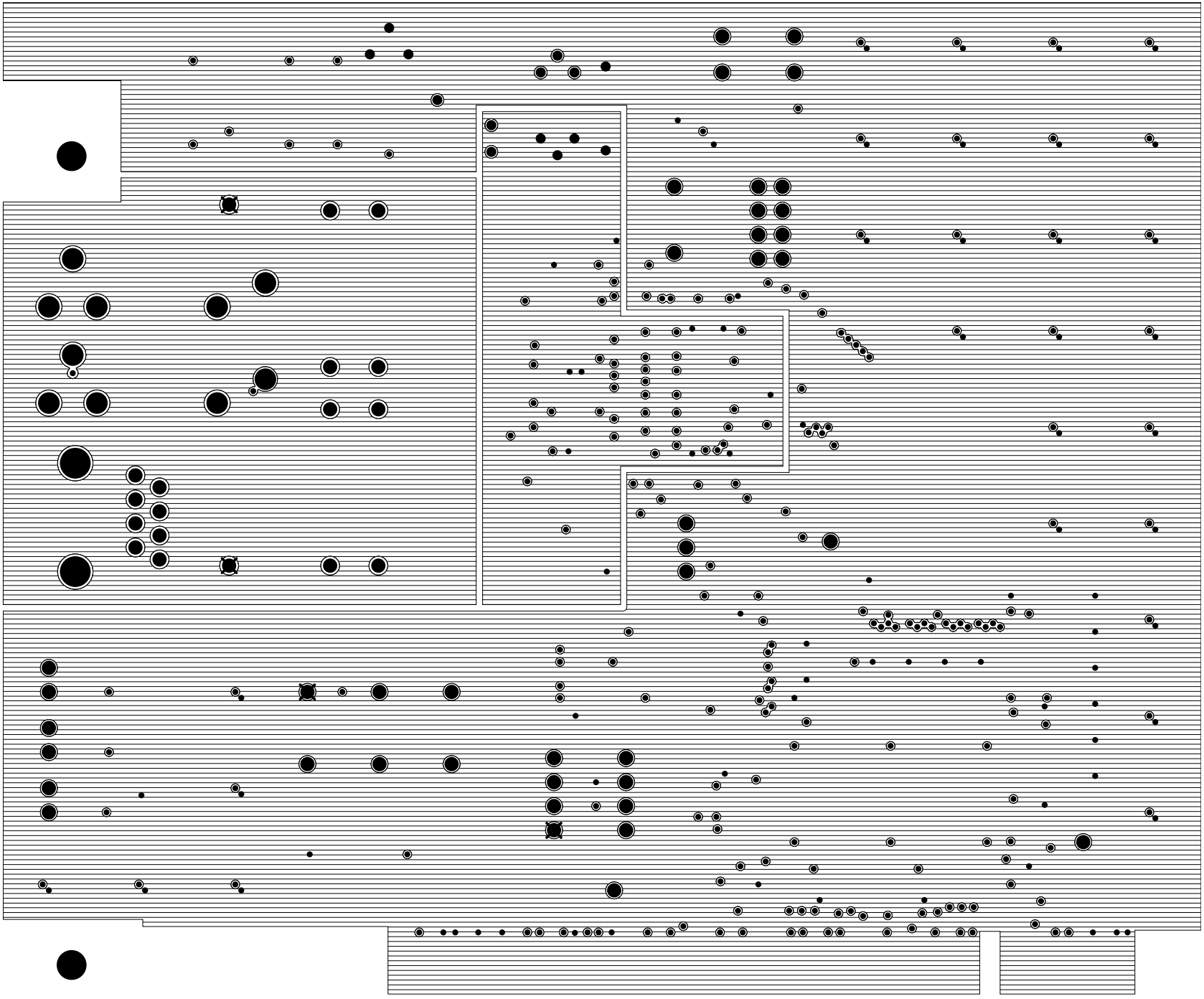
VCC PLANE



PMC-SIERRA COMET EVALUATOR BOARD REV.2.0 1998

9 BILL OF MATERIAL

Table 9: Major Components List

Ref. No	Component	Manufacturer	Package Type	Quantity
U3-U4	LC01-6	Semtech 805-498-2111	SOIC16	2
U5	SRDA3.3-4	Semtech	SOIC8	1
TR1-TR4	Thermistor-TR250-180	Raychem 800-227-7040	RES200	4
U5	LM3940	National Semiconductor 408-721-5000	SOT-223	1
U8	NM93CS46	Fairchild Semiconductor 1-800-364-3577	8-pin DIP	1
U9	PCI-9050	PLX Technology 800-759-3735	160 pin PQFP	1
T1	TG23-1505N1	Halo Electronics 650-568-6161	SMD 16 PIN	1
*	T1137	Pulse Inc. 619-674-8100	SMD 16 PIN	

* The T1137 Pulse transformer has not been tested.

Table 10: Bill of Materials

	Part Name - Value	Part Number	Ref Des	Qty
1	1N5817_-1N5817M	1N5817M	D1	1
2	74HC08_SOIC-HCMOS	74HC08D	U7	1
3	BANTAM-PCB Jacks	ELECTROSONIC PC-834-J-(BLACK)	J1, J2	2

4	CAPACITOR-0.01UF, 16V, X7R_603	DIGIKEY PCC103BVCT-ND Panasonic ECU-V1H103KBV	C8, C11-C18, C20, C21, C24, C25, C28, C29	15
5	CAPACITOR-0.1UF, 16V, X7R_603	DIGIKEY PCC1762CT Panasonic ECJ-1VB1C104K	C9, C10, C19, C23, C26, C27, C30	7
6	CAPACITOR-0.47UF, 25V, TANT TEH	DIGI-KEY PCT5474CT-ND Panasonic ECS-H1EY474R	C1, C6	2
7	CAPACITOR-22PF, 16V, NPO_603	DIGI-KEY PCC220ACVCT Panasonic ECU-V1H220JCV	C31	1
8	CAPACITOR-22UF, 6.3V, TANT TEH	DIGI-KEY PCT1226CT-ND Panasonic ECS-H0JC226R	C3, C4	2
9	CAPACITOR-4.7UF, 10V, TANT TEH	DIGI-KEY PCT2475CT-ND Panasonic ECS-H1AX475R	C22	1
10	CAPACITOR-47UF, 6.3V, TANT TEH	DIGI-KEY PCT1476CT-ND Panasonic ECS-H0JD476R	C7	1
11	CAPACITOR-68UF, 6.3V, TANT TEH	DIGI-KEY PCT1686CT-ND Panasonic ECS-H0JD686R	C2, C5	2
12	COMET_QFP-BASE	PMC PM4351-RI	U6	1
13	FUSE__SMD_SOCKET-1.000A, NANO	DIGIKEY F1222CT-ND Littelfuse 154001	F1	1
14	HEADER .1”x.1” straight male	DIGI-KEY S1011-36-ND Sullins PZC36SAAN	TP1-TP10	10
15	HEADER_4X2 4 position header, straight male	DIGI-KEY S2031-36-ND	J4	1

16	LC01_6_SMD-BASE	SEMTECH LC01-6	U3, U4	2
17	LED-GREEN, PCB .29 RIGHT ANGLE	DIGI-KEY L20365-ND Chicago Mini/SLI 5650F5	D2, D3	2
18	LED-YELLOW, PCB .29 RIGHT ANGLE	DIGI-KEY L20367-ND Chicago Mini/SLI 5650F7	D4	1
19	LM3940_SOT-BASE	LM3940IMP-3.3	U1	1
20	MAX701_SOIC-BASE	MAXIM MAX701ESA	U2	1
21	MMBT3906_SOT23-BASE	MMBT3906LT1	Q1	1
22	NM93CS46_DIP_SOCKET-BASE	NM93CS46EN Fairchild NM93CS46	U8	1
23	OSC_TTL_DIP-2.048MHZ , 50 PPM, CHA	Champion K1150BA-2.048Mhz MMD MA050T-2.048Mhz	Y1	1
25	PBSWITCH-BASE Pushbutton switch	DIGI-KEY P8007S-ND	SW1	1
26	PCI9050_PQFP-BASE	PLX PCI9050	U9	1
27	RESISTOR-0, 5%, 603	DIGI-KEY P000-GCT-ND	R24	1
28	RESISTOR-1, 5%, 603	Xicon 301-1.0	R3, R4	2
29	RESISTOR-1.0, 1%, 1206	DIGI-KEY P1.0RCT-ND Panasonic ERJ-8RQF1.0	R6	1
30	RESISTOR-100K, 1%, 603	DIGI-KEY P100KHCT-ND Panasonic ERJ-3EKF100K	R13	1

31	RESISTOR-100K, 5%, 1206	DIGI-KEY P100KECT-ND Panasonic ERJ-8GEYJ100K	R1	1
32	RESISTOR-10K, 1%, 603	Panasonic ERJ-3EKF10K	R10	1
33	RESISTOR-12.7, 1%, 603	DIGI-KEY -- P12.7HCT-ND Panasonic ERJ-3EKF12.7	R15, R16	2
34	RESISTOR-130, 5%, 603	DIGI-KEY P130GCT-ND Panasonic ERS-3EKE18.2	R8	1
35	RESISTOR-18.2, 1%, 603	DIGI-KEY P18.2HCT-ND Panasonic ERJ-3GSYJ330	R14	1
36	RESISTOR-330, 5%, 603	DIGI-KEY P330GCT-ND Panasonic ERJ-3GSYJ330	R7, R9	2
37	RESISTOR-4.7, 5%, 603	Xicon 301-4.7	R5	1
38	RESISTOR-4.7K, 5%, 603	Panasonic ERJ-3GSYJ4.7K	R2, R11, R12, R17-R22	9
39	RESISTOR-75.0, 1%, 603	Panasonic ERJ-3EKF75.0	R23	1
40	RES_ARRAY_4_SMD-4.7K	DIGI-KEY Y44.7KCT-ND Panasonic EXB-V8V4K7JV	RN1-RN12	12
41	RJ48-MOLEX_95001	MOLEX 95001-9841 (part # 95122-2881 from Richey Electronics (604-420-0313))	J3	1
42	SRDA3_3_4_SMD-BASE	SEMTECH SRDA3_3_4	U5	1
43	TG231505N1_SOIC-BASE	TG231505N1	T1	1
44	THERMISTOR-TR250-180 , RES200	Raychem TR250-180U	TR1-TR4	4
45	Socket	DIGI-KEY ED5037	Y1	6

46	8 pin dip socket	DIGI-KEY ED6008-ND Mill Max 614-93-308-31-012	U8	1
47	Bantam Covers	ADC Telecommunications PC-834-C-Black	J1, J2	2
48	Shorting Jumpers	DIGI-KEY S9002-ND Sullins SSC02SYAN	J4	4

Note:
Item 27 – 0 ohm resistor does not have to be populated

10 GLOSSARY

CompactPCI	Compact Peripheral Component Interconnect. A bus standard based on the PCI standard which defines a more rugged mechanical form factor for industrial use.
CSU	Channel Service Unit.
DS1	Off-premise T1 interface level provided by CSU.
DSX-1	Digital Cross-connect T1 interface level.
E1	European First Order transmission format. This is the standardized (ITU-T G.704) base format of the European Pleisosynchronous Digital Hierarchy. It operates at 2.048Mbps. The E1 format consists of frames consisting of 32 octets, or timeslots (numbered 0 to 31). Timeslot 0 alternates between containing an FAS and containing the National Use bits (Sn[8:4]) and an A-bit for RAI. Timeslot 0 also contains an International Use Bit (Si) which can be used to support CRC Multiframe.
HDLC	High Level Data Link Control. A family of bit-oriented protocols providing frames of information with address, control and frame check sequence fields.
MVIP	Multi-Vendor Integration Protocol. A TDM bus standard which is an extension of Mitel's ST-BUS. The MVIP bus is used in computer telephony integration applications.
PCI	Peripheral Component Interconnect – A bus standard which defines 32 bit transfers over a defined electrical interface.
PCI Host	An adapter board for a PCI system which acts as a PCI Master and performs the additional functions of clock distribution and bus arbitration.
PCI Target	An adapter board for a PCI system which does not initiate bus transactions. Also known as a slave.
ESF	Extend Super Frame format.
RJ-48C	An 8 pin RJ-45 modular connector with a standardized pinout used for 100 ohm T1 and 120 ohm E1 interfaces.

SEEP	Serial EEPROM (Electrically Erasable Programmable Read Only Memory) – A type of non-volatile memory which is programmed and read using a serial interface.
T1	T1. A level 1 digital trunk operating at 1.544 Mbit/s that is popular in North America and Japan. It is made up of 193 bits, grouped as 1 framing bit followed by 24 DS-0 channels of 8 bits each.
T1.403	A standard specifying a DS1-rate metallic interface, referred to as the network interface (NI), between the network and a customer installation.
TDM	Time Division Multiplexed – A TDM signal consists of several channels of data which are multiplexed together in time so that a byte (or word, etc.) of one channel of data is transferred, following by a byte of the second, etc.

11 REFERENCES

1. PMC-Sierra, Inc., PM4351 COMET Data Sheet, Issue 4, April 1998
2. PMC-Sierra, Inc., PM4351 COMET Reference Design, Issue 2, April 1998
3. ANSI - T1.403-1995 – American National Standard for Telecommunications – Carrier to Customer Installation – DS-1 Metallic Interface Specifications.
4. PLX Technology, PCI 9050-1 Data Book, Version 1.01, April 17, 1997

NOTES

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