PM6388/PM4388

EOCTL/TOCTL WITH FREEDM-8

REFERENCE DESIGN

RELEASED

ISSUE 2: JANUARY 1999

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CONTENTS

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

PROPRIETARY AND CONFIDENTIAL TO PMC-SIERRA, INC., AND FOR ITS CUSTOMERS' INTERNAL USE

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[10]. PCI SIG, PCI Local Bus Specification, June 1, 1995, Version 2.1

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1 OVERVIEW

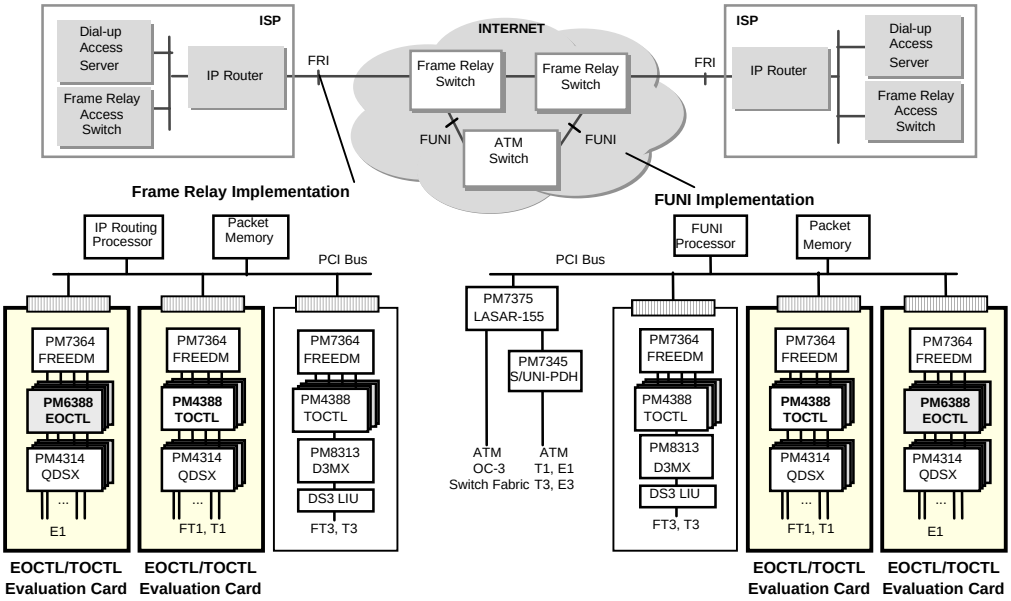
1.1 Application Perspective

The focus of the Reference Design is to show implementation of the E1/DS-1 line interface Card with PM6388 Octal E1 Framer (EOCTL) and PM4388 Octal T1 Framer (TOCTL). The FREEDM-8 (PM7366), the QDSX (PM4314) and the physical E1/DS-1 line interface are also key components of this Reference Design.

This Reference Design provides an application example of a circuit that supports a total of eight E1/T1 data links. At the system side, the PCI Bus transfers the data for upper level processing interface. The eight E1/DS-1 line interfaces are implemented using two PMC-Sierra's QDSXs. The QDSX is a physical layer device. On the system side the FREEDM-8 device interfaces to a 5/3.3Volt, 32bit, PCI connector compliant with the PCI SIG Specification Rev. 2.1. Software drivers are provided to interface the FREEDM-8 and the PC host. The EOCTL device sits between those two interfaces and provides data extraction and framing.

Example of high-level system architecture is shown in FIGURE 1.

FIGURE 1. Frame Relay Inter-Networking Overview



This Reference Design fits well into the Frame Relay network shown in figure above.

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The QDSX device is software configurable and supports both the E1 and DS-1 line interface.

The FREEDM-8 standard product is primarily designed for the frame relay application. Frame relay is a multiplexed data networking technology supporting connectivity between user equipment (routers, nodal processors/fast packet switches) and between user equipment and the public frame relay network. The frame relay protocol supports data transmission over a connection-oriented path and enables the transmission of variable-length data units over an assigned virtual connection.

User equipment such as routers, E1/T1 multiplexers, front end processors (FEPs), and packet assemblers/dissemblers (PADS) need to support the frame relay interface in order for them to be connected to a private or a public frame relay network.

1.2 Design Constraints

The purpose of the "EOCTL/TOCTL With FREEDM-8" Reference Design is to serve as an example to assist designers of data routers and frame relay switches to design their products using PMC-Sierra's FREEDM-8, EOCTL/TOCTL and QDSX standard products, as shown in FIGURE 1.

This design illustrates the frame relay application with interfaces to channelized and unchannelized E1/T1 data streams. The hardware which implements these interfaces is built, tested and debugged thereby assisting designers to more quickly bring their designs to market.

The following hardware constraints have been included in this design:

- Support the PCI local bus revision 2.1, which allows up to four PCI devices per PCI bus segment to be connected to a host processor and packet memory. This constraint allows the reference design to be implemented as an add-in card to any readily available processor board with a revision 2.1 compliant PCI bus. Up to four reference design cards can be interfaced to the processor board.
- Mechanical and electrical constraints for interfacing an add-in card to the processor board, as specified in revision 2.1 of the PCI local bus specification.

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The software interfaces to the FREEDM-8 via a host processor on the PCI bus and enables support of network protocol layers necessary to transmit and receive data packets of PVC. Software procedures are provided to illustrate the following:

- PCI device location and memory resource assignment
- Reset of the hardware via software
- Initialization of the hardware, software and the packet memory
- Activation/deactivation of the hardware
- Provisioning/unprovisioning of PVCs
- Transmit and receive packet processing
- Error handling
- Performance counters
- Diagnostics

The following software constraints have been included in this design:

- The FREEDM-8 data interfaces are the only interfaces the software has access to. The content of the user data field of the HDLC frame is not processed. Other upper layer functions such as congestion management, LMI protocol and multi-cast capability are not implemented.
- Source code is written in the C language. Executable code can run on i960 or Pentium based processor boards.

This Reference Design and Evaluation Card supports E1 and T1 data format that is hardware and/or software configurable within the same basic printed circuit board assembly.

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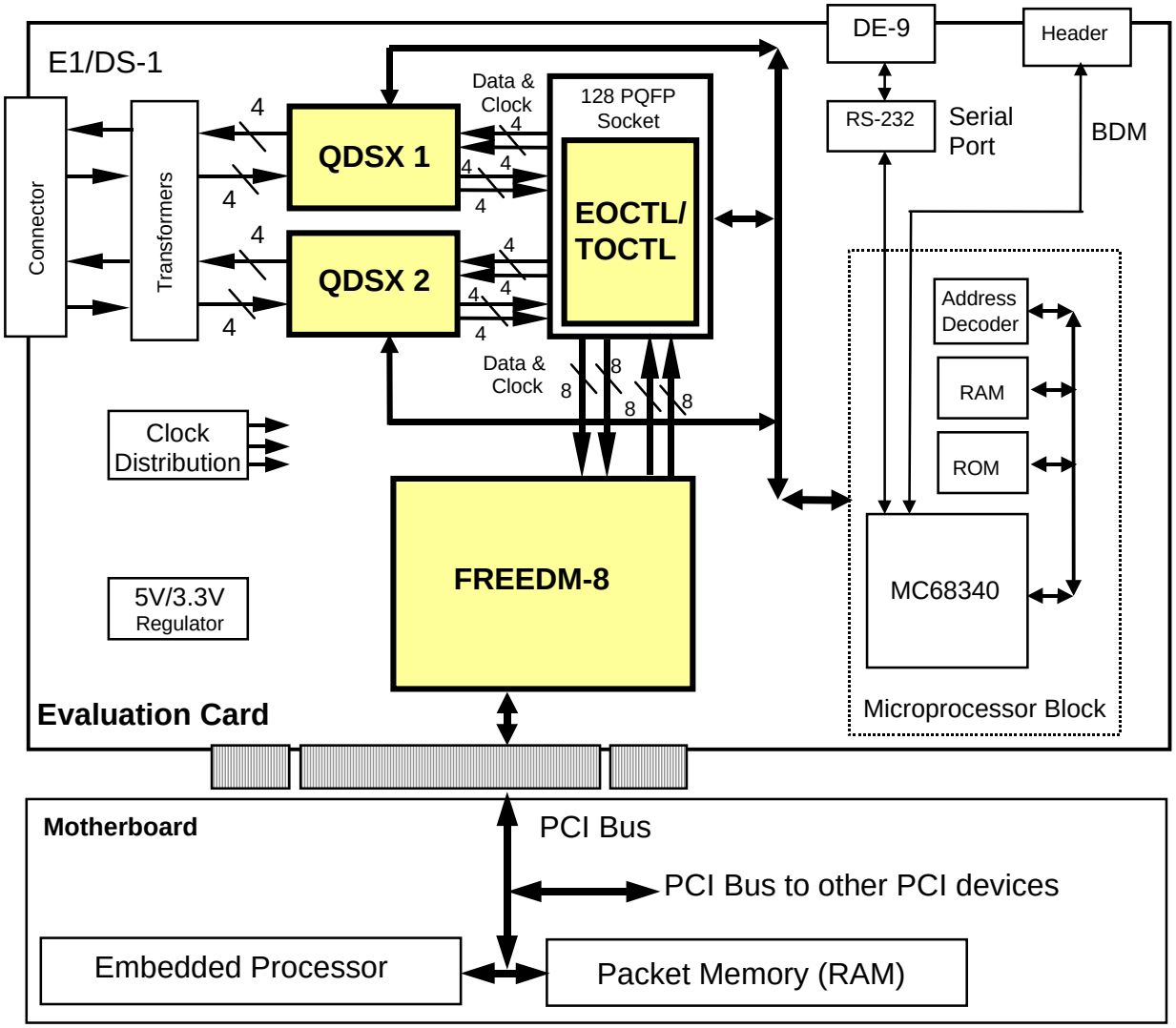
2 FUNCTIONAL DESCRIPTION

The following sections provide a functional description of the components mounted on the Board.

2.1 Block Diagram Drawing

FIGURE 2. Block Diagram



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2.2 Block Diagram Description

The Reference Design consists of the following blocks:

- **EOCTL** – E1 OCTaL Framer; single device containing eight E1 Framers;
- **TOCTL** – T1 OCTaL Framer; single device containing eight T1 Framers;
- **QDSX** – Quad DSX-1/E1 Line Interface; two devices each containing four E1/DS-1 line interfaces;
- **FREEDM** – FRame EnginE and Data Link Manager; single device interface to PCI Bus;
- Transformers and connectors – four dual bi-directional magnetics and connector supporting total of eight (8) bi-directional ports;
- Microprocessor – block contains Motorola's MC68340 processor, RAM, ROM, address decoder and supporting digital buffers and logic;
- Serial Ports – RS-232 and BDM; the RS-232 port allows control of the QDSX, EOCTL and Microprocessor during test. The BDM port allows faster software/firmware development;
- +5V to +3.3V linear voltage regulators.

The major devices such as EOCTL, TOCTL, QDSX and FREEDM-8 are described in more detail further in this document.

2.3 E1/DS-1 Connector Interface

One of the limitations imposed on the EOCTL/TOCTL Evaluation Card is a physical height dimension. The printed circuit board (PCB) is required to fit into a PC with a closed cover. This requirement in return limits the E1/DS-1 connector placement. A standard E1/DS-1 connector consists of two bantam concentric connectors. For this Reference Design a total of sixteen such connectors are required on the front-end of the card, and this is physically impossible. In this case an industry accepted solution is implemented. This consists of a multiple pin E1/DS-1 non-standard connector with attached short pieces of cables and bantam connectors. This connectorization is shown in FIGURE 3 below.

Bantam connectors (and cables) are paired for transmitter and receiver cables corresponding to the same E1/DS-1 line. A standard, DD-50 metal shell connector penetrates through the metal bracket attached to the Evaluation Card. The connector fits into a standard PC Card slot opening at the back of any PC. The mating cable/connector assembly is an integral part of the Evaluation Card.

A full metal body connector helps to keep EMI below FCC Cat B levels.

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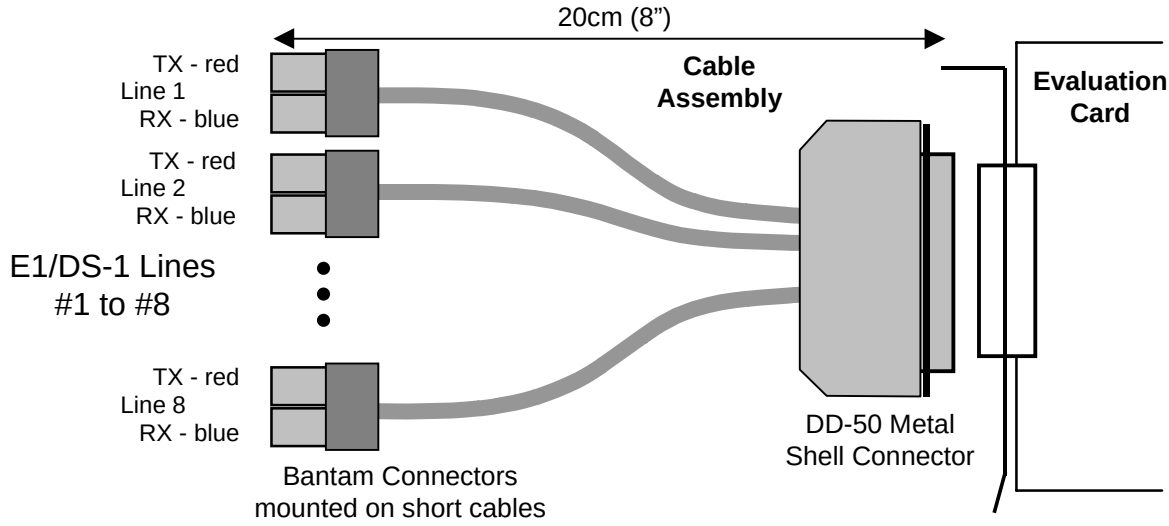
FIGURE 3. Cable Assembly for Eight E1/DS-1 Lines



Bantam connectors are individually wrapped with a colored (red/blue) heat-shrink tubing and then another piece of a heat-shrink tubing packages corresponding pair of transmitter and receiver lines.

The red color depicts transmitter and the blue one depicts receiver.

Electrical connections are shown in FIGURE 4 below.

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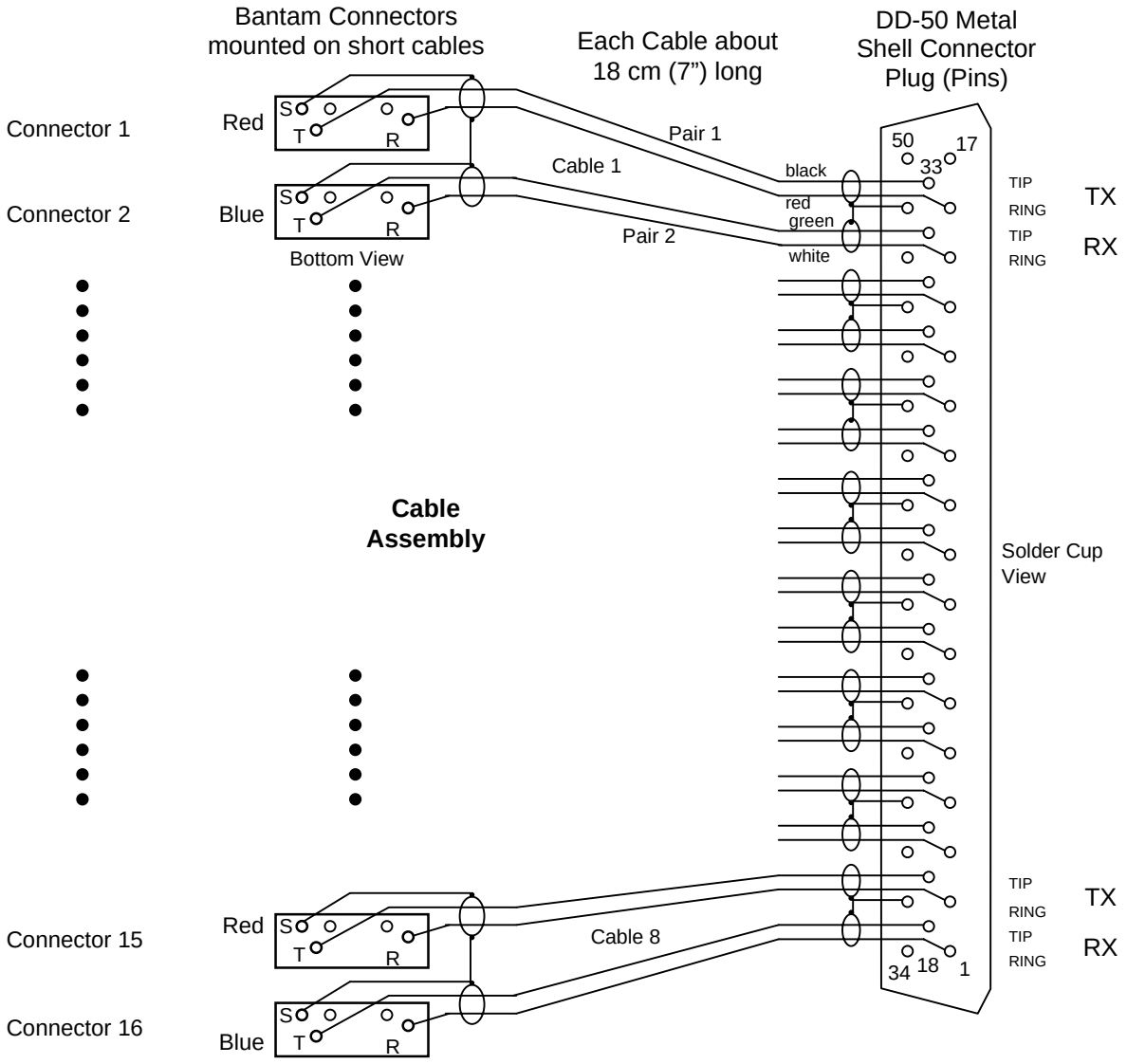
FIGURE 4. Electrical Connection of the DD-50 Connector Harness.



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2.4 Transformers and QDSX Line Interface

2.4.1 Receive Path

The E1/DS-1 receiver lines are interfaced to the QDSX (line transceivers) via transformers and resistive voltage divider pads. The interface is shown in FIGURE 5 below. To save on costs and board real estate multiple transformer packages are used. A total of four dual, bi-directional magnetics are assembled on the evaluation card.

Signals from transformers are fed into the first stage of the QDSX device, the Analog E1 Pulse Slicer, that is a part of the Receive Data Slicer (RSLC) block. The RSLC block provides the first stage of signal conditioning for the G.703 2048 kbit/s E1 (or 1544kbit/s DSX-1serial data stream by converting bipolar line signals to dual rail RZ pulses. The E1 signal is sliced at 50% (DSX-1 at 67%) of a peak amplitude.

The RSLC block relies on an external network for compliance to the E1 (DSX-1) input port specifications. The RSLC block needs an off-chip attenuator pad to operate in one of four modes: DSX-1 normal mode, DSX-1 bridging mode, E1 120Ω twisted pair mode and 75Ω coax mode.

Further details of the signal levels is discussed in section 3.3 “E1/DS-1 Receive Block” below.

The off-chip attenuator pad network is shown in FIGURE 5 below. The network values shown in the table are recommended for the specified applications:

TABLE 1. Receive Path Component Values.

	Format	Zo	R1 (Ω± 1%)	R2 (Ω± 1%)	Squelch Level at Primary (mV Typical)
	E1	120Ω	357	121	276
Not supported by Reference Design	E1	75Ω	205	95.3	220
	DSX-1 Normal	100Ω	309	93.1	227
Not supported by Reference Design	DSX-1 Bridging		0	402	50

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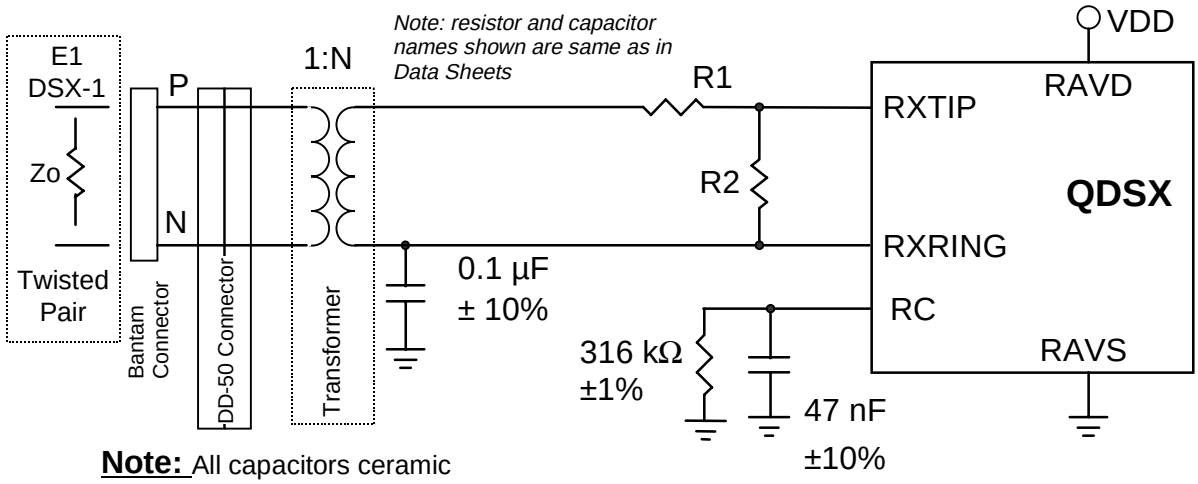
Tight tolerances are required on the resistors and turns ratio to meet the return loss specification.

FIGURE 5. External Analog Receive Interface Circuit.



Note: All capacitors ceramic

The Evaluation Card can support E1 **or** DSX-1 interface. The PCB Card has to have parts assembled to support only one of the standards at the time. No switches/headers are present on the board.

The transformer is designed for use in T1/CEPT/ISDN-PRI applications. Many manufacturers have standard products for these applications. Typical characteristics of a suitable transformer are given in the following table.

TABLE 2. E1/DS-1 Receive Transformer Characteristics

Turns Ratio	OCL (mH min.)	$C_{W/W}$ (pF max.)	L_L (µH max.)	DCR pri. (Ω max.)	DCR sec. (Ω max.)
1:2	1.20	35	0.80	0.80	1.2

where
OCL is the open-circuit inductance,
$C_{w/w}$ is the inter-winding capacitance,
L_L is the leakage inductance, and
DCR is the DC resistance.

PMC-Sierra has verified the operation of the RSLC functional block with the following transformers:

- Pulse Engineering PE64931 (1:1:1) and PE64952 (1:2CT)
- BH Electronics 500-1775 (1:1:1) and 500-1777 (1:2CT)

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Many manufacturers produce dual transformers containing the 1:2 and 1:1.36 turn ratio necessary for the receiver and transmitter circuits. PMC-Sierra has verified the operation of XPLS and RSLC with the following dual parts:

- Pulse Engineering PE64952
- Pulse Engineering PE65774 (for extended temperature range)
- BH Electronics500-1777

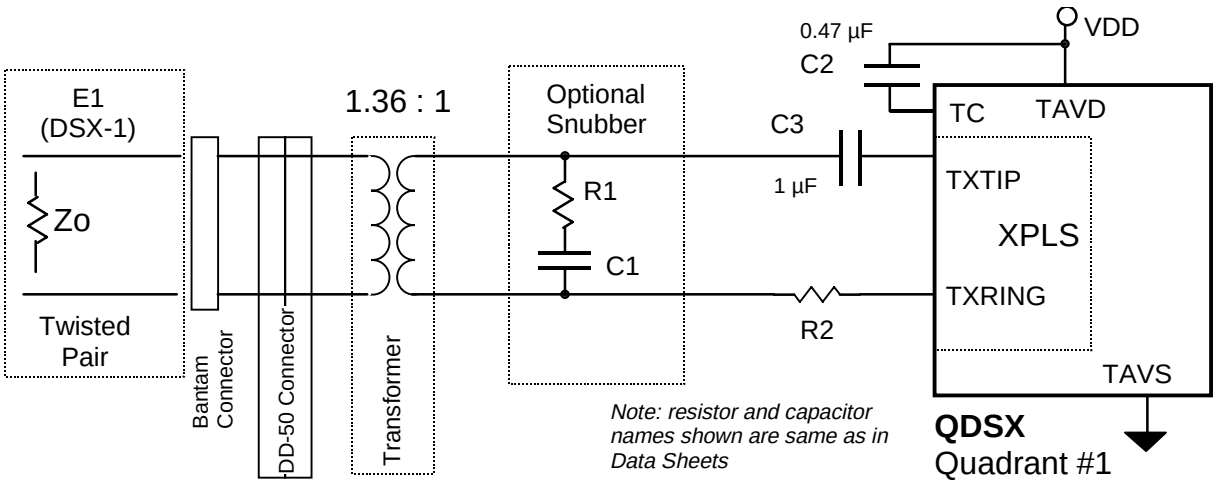
A quad transformer package T1008 is used in this reference design in order to provide efficient layout.

2.4.2 Transmit Path

The transmitter interface is shown in FIGURE 6 below. Transmit lines are interfaced from the QDSX to the E1/DS-1 lines via transformers. The serial capacitor prevents DC bias current flow through transformer windings.

The QDSX's internal line driver stage is the Transmit Pulse Generator (XPLS) block. This block outputs pulses specified by Recommendation G.703 at 2048 kbit/s (and 1544 kbit/s). The output pulse shape is synthesized digitally from user-programmed template settings with an internal Digital to Analog (D/A) converter. The signal is presented on the TXTIP[1:4] and TXRING[1:4] outputs.

FIGURE 6. External Analog Transmit Interface Circuit



The step-up transformer "amplifies" the output pulses to their final line interface levels.

A high-frequency negative-going spike may be observed on the falling edge of the transmit pulse. The optional "snubbing" network shown in FIGURE 6 can be used

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to filter out this spike. Test performed on the evaluation card shows a need for a snubber circuit for all length of the twisted pair.

TABLE 3. E1 Transmitter Interface Component Values

	Format	Zo	R1 (optional snubber)	R2	C1	C2	C3
	E1	120Ω	47Ω ±10%	18Ω ±5%, 1/8W	1000pF ±10%	0.47uF ±10%	1uF ±10%, 50V
Not supported by Reference Design	**E1**	75Ω	47Ω ±10%	6.2Ω ±5%, 1/8W	1000pF ±10%	0.47uF ±10%	1uF ±10%, 50V
	DSX-1	100Ω	22Ω ±10%	0Ω	10000pF ±10%	0.47uF ±10%	1uF ±10%, 50V

The R2 resistor value, shown in table above, differs from the standard data sheet value. That may be related to a new type of transformer (T008) and a specific cable interface (DD-50 connector) used for this reference design.

Resistor R2 in conjunction with snubber R1/C1 can control overshoot. This reference design requires a permanent snubber as specified in the table above and R2 at 18Ωon the E1 board. DSX1 interfaces use R2 at 0Ω Designers should verify compliance of the E1/DSX-1 waveform with appropriate templates by adjusting values of the R2 resistor and use of a snubber.

The evaluation card supports both E1 and DSX-1 interfaces, and the PCB Card has to be configured at assembly to support the desired mode of operation. No switches/headers are present on the board to reconfigure the line interface.

The line interface transformer should be designed for use in T1/CEPT/ISDN-PRI applications. Many manufacturers have standard products for these applications. Typical characteristics of a suitable transformer are given in the following table.

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TABLE 4. E1 Transmit Transformer Characteristics

Turns Ratio	OCL (mH min.)	$C_{w/w}$ (pF max.)	L_L (µH max.)	DCR pri. (Ω max.)	DCR sec. (Ω max.)
1:1.36	1.20	35	0.80	0.80	1.2

Where OCL is the open-circuit inductance,

$C_{w/w}$ is the inter-winding capacitance,

L_L is the leakage inductance, and

DCR is the DC resistance.

PMC-Sierra has verified the operation of the XPLS functional block with the following 1:1.36 transformers:

- Pulse Engineering PE64937 (1:1.36)
- Pulse Engineering PE65340 (1:1.36) (for extended temperature range)
- BH Electronics 500-1776 (1:1.36)

There are many manufacturers making dual transformers on the market. Hybrid packages contain 1:2 and 1:1.36 transformers necessary for the receiver and transmitter circuits. PMC-Sierra has verified the operation of XPLS and RSLC with the following dual parts:

- Pulse Engineering PE64952
- Pulse Engineering PE65774 (for extended temperature range)
- BH Electronics500-1777.

To save on cost and board real estate a multiple transformer package is used. A total of four dual, bi-directional magnetics are assembled on the card.

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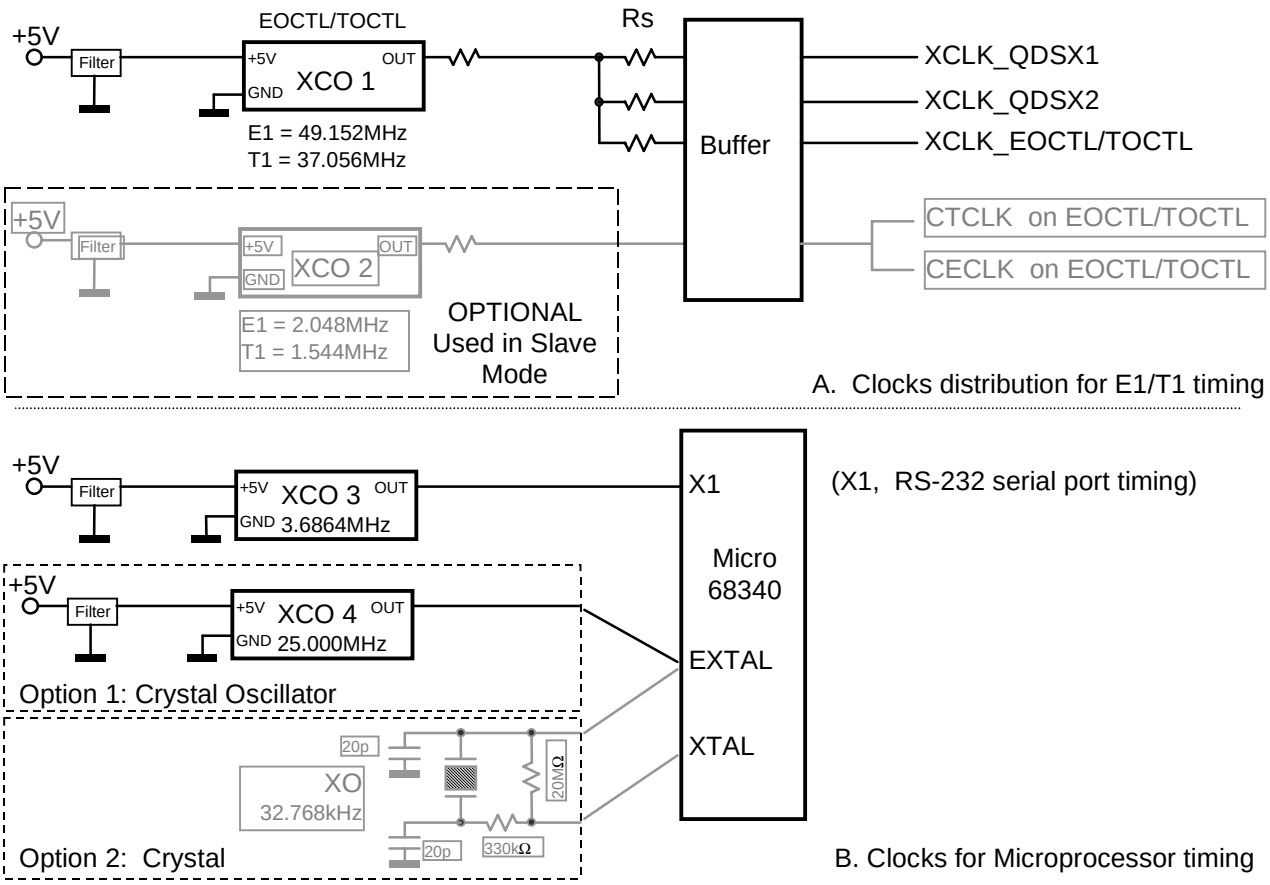
2.5 Clock Distribution

The Reference Design employs crystal oscillators to provide stable clock timing for transmitted E1/T1 data. The clock distribution block diagram is presented in FIGURE 7 below.

FIGURE 7. Clock Distribution on Evaluation Card



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2.5.1 E1/T1 Timing

The crystal oscillator XCO1, shown in FIGURE 7 above, provides timing for EOCTL/TOCTL and QDSX devices. The EOCTL/TOCTL device on this reference design is set to a Master Clock Mode and requires only a single clock at the XCLK input. The line clock is derived from the XCLK by dividing it down by 24. A 50 ppm frequency tolerance is required to meet Recommendation G.703. Therefore, the following oscillators are used:

- E1 – 49.152MHz ±50 ppm (parts per million);
- T1 – 37.056MHz ±50 ppm (parts per million).

In a Slave Clock Mode the EOCTL/TOCTL requires line rate clock input on its CTCLK/CECLK inputs. This is shown with shaded lanes in the above diagram.

Each crystal oscillator is powered through a low pass filter to minimize EMI radiation and/or interference to other blocks on the Reference Design circuitry. More on power supply filtering can be found in section 9.1.4 below.

2.5.2 Microprocessor Clocks

The microprocessor requires two clock signals to operate as shown in FIGURE 7 above.

The main clock can be fed from an external crystal oscillator or it can be synthesized using a low-cost crystal and internal PLL. This reference design has the 25MHz clock supplied from an external crystal HCMOS oscillator (XCO4). The crystal option (and internal PLL) is desired for a cost-sensitive design.

The second clock signal is used for the RS-232 serial port timing. That signal is fed from a crystal oscillator XCO3 at 3.6864 ±100ppm.

2.6 LED Indicators

The Reference Design employs green and red LEDs for a visual indication of some parameters. A simplified block diagram shown in FIGURE 8 below depicts the LED's functions.

2.6.1 Power Indicators

The green LEDs are used to signal the presence of +5V and +3.3V. The LED D3 is dedicated to +5V. It turns on if "+5V" line exceeds +2.2V. The LED D5 turns on

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if the “+3.3V” line exceeds +2.5V. Those LEDs are used to show that power is being supplied to the board.

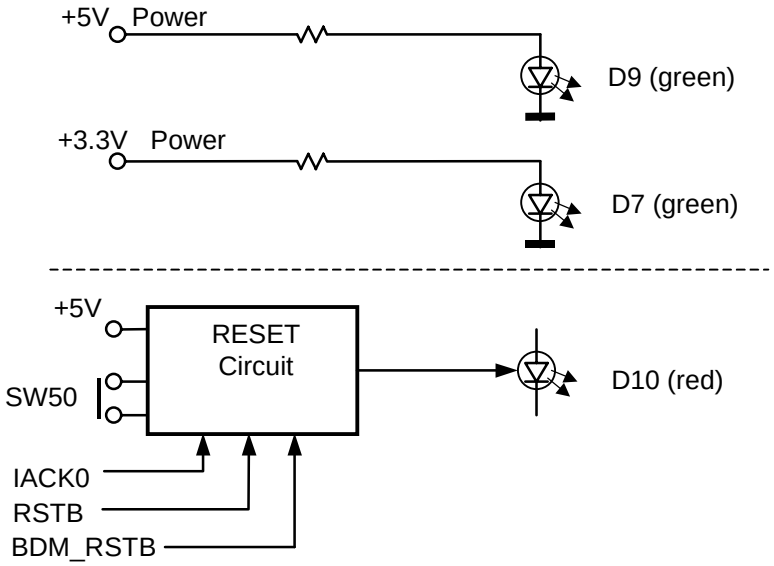
2.6.2 Reset Indicator

The red LED D10 is associated with the RESET circuit. D10 signals logic low on RSTB line. This line resets the Microprocessor, QDSX and EOCTL/TOCTL devices.

The Reset indicator is activated on five conditions:

- on power up while capacitor C1 is charged
- when push-button switch SW50 is activated
- if microprocessor sets IACK0 line “low” (“0”)
- if microprocessor activates RSTB by pulling it “low”
- on reset from an external BDM interface.

FIGURE 8. Led Indicators.



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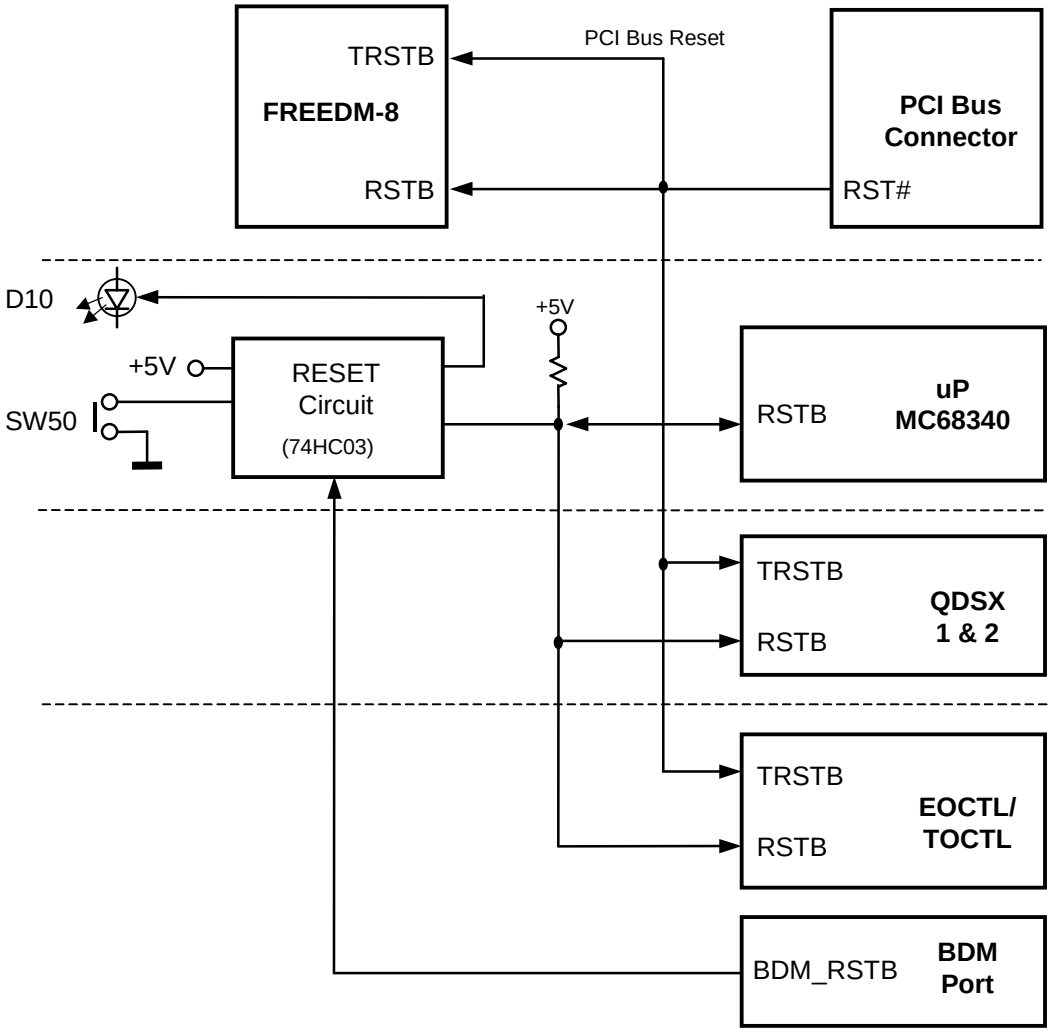
2.7 Reset Circuit

The reset circuit block diagram, used for this Reference Design, is shown in FIGURE 9 below. Each block is described in subsequent sections.

FIGURE 9. Reset Circuit.



2.7.1 PCI Bus Reset

The PCI Bus connector provides an active low RST# reset line. This line is used as a main reset for the FREEDM-8 device and as a boundary scan reset for FREEDM-8, QDSX and EOCTL/TOCTL devices (TRSTB). The Microprocessor can not be reset with this line.

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An option for a manual reset is not available on the Evaluation Card.

The RST# reset line is active on system power-up and/or per PCI Bus interface requirement.

2.7.2 Microprocessor Reset Line RSTB

The microprocessor reset RSTB is active low. This interface is an input/output on the MC68340. The RSTB signal can be generated with the reset circuit or by the microprocessor itself (software reset). The reset circuit employs an open drain 47HC03 device and that allows connecting two active outputs together. A pull-up resistor is required.

A push-button switch SW50 is used for manual reset of all devices connected to the RSTB\I net (Microprocessor, QDSXs, and EOCTL/TOCTL). The BDM port, connected through a NAND gate, can also generate reset.

When the RSTB line is asserted by software or hardware means (active low), a red LED D10 turns on to display the reset status present on the board.

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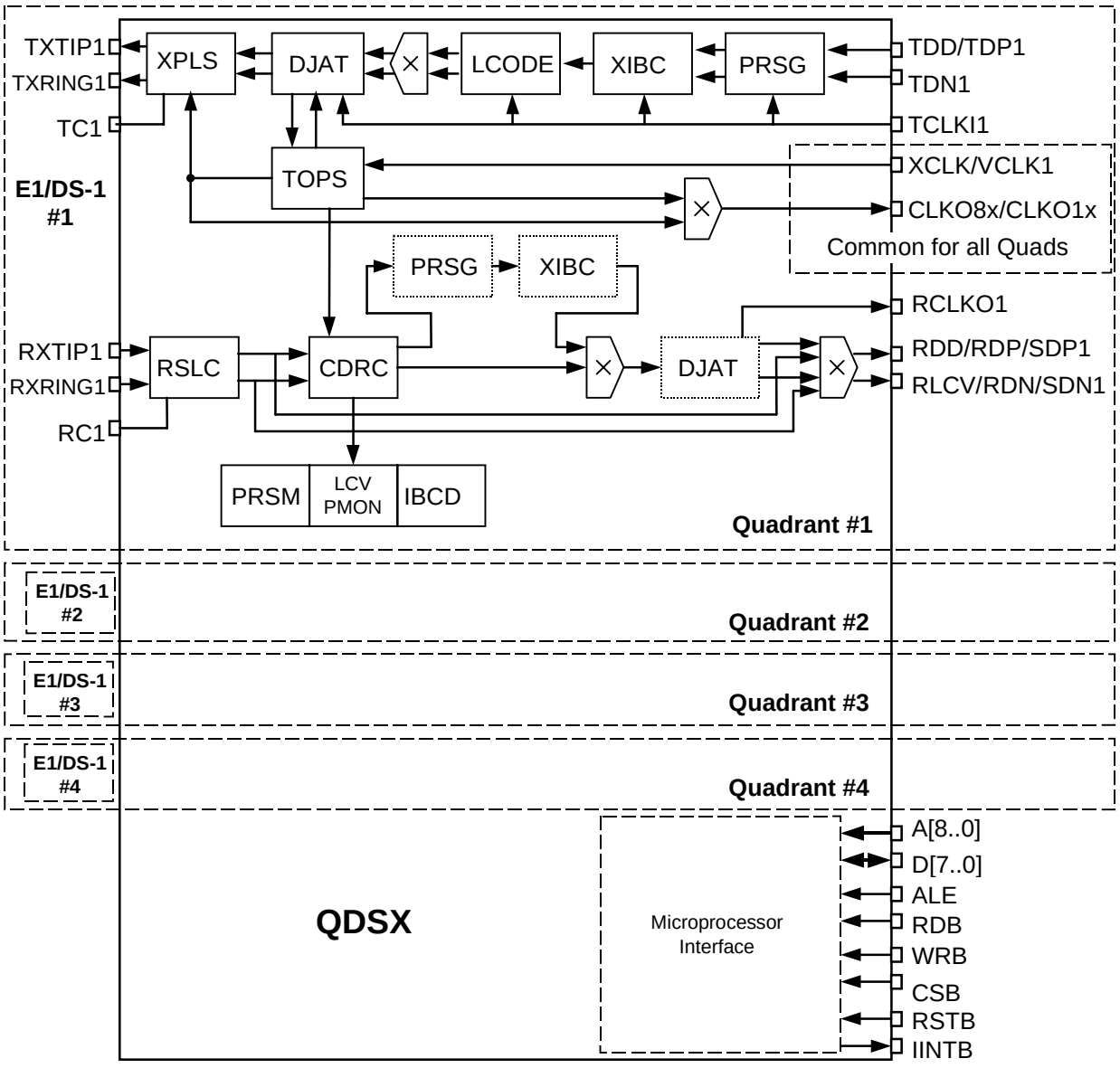
3 QDSX DEVICE DESCRIPTION

The PM4314 QDSX Quad T1/E1 Line Interface Device is a monolithic integrated circuit supporting G.704-compatible transmit and receive interfaces for four 2048 kbit/s E1 data streams or four 1544kb/s T1 data streams. Two QDSX devices are assembled on the Evaluation Board.

3.1 QDSX Block Diagram

FIGURE 10. Block Diagram



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3.2 E1/DS-1 Transmit Block

3.2.1 Transmit Interface

The TXTIP and TXRING are the output pins for the Transmit Pulse Generator (XPLS) block. This block functions as the Analog Pulse Generator converting NRZ signals into line signals suitable for use in a G.703 intra-office environment.

A logical "1" on the positive NRZ input to XPLS causes a positive pulse to be transmitted on an E1/DS-1 line. A logical "1" signal on the negative NRZ input to XPLS causes a negative pulse to be transmitted on a E1/DS-1 line. If both positive and negative NRZ inputs to XPLS are logical "0" or "1," no output pulse is transmitted.

The output wave shape is synthesized digitally from a user programmed template with an internal digital-to-analog (D/A) converter. A 4-bit (16 levels) D/A converter is updated eight times per period with programmed words. These words define the output pulse shape. Recommended codes for CEPT E1 120 Ω and DS-1 110 Ω symmetrical lines are given in the Operations section of the Data Sheet [1]. If an external circuit differs from the recommended one, the pulse generator permits creation of custom pulse shapes. Again refer to the Data Sheet [1] operations section for details. An example of a pulse generation is shown in FIGURE 12 below.

Each quadrant Transmitter has dedicated power supply pins as shown in FIGURE 11 below. The TAVD[1:4] are +5V lines fed via dedicated filters. Care must be taken to avoid coupling noise between quadrants and from transmitter to receiver on the same quadrant. Therefore RC elements are used to prevent power rail noise propagatiion to/from different circuitry on the Evaluation Card. The 0.01 uF capacitors must be placed as close as possible to the corresponding TAVD[1:4] and TAVS[1:4] pins. The 0.47uF capacitor is used to decouple the internal reference generator and must be connected from the TC[1:4] pin to the 0.01 uF filtering capacitor and corresponding TAVD[4:1]. A serial inductor and a resistor provide attenuation of supply current noise. Resistor RR1/TR1 and the 0.01/10 uF capacitors provide interference attenuation. Resistor value for TR1 can be calculated to have voltage drop of no more than 50 mV to prevent supply voltage mismatch.

The tantalum capacitor and the serial resistor help to meet the requirements stated in the data sheet [1]: *“Analog power supplies must be applied after both VDDI[3:1] and VDDO[6:1] have been applied or they must be current limited to less than the maximum latchup current specification (100 mA). In normal operation the differential voltage measured between the TAVD[4:1] and RAVD[4:1]*

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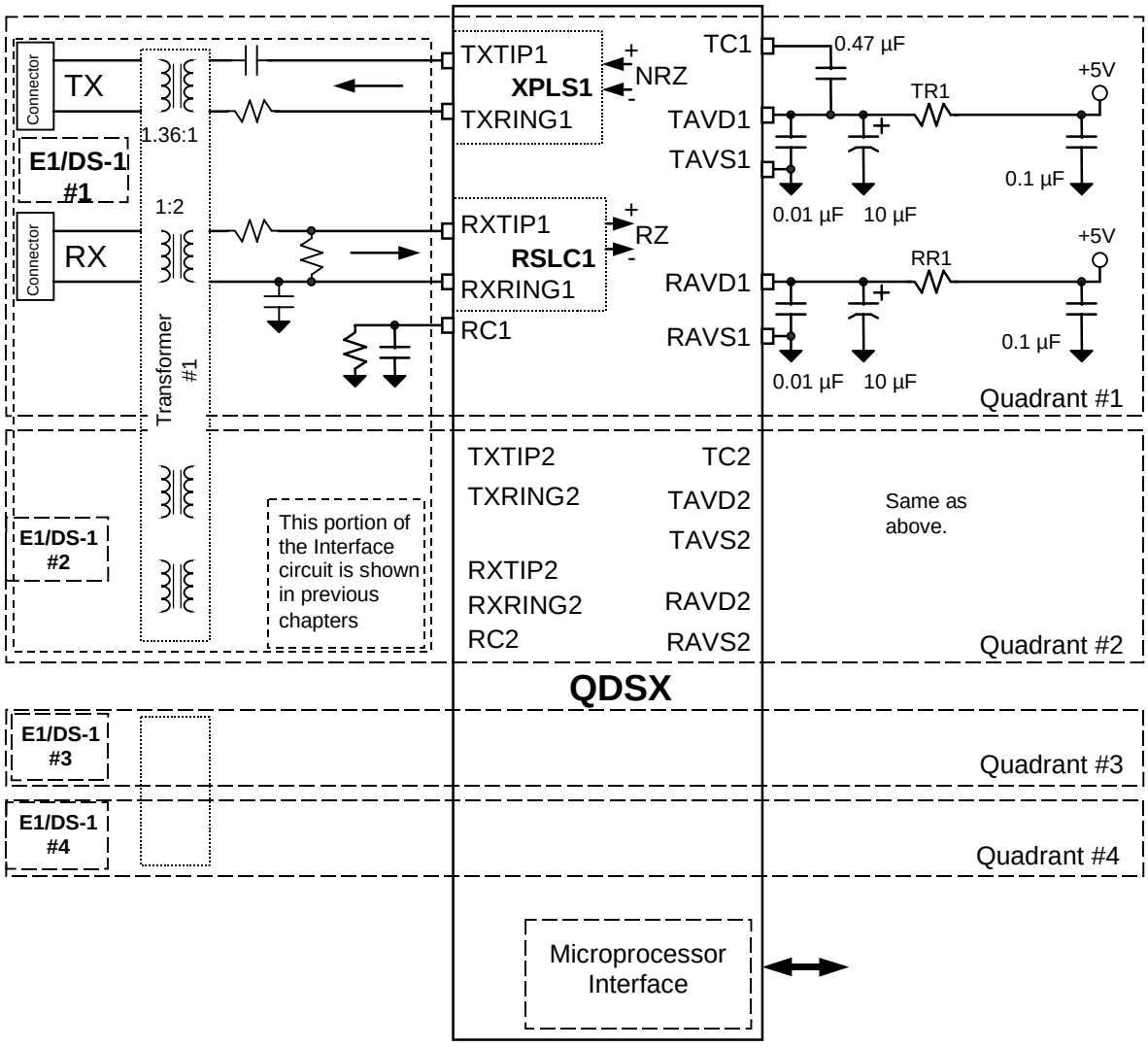
supplies and the VDDI[3:1] and VDDO[6:1] supplies must be less than 0.5 volt. The relative power sequencing of TAVD[4:1] and RAVD[4:1] power supplies is not important."

Ground pins TAVS[1:4] must be connected immediately to the ground plane with traces as short as possible in order to keep inductive effects low.

FIGURE 11. E1/DS-1 Interface of QDSX Device



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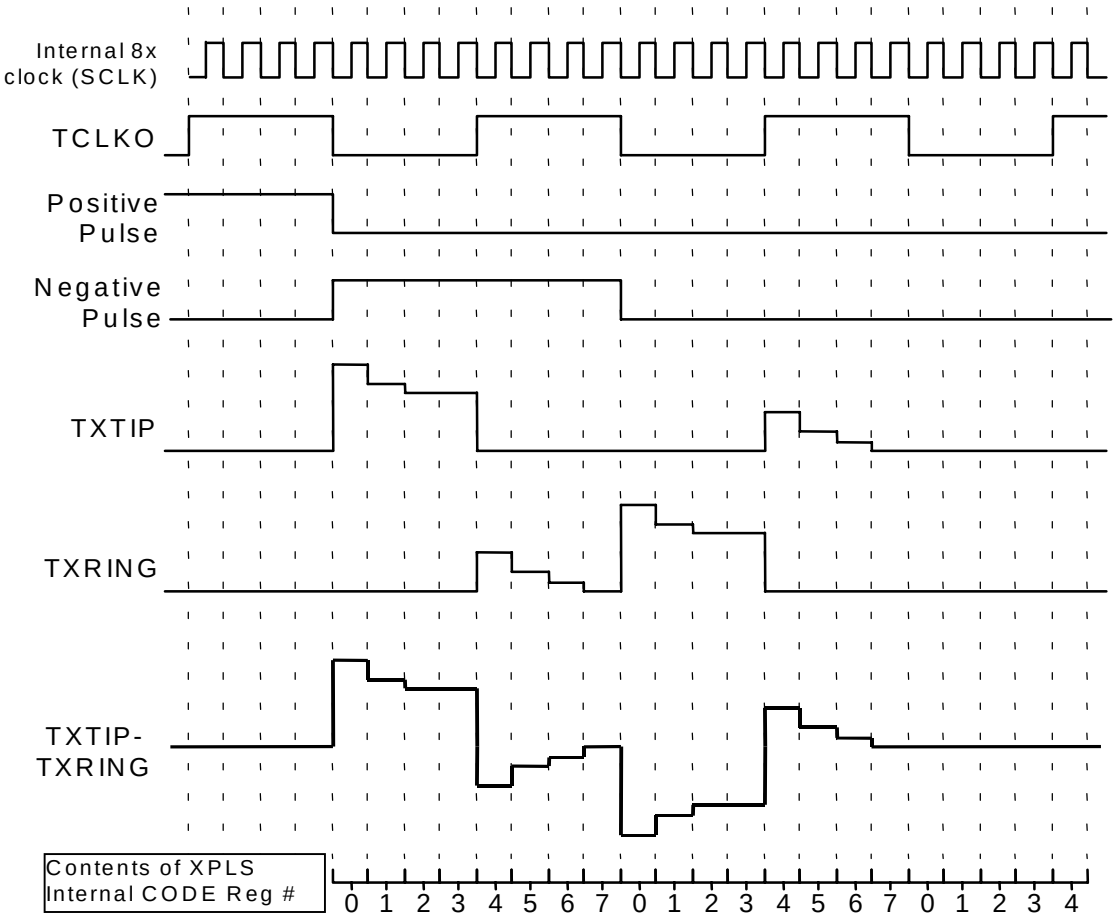
3.2.2 Programming the XPLS Waveform Template

An example of a DS-1 output waveform is presented in FIGURE 12 below.

FIGURE 12. Transmit Pulse Generation for DS-1 Mode



The highlighted curve above shows that the pulse-shape is not intuitive and is built with a complex algorithm. The final waveform produced depends on transformer and associated components, as shown in FIGURE 6 in the previous chapter.

The Data Sheet [1] in chapter “OPERATIONS” (page 100) show recommended values for the D/A converter (driver). Register 02CH (06CH, 0ACH and 0ECH) Bit7 RPT sets the default values. However, in some cases, transmitted wave-shape may not meet the ANSI template for DS1 and E1. In this instances the values specific to the layout, employed transformers, connectors and cable harness must be determined. For the reference design this has been verified through a test and is shown in the table below.

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TABLE 5. Transmit XPLS Code (for meeting ANSI DS-1/E1 template).

	Length Setting [ft]	Recommended Code Register Values with WIDEN = 1							
		Register Number							
		0	1	2	3	4	5	6	7
DS-1 With the serial resistor at 0Ω and snubber	0 – 110	9	9	9	9	1	1	1	0
	110 – 220	A	9	9	9	2	3	1	1
	220 – 330	C	A	A	A	3	3	1	1
	330 – 440	D	B	A	A	4	3	2	1
	440 – 550	E	B	B	A	6	3	3	1
	550 – 660	F	C	B	B	7	4	3	1
E-1 With the serial resistor at 18Ω and snubber in place	All length G.703 2048 kb/s	B	B	B	B	0	0	0	0

NOTE: on the TOCTL version of the evaluation card the QDSX devices have default setting on power-up at 0 – 110 feet cable length. Other cable length can be programmed through a serial port.

It was confirmed through a test that the DS-1 transmit circuit requires snubber circuit to be assembled to meet ANSI T1.102 (and ANSI T1.403 (1989)) DSX-1 template.

The waveforms corresponding to each cable length settings, shown in TABLE 5 above, are presented below in FIGURE 13, FIGURE 14, FIGURE 15, FIGURE 16, FIGURE 17 and FIGURE 18. Each figure has two waves superimposed to show waveform at the minimum and maximum length (DSX-1) of a cable for each cable setting.

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FIGURE 13. DSX-1 Waveforms at 0 Feet (A) and 110 Feet (B) with XPLS setting at 0-110 feet.

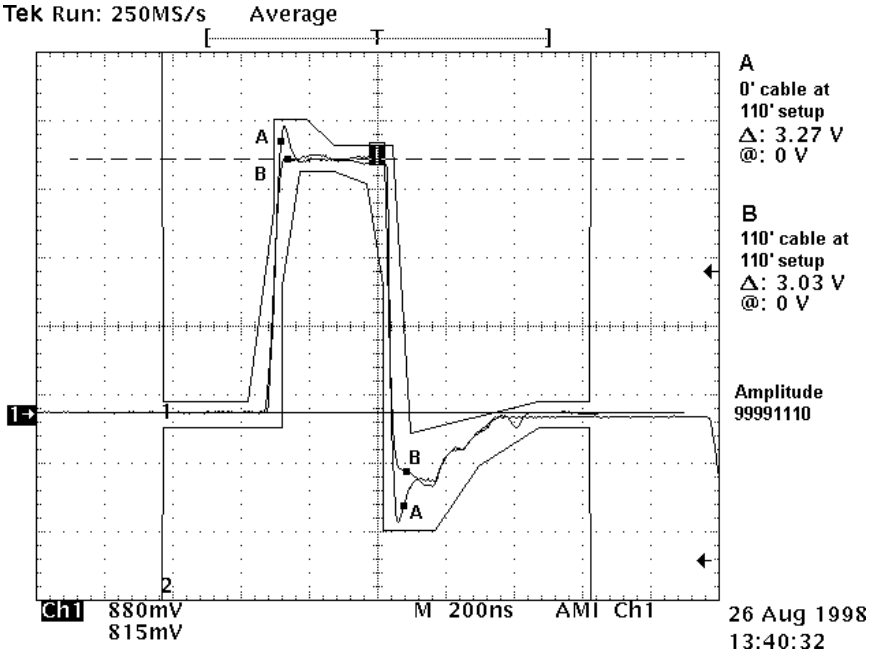

FIGURE 14. DSX-1 Waveforms at 110 Feet (A) and 220 Feet (B) with XPLS setting at 110-220 feet.

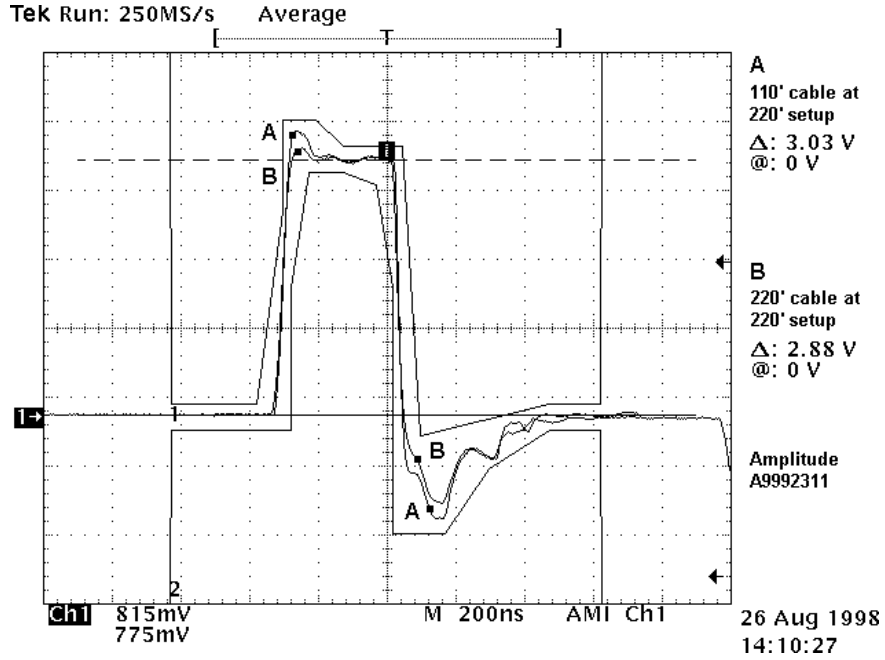

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FIGURE 15. DSX-1 Waveforms at 220 Feet (A) and 330 Feet (B) with XPLS setting at 220-330 feet.

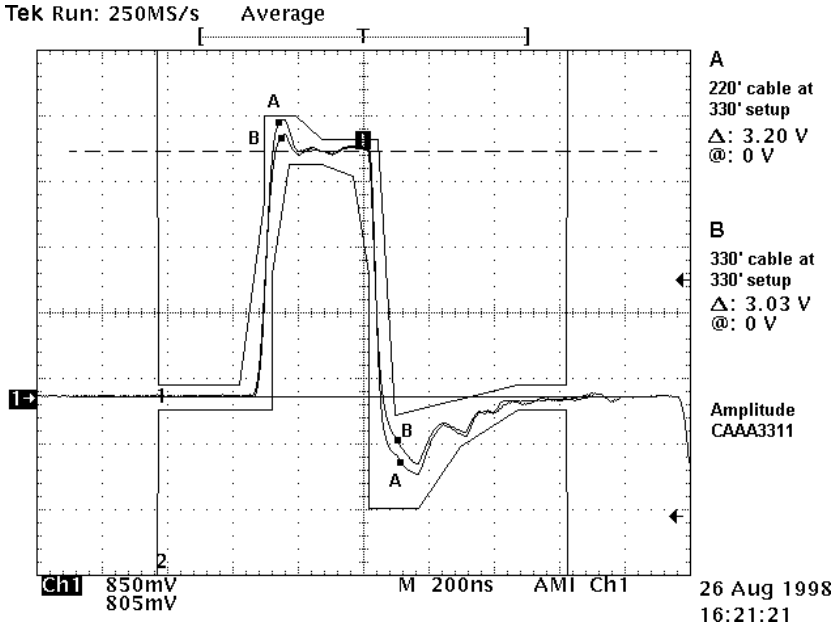

FIGURE 16. DSX-1 Waveforms at 330 Feet (A) and 440 Feet (B) with XPLS setting at 330-440 feet.

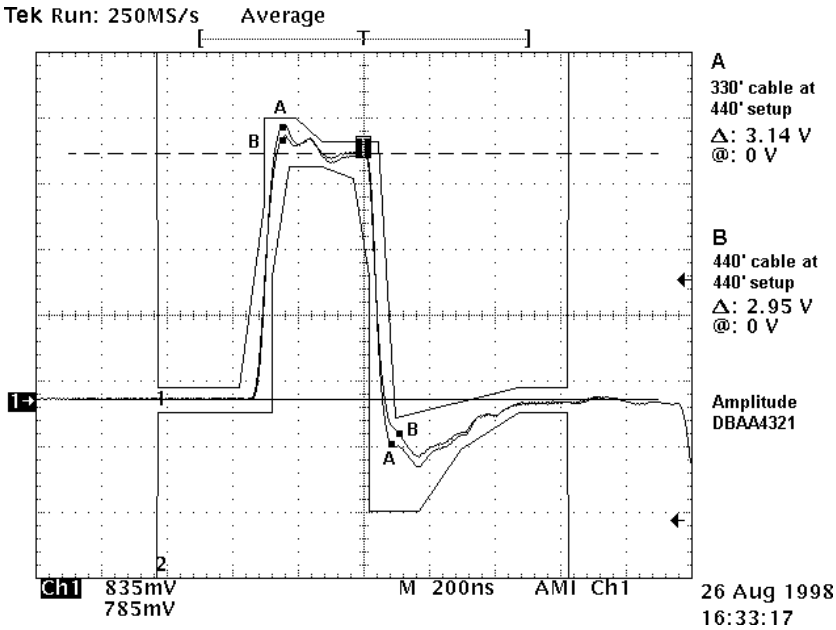

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FIGURE 17. DSX-1 Waveforms at 440 Feet (A) and 550 Feet (B) with XPLS setting at 440-550 feet.

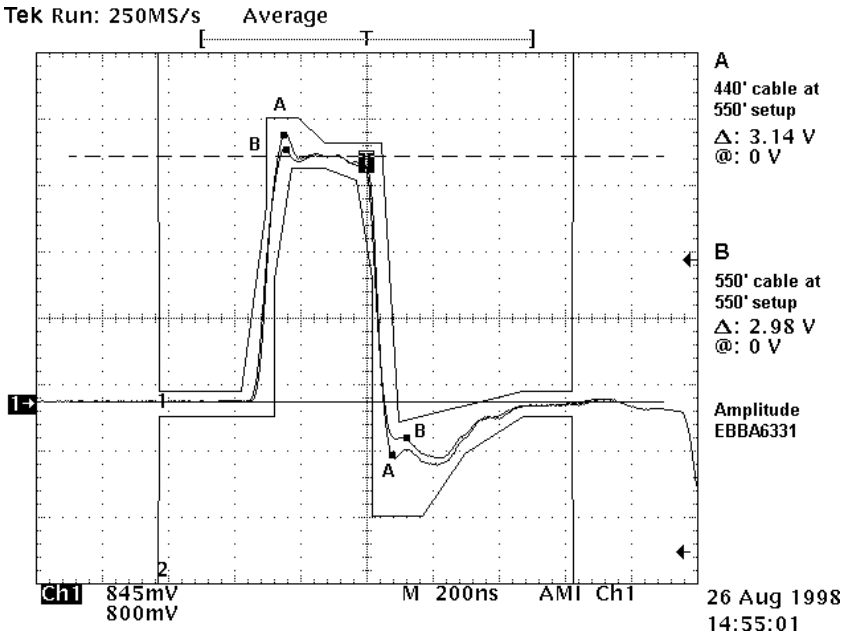

FIGURE 18. DSX-1 Waveforms at 550 Feet (A) and 660 Feet (B) with XPLS setting at 550-660 feet.

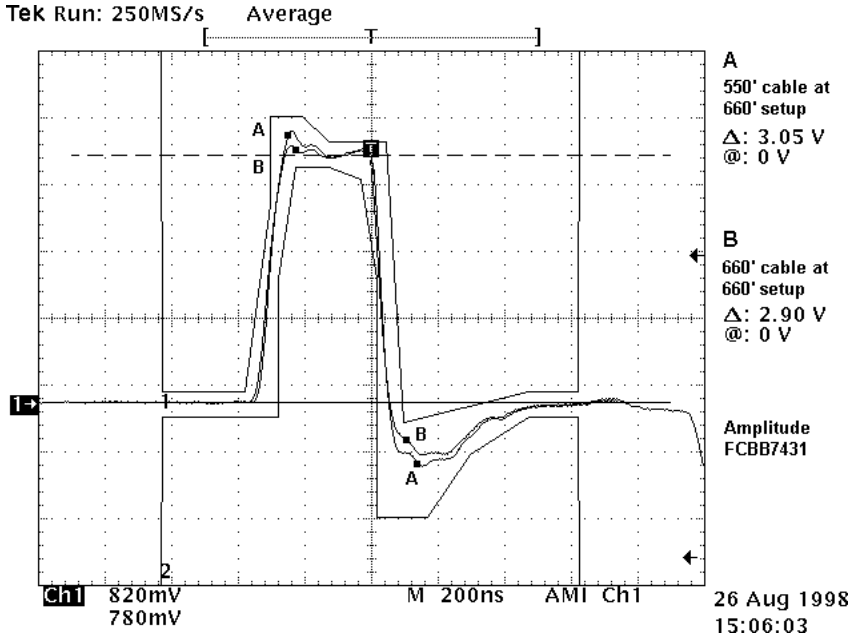

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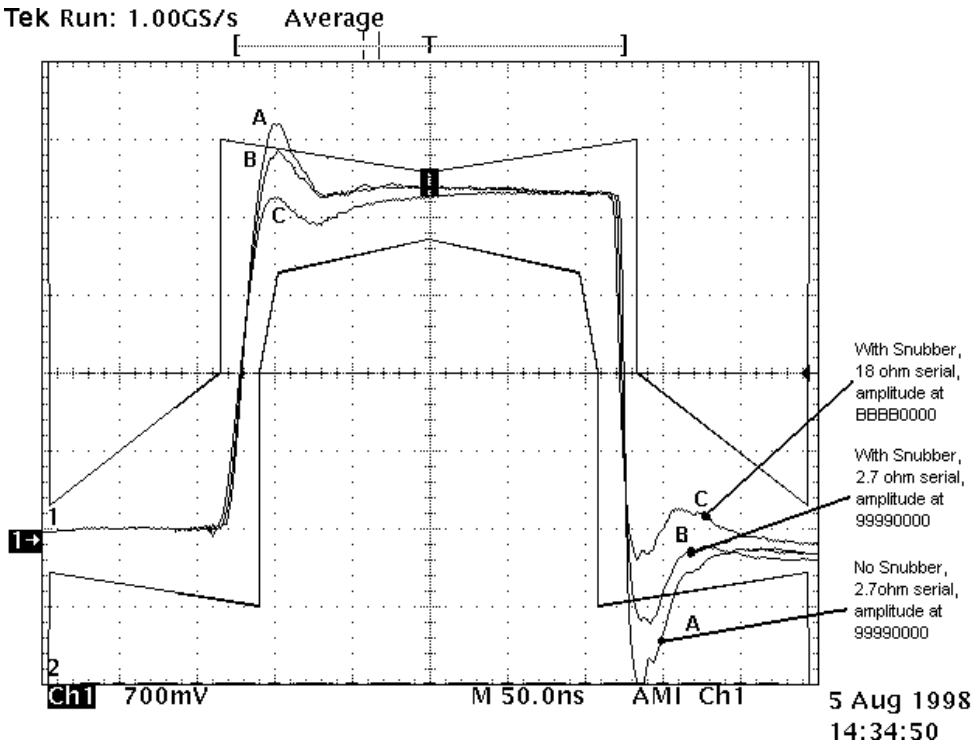
FIGURE 19. E1 Waveforms.



Three waveforms for E1 transmitter are superimposed and are shown in FIGURE 19 below. Waveform A shows an E1 signal without a snubber and the serial resistor at 2.7 ohm (as recommended in [1]). Waveform B shows signal with the snubber in place and a serial resistor of 2.7 ohm. Waveform C shows a transmitted signal with the snubber in place and the serial resistor of 18 ohm. The amplitude of the C waveform was set to BBBB0000 to compensate for signal loss associated with a higher value of the serial resistor.

It is clearly visible that curves A and B do not fit into the E1 template. Waveform C meets the requirement. The waveform C passed the CTR-4 Layer1 test at TUV Telcom Services, Inc.

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3.3 E1/DS-1 Receive Block

The RXTIP and RXRING are the inputs to the Analog Pulse Slicer (RSCL) block. This is the first stage of the QDSX signal conditioning. A bipolar G.703 serial data stream is converted to dual rail RZ pulses.

In 120Ω E1 mode, the amplitude of a received pulse at the 1:2 line-coupling transformer's primary can be in the range from 3.3V to 1.4V (depending on the length of the cable from the signal source). In this mode, the QDSX can receive signal levels down to a typical squelching level of 276mV, which means that there is 14.1 dB margin between the minimum expected signal level and the typical minimum receivable signal level.

In 75Ω E1 mode, the amplitude of a received pulse at the 1:2 line-coupling transformer's primary can be in the range from 2.6V to 1.1V (depending on the length of the cable from the signal source). In this mode, the QDSX can receive signal levels down to a squelching level of 220mV which means that there is a 14.0 dB margin between the minimum expected signal level and the minimum receivable signal level in the worst case.

The RSLC block provides a squelching circuit, which indicates an alarm when input pulses are below the squelching level threshold. In this state, data is not sliced, which prevents the detection of noise on an idle transmission line. The “low level” signal condition or “signal squelch” may be enabled to generate interrupts. Clock and data are recovered from the dual rail RZ digital pulses using a digital phase-locked loop that provides excellent high frequency jitter tolerance. The recovered data is decoded using B8ZS line code rules. Loss of signal and line code violations are detected as well as excessive zeros, and B8ZS signatures. These various events or changes in status may be enabled to generate interrupts. Additionally, loss of signal and line code violations is also indicated on outputs. The SQ status bit in the RSLC Interrupt Enable/Status registers (031H, 071H, 0B1H, and 0F1H) goes high whenever the RSLC block is squelching the input signal. The RSLC can be configured to generate an interrupt whenever the SQ status bit changes state.

Each quadrant Receiver has dedicated power supply pins. The RAVD[1:4] are the +5V lines fed via dedicated filters. Care must be taken to avoid coupling noise between quadrants and from transmitter to receiver on the same quadrant. Therefore RC elements are used to prevent power rail noise propagation to/from different circuitry on the Evaluation Card. The 0.01 uF capacitors must be placed as close as possible to the RAVD[1:4] and RAVS[1:4] pins. A serial inductor and a resistor provide attenuation of supply current noise. Resistor TR1 and 10uF (SMD tantalum) capacitor provide attenuation at low frequency. The RL1 inductor and

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0.01/10 uF capacitors provide attenuation at high frequency. Resistor value for RR1 can be calculated to have a voltage drop of no more than 50 mV to prevent supply voltage mismatch.

The tantalum capacitor and the serial resistor help to meet requirement stated in data sheet [1]: *"Analog power supplies must be applied after both VDDI[1:3] and VDDO[1:6] have been applied or they must be current limited to less than the maximum latchup current specification, (100 mA). In normal operation the differential voltage measured between TAVD[1:4] and RAVD[1:5] supplies and VDDI[1:3] and VDDO[6:1] must be less than 0.5 volt. The relative power sequencing of TAVD[1:4] and RAVD[1:4] power supplies is not important."*

Ground pins RAVS[1:4] must be connected immediately to the ground plane with traces as short as possible.

3.4 Drop Side Interface

The drop side interface (backplane) provides data and clock for both directions of the E1/T1 interface. In the transmit direction three data lines are interfaced:

- TDD/TDP - Transmit Data in a single rail mode or Positive Transmit Data in dual-rail mode.
- TDN - Negative Transmit Data in a dual-rail mode.
- TCLKI - Transmit Clock Input, 2.048 MHz for E1 (1.544 MHz for T1).

In the receive direction data is output on three lines:

- RDD/RDP - Receive Data in a single rail mode or positive receive data in dual-rail mode.
- RDN - Negative Transmit Rail in a dual-rail mode.
- RCLKO - Receive Clock Output, 2.048 MHz for E1 (1.544 MHz for T1).

There are two additional clock line interfaces:

- High-speed XCLK clock is the timing reference required by many portions of the QDSX. XCLK is nominally a 24 x 2.048 MHz = 49.152 MHz for E1 or 37.056 MHz for T1. When jitter attenuation is not required, an 8x clock can drive XCLK at 16.384 MHz for E1 or 12.352 MHz for T1.

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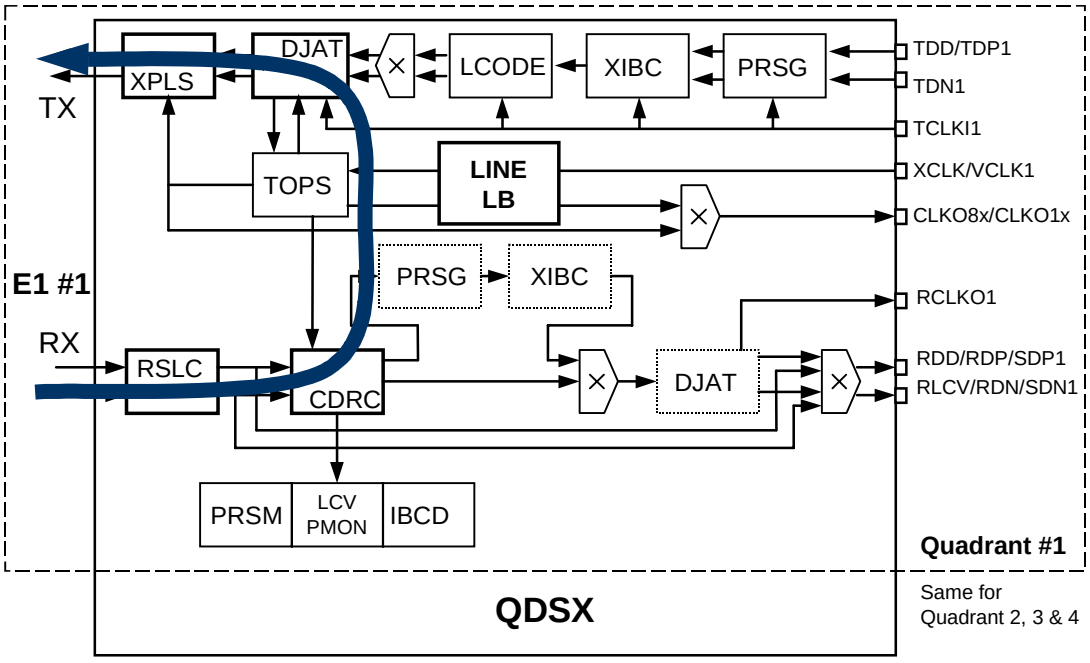
- The other clock interface is the CLKO8x/CLKO1x. This output has two modes of operation. The first one provides a divide by three the 24x clock. In the second mode, when an 8x clock is input to XCLK, this pin outputs a divide by eight clock. This baseband E1 clock can be used to drive all four quadrants in synchronous mode by feeding this signal parallel to all TCLK[1:4].

3.5 Loopback Options

The QDSX provides three modes of loopbacks. Loopback paths are shown in FIGURE 20, FIGURE 21and FIGURE 22 below. Only the first quadrant of the QDSX is shown for simplicity.

FIGURE 20. QDSX Line Loopback Mode



The Line Loopback provides diagnostic capabilities for the E1 line interface side. In this case the signal is sliced (RSLC), reclocked (CDRC) and run through a jitter attenuator (DJAT) before being looped back (XPLS). Detecting loopback code in an incoming E1 data stream can activate this loopback also.

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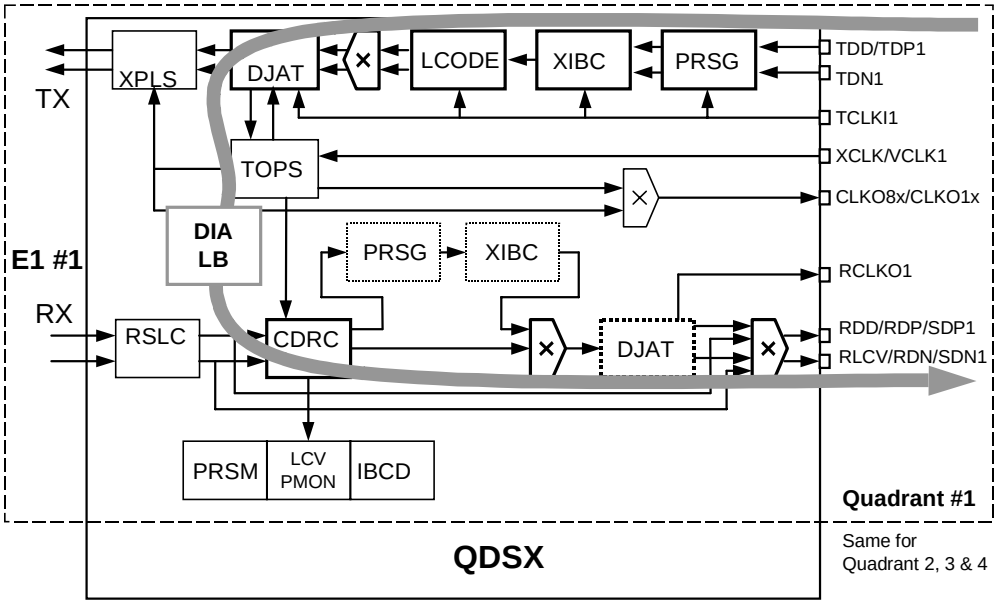
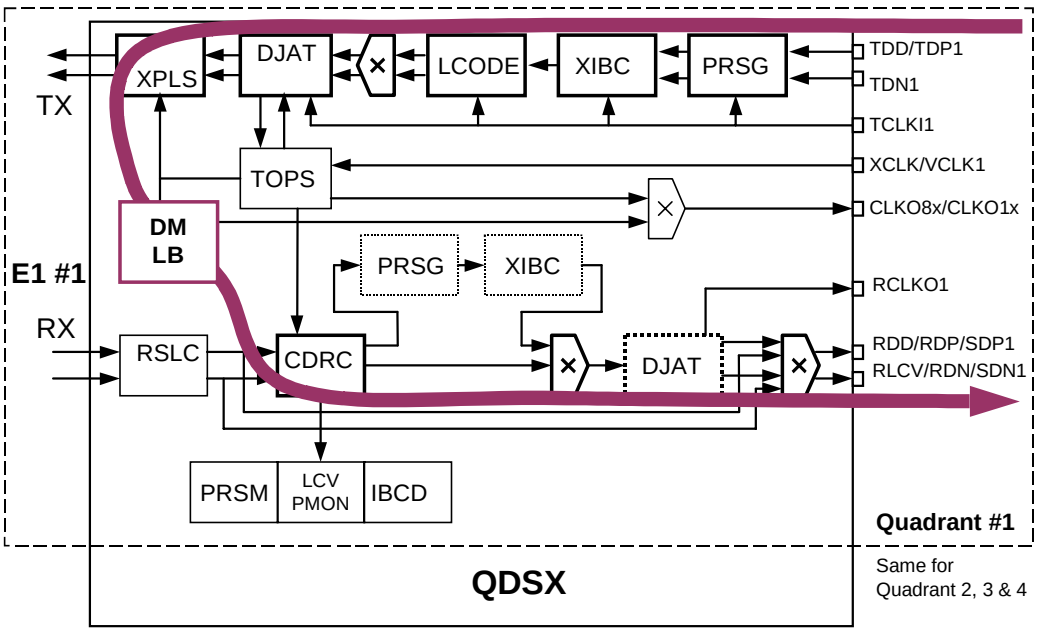
FIGURE 21. QDSX Diagnostic Loopback Mode.



DIALB is a diagnostic digital line loopback used to verify integrity of the data path at the system side of the QDSX device.

FIGURE 22. QDSX Metallic Loopback Mode.



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The DMLB is a diagnostic metalic loopback mode, where the digital RZ version of the TX signals are internally connected to the receive input at CDRC.

3.6 Transmit Jitter Attenuation

The QDSX device provides jitter attenuation in the transmit direction of E1/DS-1 interface using the Digital Jitter Attenuator (DJAT) block (with FIFO). The DJAT input jitter tolerance is 35 Unit Intervals peak-to-peak (UIpp) for an E1 interface with the worst case frequency offset of 308 Hz. The input jitter tolerance is 29 UIpp for a DS-1 interface with the worst case frequency offset of 354 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

The DJAT generates a "jitter-free" 2.048/1.544 MHz clock by adaptively dividing the 24x XCLK input. Adaptation is done according to the phase difference between the generated "jitter-free" clock and the input data clock to DJAT (TCLKI[X] when DJAT is in the default transmit path, or the recovered clock RCLKO[X] if in line loopback mode or when DJAT is configured to be on the receive path). Phase variations in the input clock with a jitter frequency above 8.8 Hz (for the E1 format) or 6.6 Hz (for the T1 formats) are attenuated by 6 dB per octave of jitter frequency. The “jitter-free” clock tracks phase variations below these jitter frequencies.

For further details please refer to the QDSX Data Sheet [1].

3.7 Receiver Jitter Tolerance and Jitter Attenuation

The E1 line receiver provides jitter tolerance that complies with ITU-T Recommendation G.823. Jitter tolerance is determined by performance of the Clock and Data Recovery unit (CDRC). The tolerance is measured with a PRBS20 (with 14 zero restriction) sequence. The QDSX provides two options for the jitter tolerance characteristics. The first option provides better tolerance at low jitter frequencies and the second one provides better jitter tolerance at high jitter frequencies. The DSX-1 interface complies with Bellcore TA-TSY-000170 and AT&T TR62411 specifications.

The jitter attenuation (DJAT) function can optionally be moved to the receive side. The recovered clock and data is passed through the jitter attenuator before being presented at the digital receiver block outputs.

For further details please refer to the QDSX Data Sheet [1].

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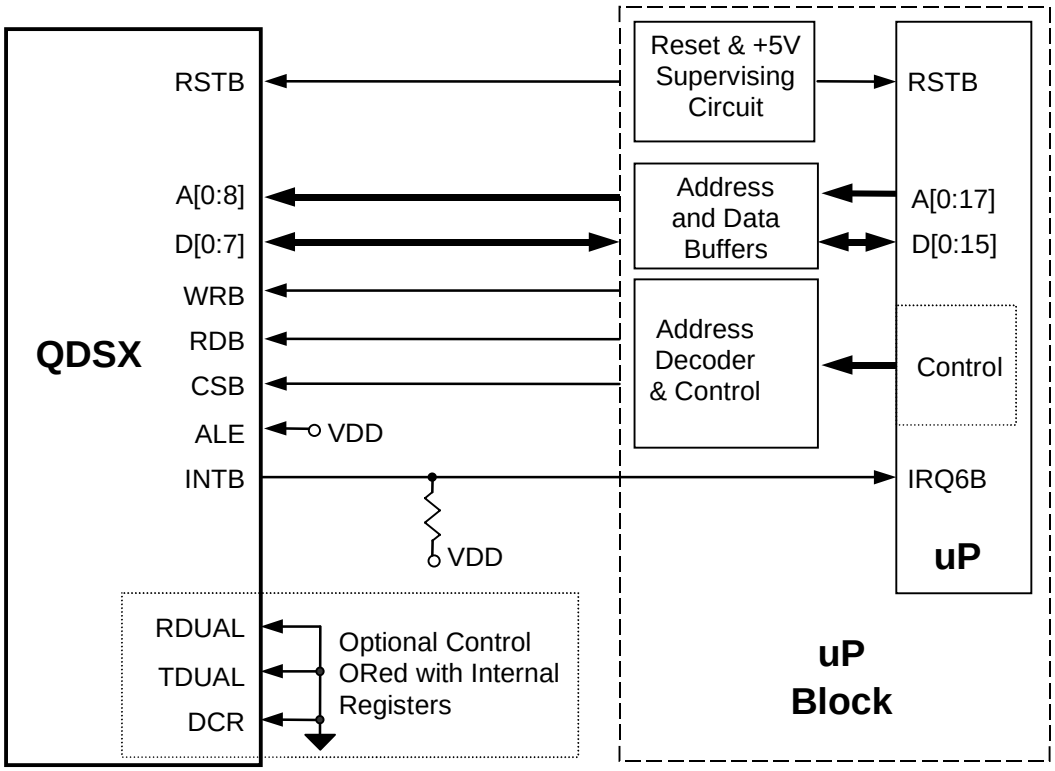
3.8 Microprocessor Interface to QDSX

The QDSX device provides a generic microprocessor interface. This is shown in FIGURE 23.

FIGURE 23. Microprocessor Interface on QDSX



Optional control lines (RDUAL, TDUAL and DCR) are connected to GND and are not used for QDSX control. The same functions are executed via writing to registers through uP port. The interrupt signal INTB is an open-drain output that can be wire ORed with other device. INTB needs a +5V pull-up resistor.

The QDSX device is fully configurable for normal and test modes through the microprocessor interface. The normal mode register access allows the QDSX to be to configured and monitored. The test mode option allows the execution of production test, board test and troubleshooting.

For more on microprocessor interface timing see to references [1], [9] and [11].

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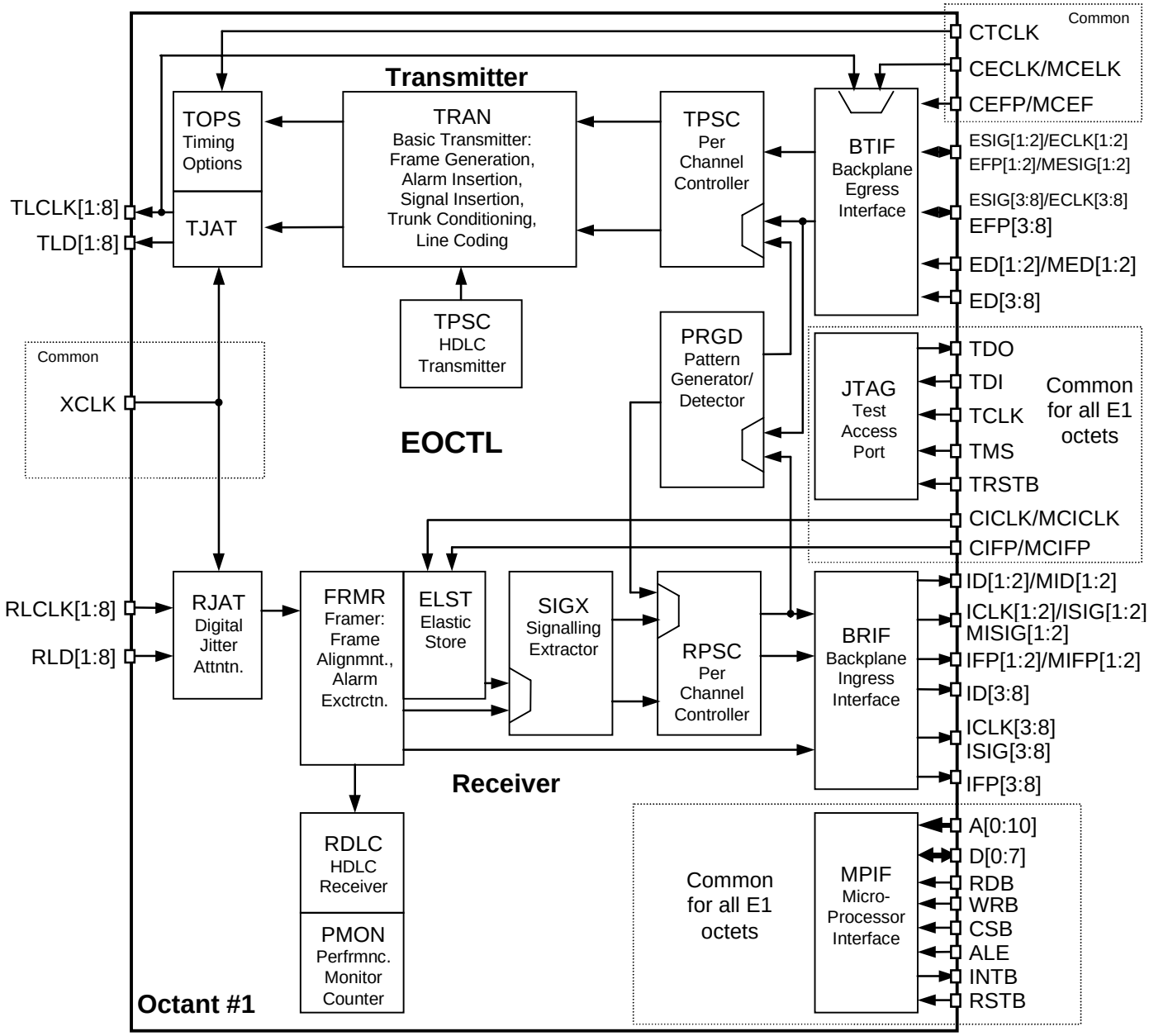
4 EOCTL DEVICE DESCRIPTION

4.1 Block Diagram

FIGURE 24. EOCTL Block Diagram (Octant #1)



NOTE: Octant #1 shown only. Blocks common to all octets are framed with dashed line. Power supply and ground pins not shown.

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The block diagram shows one of the eight octants inside the EOCTL device. All common blocks are framed with dashed line. Other octants are not shown due to complexity of the circuit.

The PM6388 E1 OCTaL Framer (EOCTL) is a feature-rich device for use in systems carrying data (frame relay, Point to Point Protocol, and other protocols) or voice over E1 facilities. Each of the framers and transmitters are independently software configurable, allowing feature selection without changes to external wiring.

On the receive line interface side, each of the eight independent framers can be configured to frame a basic G.704 2048 kbit/s signal as well as finding the signaling multiframe alignment signal and the CRC multiframe alignment. Framing can also be bypassed (unframed mode). The EOCTL detects and indicates the presence of various alarm conditions such as loss of frame-alignment, loss of signaling multiframe alignment, loss of CRC multiframe alignment, reception of remote alarm indication signals, remote multiframe alarm signals, alarm indication signal (AIS) and timeslot 16 alarm indication signal. The EOCTL integrates red and AIS alarms as per industry specifications. Performance monitoring with accumulation of CRC-4 errors, far-end block errors, framing bit errors, and out-of-frame events is also provided.

The EOCTL also detects and terminates HDLC messages on TS16, the Sa National bits, and/or on any arbitrary timeslot. Each HDLC link is terminated in a 128 byte FIFO.

Each of eight independent framers can be configured to frame to either of the common E1 signal formats: CRC-4 MF or to be bypassed (unframed mode). The EOCTL detects and indicates the presence of YELLOW and AIS patterns and also integrates YELLOW, RED, and AIS alarms.

Performance monitoring with accumulation of CRC-4 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided. The HDLC messages are terminated in a 128-byte FIFO. An elastic store that optionally supports slip buffering and adaptation to back plane timing is provided, as is a signaling extractor that supports signaling de-bounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The EOCTL also supports idle code substitution and detection, digital milliwatt code insertion, data extraction, trunk conditioning, data sign and magnitude inversion, and pattern generation or detection on a per-DS0 basis.

On the transmit side, the EOCTL generates framing for CRC-4 MF E1 formats, or framing can be optionally disabled. The EOCTL supports signaling insertion, idle

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code substitution, data insertion, line loopback, data inversion, zero-code suppression, and pattern generation or detection on a per-E0 basis.

The EOCTL can generate a low jitter transmit clock, and also provides jitter attenuation in the receive path.

It should be noted that the EOCTL operates on unipolar data only. The E1 HDB3 and DS-1 B8ZS substitution and line code violation monitoring, if required, must be processed by the E1/DS-1 LIU, in this case the QDSX.

The system side of the EOCTL supports clock, data and framing interfaces. On the Evaluation Card the EOCTL device connects to FREEDM-8. The EOCTL also supports an alternative backplane interface where up to 4 links can be byte-multiplexed onto one of two 8.192Mbps buses.

Further information on the EOCTL can be found in the long form data sheet [2].

4.2 EOCTL Device – Transmit Direction

The “Transmit Direction” is referred to a direction, where gapped data from the system side (egress) is input to the EOCTL, processed by the EOCTL and output on the line interface side (of the EOCTL) as a continuous NRZ data and clock.

4.2.1 BTIF - Backplane Egress Interface

This interface receives payload serial data and clock from the FREEDM device. **NOTE:** This reference design has the default power-up state set to: Master Clock, NxTS Mode, Gapped Clock, 2.048mbit/s Receive/Transmit rates modes. Other operation modes are not discussed in this document.

The EOCTL internal system timing clock is fed from an on board crystal oscillator.

Functions and connections of each BITF interface are as follows:

- **Egress Data ED[1:8]** - the egress data streams are input on these pins. ED[x] lines are shown on the Block Diagram in two subsections ED[1:2]/MED[1:2] and ED[3:8]. The MED[1:2] supports multiplexed data, and is not used on this Reference Design. Therefore, only the ED[1:8] inputs are used. The Clock Master *NxTS* mode is active on the Evaluation Card. ED[x] is sampled on the rising edge of ECLK[x].

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- **Egress Clock (ECLK[1:8]) –** clock for the ED[1:8] data. The Gapped Mode is used. The instantaneous clock speed is 2.048MHz. The gap is used by FREEDM-8 to determine the beginning and the end of the data stream as there are no framing pulses available. The gap coincides partially with the framing signal. The gapped clock is fed from EOCTL to FREEDM device.
  On this reference design default is to gap all DS0 timeslots, while time slots DS1 through DS31 are clocked in. The timeslot DS0 is used by EOCTL to insert framing bits. ECLK[x] is a version of a TLCLK[x] clock. The TLCLK[x] is by default derived from the XCLK by divide by 8. ED[x] is sampled on the rising edge of the associated ECLK[x].
- **Common Transmit Clock (CTCLK).** A Slave Clock Mode is not supported on this reference design and therefore CTCLK is terminated to ground. A provision for an external clock is laid out on the PCB. A 1x2 header TP24/TP25 allows an external clock to be fed to the EOCTL/TOCTL device for a test and demonstration purposes only. The CTCLK has to be at 2.048MHz for E1 and 1.544MHz for DS-1.
- **Common Egress Clock (CECLK) / Multiplexed Common Egress Clock (MCECLK).** This reference design does not support this clock interface. A provision for an external clock is laid out on the PCB and is connected in parallel to CTCLK – see above. The CECLK must be 2.048MHz for E1 or 1.544MHz for DS-1. For more on clock options see reference [2].
- **Common Egress Frame Pulse (CEFP) / Multiplexed Common Egress Frame Pulse (MCEFP)** – this framing bit input is not used on this Reference Design and is connected to GND.

The egress interface has two modes of operation: Non-Multiplexed Bus Egress Mode and Multiplexed Bus Egress Mode. The Non-Multiplexed mode is used on this Reference Design.

The Non-Multiplexed Bus Egress Modes. In this mode the egress Interface allows egress data to be inserted into the transmit line using one of four possible modes. These modes are selected by the ECLKSLV and ESIG_EN bits in the Transmit Backplane Configuration and Egress Interface Options Registers.

For more on bus modes see reference [2].

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4.2.2 TPSC – Per-Channel Controller

The Transmit Per-DS0 Serial Controller allows data and signaling trunk conditioning or idle code to be applied on the transmit E1 stream on a per-channel basis. It also allows per-channel control of zero code suppression, data inversion, per-channel loopback (from the ingress stream), channel insertion, and the detection or generation of pseudo-random or repetitive patterns.

The TPSC interfaces directly to the TRAN block and provides serial streams for signaling control, idle code data, digital milliwatt insertion, and egress data control.

4.2.3 TRAN – Basic E1 Transmitter

The E1 Transmitter (TRAN) generates a 2048 kbit/s data stream according to ITU-T recommendations, providing individual enables for frame generation, CRC-4 Multi-frame generation, and channel associated signaling (CAS) multi-frame generation.

In concert with Transmit Per-Channel Serial Controller (TPSC), the TRAN block provides per-timeslot control of idle code substitution, data inversion, digital milliwatt substitution, selection of the signaling source and CAS data. All timeslots can be forced into a trunk conditioning state (idle code substitution and signaling substitution) by use of the master trunk conditioning bit in the Configuration Register.

Common Channel Signaling (CCS) is supported in timeslot 16 through the internal HDLC Transmitter (TDPR). Support is provided for the transmission of AIS and TS16 AIS, and the transmission of remote alarm (RAI) and remote multiframe alarm signals.

The E1-TRAN supports insertion of 4-bit code words into the National Bits Sa4 to Sa8 as specified in ETS 300-233. Alternatively, the National bits may individually carry data links derived from the internal HDLC controllers, or may be passed transparently from the ED[x] input.

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4.2.4 TJAT – Digital Jitter Attenuation

The TJAT block provides the Digital Jitter Attenuation function in the transmit data path. This block is positioned between the egress interface and the transmit line data. TJAT block receives jittered data and stores the stream in a FIFO timed to the associated clock (CECLK). The jitter-attenuated data emerges from the FIFO timed to the jitter-attenuated clock. In the TJAT, the jitter-attenuated clock TLCLK[x] may be referenced to either CTCLK, CECLK, or RLCLK[1:8].

Jitter attenuator generates its output clock (TLCLK[1:8] by adaptively dividing the 49.152 MHz XCLK signal according to the phase difference between the jitter attenuated clock and the reference clock. Jitter fluctuations in the phase of the reference clock are attenuated by the phase-locked loop within TJAT so that the frequency of the jitter-attenuated clock is equal to the average frequency of the reference. Phase fluctuations with a jitter frequency above 8.8 Hz are attenuated by 6 dB per octave of jitter frequency. The jitter-attenuated clock tracks wandering phase fluctuations with frequencies below 8.8 Hz. The jitter attenuated clock (ICLK[x] for the RJAT and TLCLK[x] for the TJAT) is used to read data out of the FIFO.

If the FIFO read pointer comes within one bit of the write pointer, the TJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics. The TJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 35 UIpp of input jitter at jitter frequencies above 9 Hz. For jitter frequencies below 9 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications the TJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The TJAT blocks meet the low frequency jitter tolerance requirements ITU-T Recommendation G.823.

TJAT exhibits negligible jitter gain for jitter frequencies below 8.8 Hz, and attenuates jitter at frequencies above 8.8 Hz by 20 dB per decade. In most applications the TJAT Blocks will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through TJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is

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directly related to the use of 24X (49.152 MHz) digital phase locked loop for transmit clock generation. TJAT meets the jitter transfer requirements of ITU-T Recommendations G.737, G.738, G.739, and G.742.

Jitter Tolerance. Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For TJAT, the input jitter tolerance is 35 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 308 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

4.2.5 PRGD – Pattern Generator

The Pattern Generator/Detector (PRGD) block is a software programmable test pattern generator, receiver, and analyzer. Patterns may be generated in either transmit or receive directions, and detected in the opposite direction. Two types of ITU-T O.151 compliant test patterns are provided: pseudo-random and repetitive.

The PRGD can be programmed to generate any pseudo-random pattern with length up to 2^{32}-1 bits or any user programmable bit pattern from 1 to 32 bits in length. In addition, the PRGD can insert single bit errors or a bit error rates between 10^{-1} to 10^{-7}.

The PRGD can be programmed to check for the presence of the generated pseudo-random pattern.

The PRGD may also be programmed to check for repetitive sequences. When configured to detect a pattern of length N bits, the PRGD will load N bits from the detected stream, and determine whether the received pattern repeats itself every N subsequent bits. All the features (error counting, auto-synchronization, etc.) available for pseudo-random sequences are also available for repetitive sequences.

4.3 EOCTL Device – Receive Direction

The Receiver section of the EOCTL device in general receives an E1 data stream from a line interface device and outputs at the ingress interface into a backplane type of destination. On this reference design the data is input on the RLD[1:8] pin(s) from the QDSX device, processed by the EOCTL and then fed into the FREEDM device by the BRIF output ID[1:8].

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4.3.1 RJAT – Digital Jitter Attenuation

The very first block in receiver path is the Receive Digital Jitter Attenuator (RJAT). The function of this block is very similar to TJAT described in section *4.2.4* above. For more on RJAT refer to that section and to document [2].

4.3.2 FRMR - E1 Framer

De-jittered data from RJAT is fed to the E1 Framer (FRMR), which searches for frame alignment, CRC multiframe alignment, and Channel Associated Signaling (CAS) multiframe alignment in the incoming recovered PCM stream.

An elastic store ELST (part of the E1 Framer) synchronizes the ingress frames to the common ingress clock and frame pulse (CICLK and CIFP or MCICLK and MCIFP) in the Clock Slave ingress modes. The frame data is buffered in a two-frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

The elastic store can optionally be bypassed to eliminate the two-frame delay. In this configuration (the Clock Master ingress modes), the elastic store is used to synchronize the ingress frames to the transmit line clock (TLCLK[x]) so that per-channel loopbacks may be enabled. Per-channel loopbacks are only available when the elastic store is bypassed, or when CECLK and CICLK clocks and CEFP and CIFP frame pulses are tied together, and the CICLKRISE and CECLKFALL register bits are either both logic 1 or both logic 0. CICLKRISE and CECLKFALL are found in registers 3 and 4 of each octant, respectively. The elastic store cannot be bypassed if the Multiplexed bus is enabled.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The subsequent ingress frame is deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The previous ingress frame is repeated.

A slip operation is always performed on a frame boundary.

For payload conditioning, the ELST can be configured to insert a programmable idle code into all channels when the FRMR is out of frame alignment.

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4.3.3 SIGX – Signal Extractor

The Signaling Extraction (SIGX) block provides signaling bit extraction from timeslot 16 of the ingress. When the external signaling interface is enabled, the SIGX serializes the bits into a serial stream (ISIG[x] or MISIG[x]) aligned to the synchronized outgoing data stream (ID[x] or MID[x]).
The SIGX also provides user control over signaling freezing and provides control over signaling bit fixing and signaling debounce on a per-channel basis. The block contains three multiframes worth of signal buffering to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition. With signaling debounce enabled, the per-channel signaling state must be in the same state for 2 multiframes before appearing on the serial output stream. The SIGX indicates the occurrence of a change of signaling state for each channel via an interrupt and by a change of signaling state bit for each channel.

4.3.4 RPSC – Per-Channel Controller

The RPSC allows data and signaling trunk conditioning to be applied to the receive E1 stream on a per-channel basis. It also allows per-channel control of data inversion, the extraction of clock and data on ICLK[x] and ID[x] (when the Clock Master: NxTS mode is active), and the detection or generation of pseudo-random or repetitive patterns. The RPSC operates on the data after its passage through ELST, so that data and signaling conditioning may overwrite the ELST trouble code.

4.3.5 BRIF – Backplane Ingress Interface

In general terms this interface transmits serial data, signal data, frame pulses and clock(s) to a system (a backplane) destination. The Reference Design uses only data and clock signals that are fed to the FREEDM-8 device. Output data is in E1 format with a gap at the DS0 time slot.

Functions and connections of each BRIF interface pins are as follows:

- **Ingress Data ID[1:8]** - presented to the system HDLC (packet) data. Default settings on the reference design sets the data gap at the DS0 time slot. Time slots DS1 through DS31 are clocked out. Each ID[x] signal contains the recovered payload data stream. ID[x] is aligned to the receive line timing and is updated on the active edge of the associated ICLK[x].

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- **Ingress Clock (ICLK[1:8])** - clock output for the ID[1:8] data. The Ingress Clocks are active when the external signaling interface is disabled. Each ingress clock is a smoothed (jitter attenuated) version of the associated receive line clock (RLCLK[x]). The Clock Master: NxTS mode is active on this reference design. Default on the Evaluation Card sets clock gap at the DS0 time slot. ICLK[x] is a gapped version of the smoothed RLCLK[x]. ID[x] is updated on the active edge of ICLK[x].
- **Common Ingress Clock (CICLK) / Multiplexed Common Ingress Clock (MCICLK) –** this output is not used on this reference design. For more on clock modes refer to [2].
- **Common Ingress Frame Pulse (CIFP) / Multiplexed Common Ingress Frame Pulse (MCIFP)** – this output is not used on this reference design.
- **Ingress Frame Pulse (IFP[1:8])** – this output is not this reference design.

The ingress interface has two modes of operation: Non-Multiplexed Bus Ingress Mode and Multiplexed Bus Ingress Mode. The Non-Multiplexed mode is used on this Reference Design.

The Non-Multiplexed Bus Ingress Modes. In this mode the Ingress Interface allows ingress data to be presented to a system using one of four possible modes as selected by the ICLKSLV and ISIG_EN bits in the Receive Backplane and Ingress Interface Options Registers.

For more on Ingress Bus modes refer to EOCTL Data Sheet [2].

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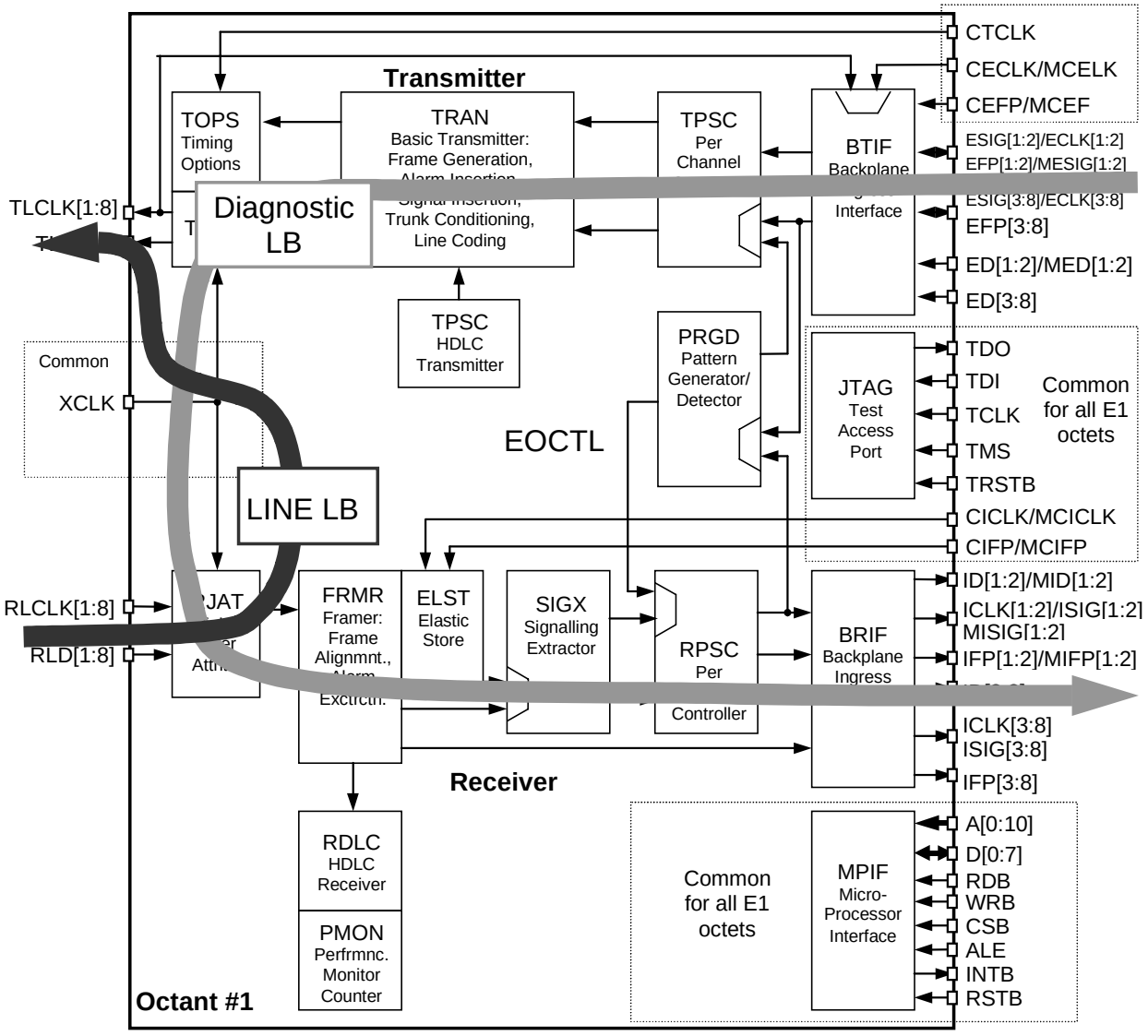
4.4 Loopbacks

FIGURE 25. EOCTL Loopbacks (Octant #1)



The figure above shows the Diagnostic Loopback, which includes most of the EOCTL/TOCTL circuitry. Loopback is executed at the line interface side including TJAT and RJAT.

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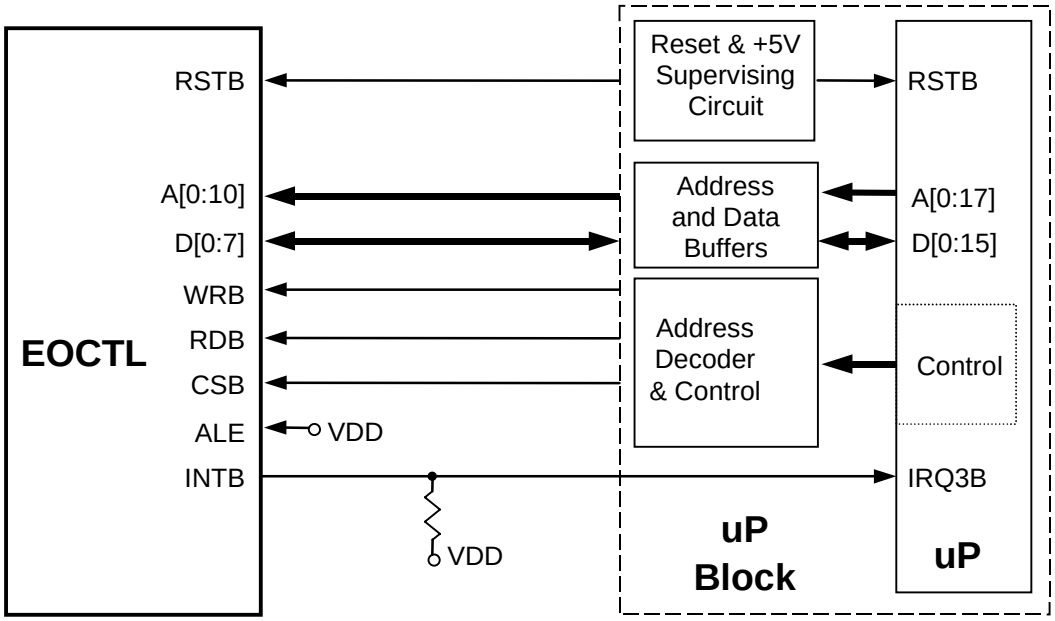
4.5 Microprocessor Interface on EOCTL

The EOCTL device provides a generic microprocessor interface. This is shown in FIGURE 26.

FIGURE 26. Microprocessor Interface on EOCTL



The Motorola 68340 microprocessor is used to monitor and control the EOCTL device. Address decoder and control lines are generated with PAL devices.

The interrupt signal INTB is an open-drain output that can be wire ORed with other devices. INTB needs a +5V pull-up resistor.

For more on microprocessor interface timing refer to EOCTL Data Sheet [2] and MC68340 Software [9].

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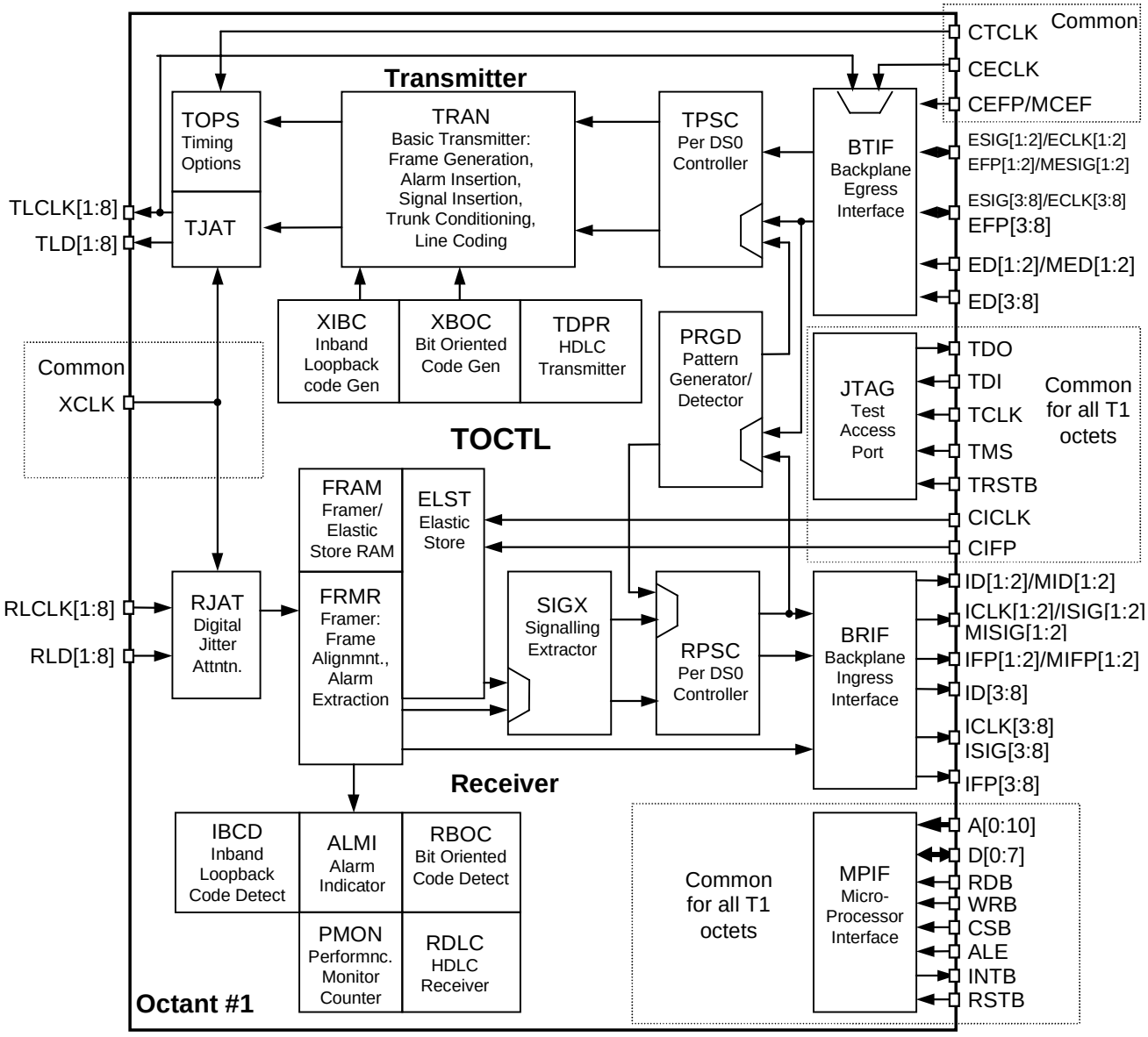
5 TOCTL DEVICE DESCRIPTION

FIGURE 27. TOCTL Block Diagram (Octant #1)



NOTE: Octant #1 shown only. Blocks common to all octets are framed with dashed line. Power supply and ground pins not shown.

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The noticeable differences between EOCTL and TOCTL devices (on the TOCTL block diagram above and EOCTL on FIGURE 24) are related mostly to framing procedures, which are different for each data interface. The external interface ports (pins) are exactly the same as for EOCTL and are not elaborated in this chapter.

The PM4388 Octal T1 Framer (TOCTL) is a feature-rich device for use primarily in systems carrying data (frame relay, Point to Point Protocol, or other protocols) over DS-1 facilities. Each of the framers and transmitters is independently software configurable, allowing feature selection without changes to external wiring.

On the receive side, each of eight independent framers can be configured to frame to either of the common DS-1 signal formats: (SF, ESF) or to be bypassed (unframed mode). The TOCTL detects and indicates the presence of Yellow and AIS patterns and also integrates Yellow, Red, and AIS alarms.

Performance monitoring with accumulation of CRC-6 errors, framing bit errors, out-of-frame events, and changes of frame alignment is provided. The TOCTL also detects the presence of in-band loopback codes, ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. The HDLC messages are terminated in a 128 byte FIFO. An elastic store that optionally supports slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing and interrupt on signaling state change on a per-DS0 basis. The TOCTL also supports idle code substitution and detection, digital milliwatt code insertion, data extraction, trunk conditioning, data inversion, and pattern generation or detection on a per-DS0 basis.

On the transmit side, the TOCTL generates framing for SF or ESF DS-1 formats, or framing can be optionally disabled. The TOCTL supports signaling insertion, idle code substitution, data insertion, line loopback, data inversion, zero-code suppression, and pattern generation or detection on a per-DS0 basis.

The TOCTL can generate a low jitter transmit clock from a variety of clock references, and also provides jitter attenuation in the receive path.

The TOCTL provides a parallel microprocessor interface for controlling the operation of the TOCTL device. Serial PCM interfaces allow 1.544 Mbit/s ingress/egress system interfaces to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic.

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It should be noted that the TOCTL device operates on unipolar data only: B8ZS substitution and line code violation monitoring, if required, must be processed by the T1 LIU.

The operations of the TOCTL device is similar to the EOCTL and is not elaborated further in this reference resign document.

Refer to the TOCTL Data Sheet [3] for more information.

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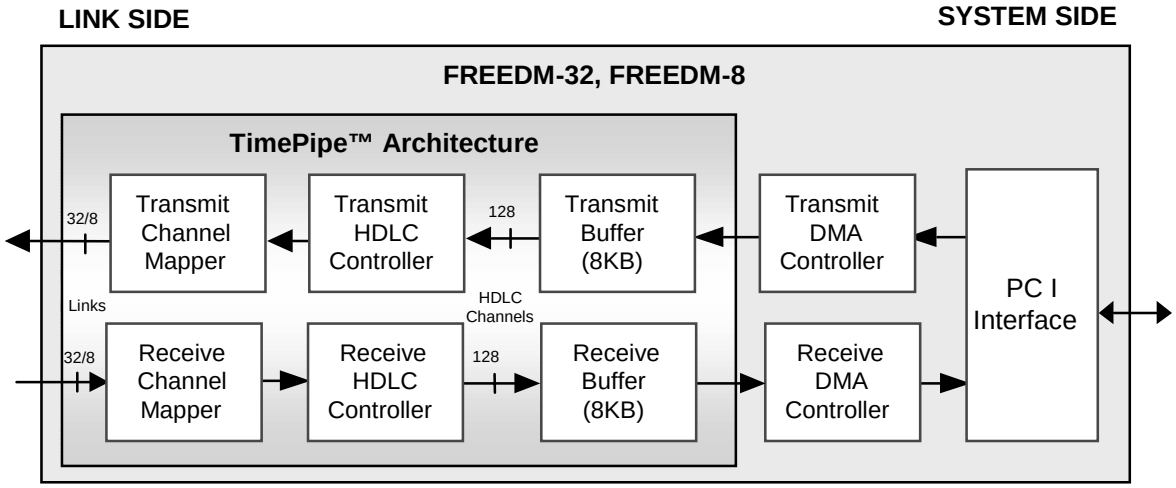
6 FREEDM-8 DEVICE DESCRIPTION

6.1 Block Diagram

The FRame EnginE and Data Link Manager (FREEDM) is a family of advanced data link layer processors that is ideal for applications such as Internet access equipment, frame relay switches, ATM switches, packet-based CDMA base station controllers and Digital Subscriber Loop Access multiplexers (DSLAM).

FIGURE 28. FREEDM Block Diagram and the TimePipe Architecture



The cornerstone of the FREEDM product family is the revolutionary TimePipe™ architecture (as shown in FIGURE 28). The TimePipe architecture enables a single FREEDM-8 device to support up to 8 physical links, 128 HDLC channels and 8 KB of integral packet buffer in each of the transmit and receive direction. Each one of the 8 physical links can be independently timed from 56 kbit/s to 52 Mbit/s. This unparalleled level of integration not only simplifies networking equipment designs, but also enables a new generation of line card designs that can use a common data link layer processor for a wide variety of line rates ranging from T1, E1, E3, T3 to HSSI.

Power is useful only if it can be directed to perform the intended work. The TimePipe architecture is not only powerful but also highly configurable as well. A flexible channel mapper mechanism is provided such that any link can be assigned to any HDLC channel in software. In the case of a channelized application, data carried on one or more time-slots within the same link can be grouped and assigned to a single HDLC channel.

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The 8kB packet buffer can be flexibly allocated to active HDLC channels. The 8kB buffer is organized as 512 blocks of 16 byte FIFOs. The number of blocks assigned to any HDLC channel is configurable in software.

In the receive direction, the Receive HDLC Controller performs flag delineation, bit destuffing, CRC verification using CRC-32 or CRC-CCITT algorithm and length checking. In the transmit direction, the Transmit HDLC Controller performs flag insertion, bit stuffing and CRC calculation using either CRC-32 or CRC-CCITT algorithm.

On the system side, FREEDM provides a 33 MHz, 32 bit PCI 2.1 compliant bus interface. Two efficient transmit and receive DMA controllers are provided to support burst data transfers across the PCI bus.

The following documents should be consulted for further information on the operation and interfaces of the FREEDM-8:

- FREEDM-8 Datasheet [4]
- FREEDM-8 PCI Bus Utilization and Latency Test [5]
- FREEDM-32 Programmer's Guide [6]

6.2 PCI Bus Interface to the Host Processor and Packet Memory

The FREEDM-8 is configured, controlled and monitored across the PCI bus interface by a host processor and packet memory (RAM). In some configurations multiple reference design cards may be present on the PCI bus. During a bus transaction one of the FREEDM-8 devices may act as the bus master in accessing the packet memory, or the host processor may act as the bus master in accessing one of the FREEDM-8 registers on this reference design.

FIGURE 29 below shows an address map for a PCI bus with one FREEDM-8 device. The data structures shown are required to interface one FREEDM-8 to the PCI bus. In this figure, PCI addresses are 32-bit physical addresses, which can be observed at the address pins of the PCI bus interface.

When multiple FREEDM-8's are attached to the bus, each FREEDM-8 must have a unique set of the following data structures.

- Transmit Descriptor Table
- Receive Descriptor Table
- Transmit Queue Space
- Receive Queue Space

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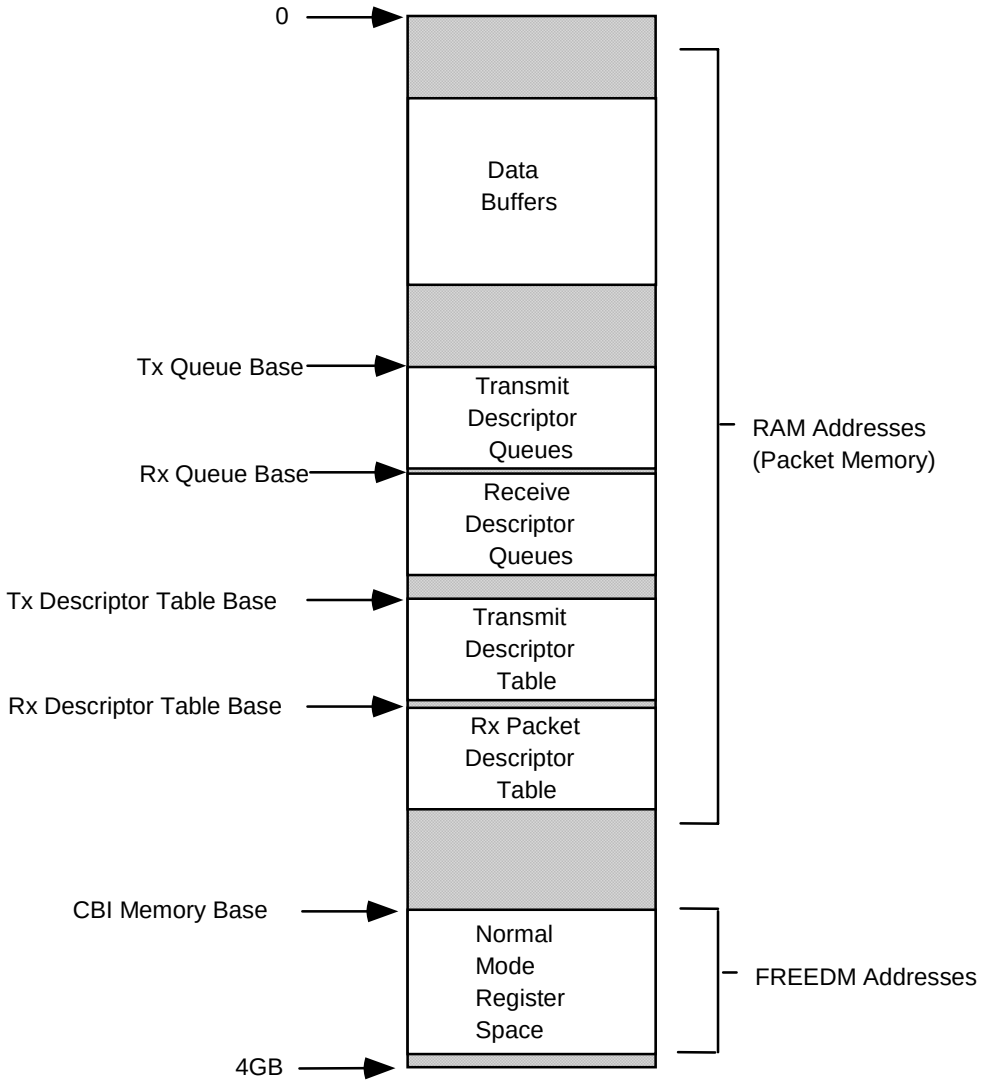
- Normal Mode Register Space

The data structures within packet memory are accessed by software running on the host processor, or by the FREEDM-8. The software specifies the location of these data structures by writing base addresses into the appropriate FREEDM-8 registers, before activating the FREEDM-8.

FIGURE 29. PCI Address Map



The data Buffers are filled with the data received by the FREEDM-8, or contain transmit data, which is read by the FREEDM-8. The descriptor tables and the queues are required to manage these buffers.

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The software running on the host processor to manage and control operation of the FREEDM-8 device accesses the Normal Mode Register space. This register space is located in the FREEDM-8 and is mapped into the PCI address space by the software running on the host processor during the boot-up sequence.

The PCI Configuration Space does not reside in the PCI address map, but it is a requirement for all PCI devices. The Configuration Space is a block of 256 contiguous bytes that reside in the PCI device (the FREEDM-8 in this case), and is accessed by the host processor in a PCI bus Configuration Read (or Write) transaction, rather than a Memory Read (or Write) transaction. Access to this configuration space is system specific and a thorough discussion of it can be found in the PCI specification [10].

A description of the software running on the host processor can be found in the document PMC-970280, "FREEDM-32 Software Reference Design".

6.3 Line Loopback

The FREEDM-8 (and FREEDM-32) device are equipped with line loopback capability. However, it may not work properly if EOCTL/TOCTL device is in Master Clock Mode. Therefore, the line loopback on the FREEDM-8 device is not exercised on this reference design.

6.4 Software Driver

This reference design provides PMC-Sierra's proprietary software driver suitable for test and demonstration purposes only. The driver resides on the Host PC and interfaces with the FREEDM-8 via the PCI Bus.

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7 ON-BOARD MICROPROCESSOR

The FREEDM-8 device has no microprocessor port build-in and therefore an on-board processor is needed. The Motorola 68340 processor monitors and controls the EOCTL and QDSX devices. It provides the following features:

- 16-bit data bus
- Interrupt controller
- Address decoder
- Timer
- Serial interface

The 68340, is commonly used in many host applications, and its main advantage is that it requires a very small number of external components to be operational. The components include clock circuitry, RAM, ROM, and a serial interface (RS232). It also has an abundance of third-party software support, such as real-time operating systems and C-compilers. In addition, the 68340, has a built-in background debug function, which greatly simplifies the code debugging operation.

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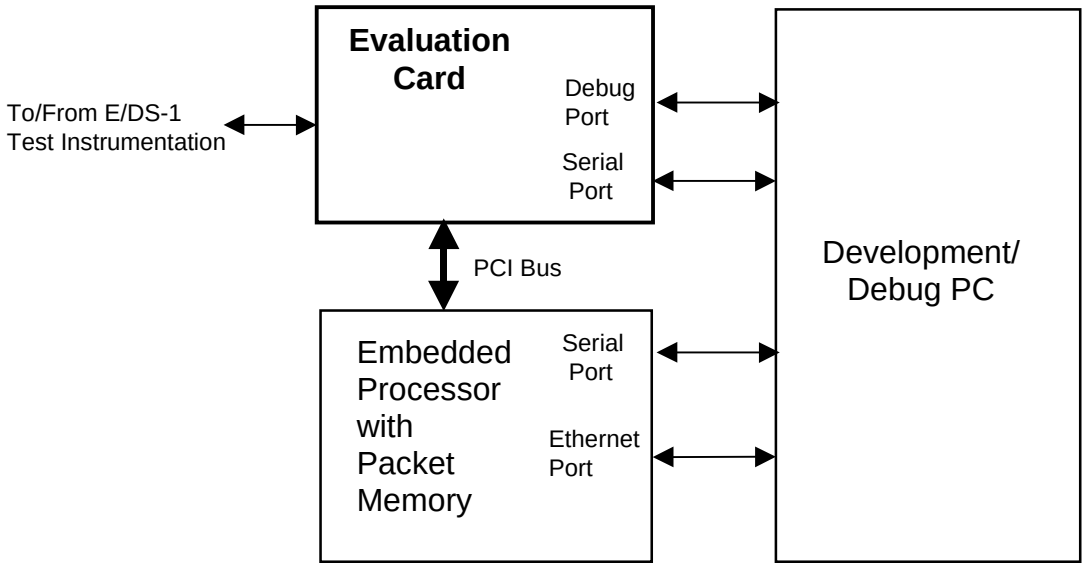
8 SOFTWARE AND FIRMWARE

8.1 System Testbed Description

The EOCTL/TOCTL (FREEDM-8) reference design card is connected to the test system as shown in figure below. The E1/DS-1 interfaces are attached to external instrumentation. The instrumentation can source data into the receive link of the Evaluation Card. The data is returned on the transmit link after loopback through the packet memory, or loopback at a line interface.

FIGURE 30. System Testbed Block Diagram



Alternatively, the host processor and packet memory can source the transmit data. The diagnostic loopback mode of the devices can be used to loopback the transmit data to the receive path.

The serial port of the Evaluation Card allows the development/debug PC to monitor the status of the EOCTL/TOCTL and QDSX's chips. This port is also used to program registers for initialization, software reset and diagnostics.

The debug ports of the reference design card allows the development/debug PC to load software and monitor the status of the software running on the on-board microprocessor. Software can be downloaded through the debug port or provided via the ROM. This port is required during the software development cycle, and is not required for normal operation of the Evaluation Card.

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The serial port of the host processor is used to monitor and control the operation of the FREEDM-8 and the host processor via the development/debug PC.

The processor's Ethernet port is provided to download software into the host processor more quickly than can be achieved via the serial port.

8.2 Firmware Description

The firmware stored in the ROM enables the reading and writing to registers. This enables the EOCTL/TOCTL and QDSX devices to be reset, initialized and monitored for errors etc.

During code development process it's possible to remove ROM from a socket and to download software to the RAM (microprocessor). That procedure speeds up the code troubleshooting process.

8.3 Boot Sequence

8.3.1 EOCTL/TOCTL Detection

The firmware residing in ROM (or downloaded through the BDM port) on power-up prompts processor to search for device type mounted on to U3 spot. EOCTL Chip ID is available in register 009H. The TOCTL Chip ID Program is available in 00CH.

Program overwrites default states of registers in both QDSX and EOCTL or TOCTL devices as required per E1 or DS1 application.

8.3.2 FREEDM-8 Power-up

The FREEDM-8 device has to be initialized via the PCI Bus interface. On-board microprocessor has no access to the FREEDM IC. Software driver is not available at the present time.
NOTE: while programming, make sure FREEDM is set for E1 or T1 data format as required.

8.3.3 EOCTL Boot

If EOCTL is detected, program writes to registers as shown in TABLE 6 below. EOCTL is set to Clock Master mode, Channelized E1, with a clock gap extended across all time-slots 0 (TS0).

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TABLE 6. Power-up Register Initialization with EOCTL

Item	EOCTL Register	Hex Value	Description
1	Receive Line Options 000H, 080H, 100H, 180H, 200H, 280H, 300H, 380H	08H	Bit3 = 1; AUTOYELLOW enabled. This sets auto insertion of RAI (remote alarm indication, yellow alarm) if loss of frame, loss of CRC multiframe and/or AIS (alarm indication). Bit 0 in register 00EH (all octants), has to be set to 0.
2	Transmit Timing Options 004H, 084H, 104H, 184H, 204H, 284H, 304H, 384H	0BH	Bit3=1; changed to set TJAT PLL clock. Bit1=1; changed to select TLCLK as XCLK divided by 24. Bit0=1; changed to select TLCLK as XCLK divided by 24.
3	Receive Backplane Configuration 010H, 090H, 110H, 190H, 210H, 290H, 310H, 390H	89H	Bit7=1; changed to set per-timeslots mode. Bit5=0; changed to select Clock Master. Bit0=1; changed to set backplane speed at 2.048 MHz.
4	Receive Backplane Frame Pulse Configuration 011H, 091H, 111H, 191H, 211H, 291H, 311H, 391H	00H	Bit5=0; changed as required (ICLKSLV=0)
5	Receive Backplane Parity/F-Bit Configuration 012H, 092H, 112H, 192H, 212H, 292H, 312H, 392H	01H	Bit0=1; changed to set totem-pole outputs
6	Transmit Backplane Configuration 018H, 098H, 118H, 198H, 218H, 298H, 318H, 398H	99H	Bit7=1; changed to set per-timeslot mode Bit5=0; changed to set Clock Master Bit0=1; changed to set backplane speed at 2.048 MHz.
7	RJAT Configuration 023H, 0A3H, 123H, 1A3H,	30H	Bit4=1; changed to enable FIFO self-center.

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	223H, 2A3H, 323H, 3A3H		Bit1=0; changed to optimise RJAT PLL Bit0=0; changed to allow RJAT PLL normal operation
8	TJAT Configuration 027H, 0A7H, 127H, 1A7H, 227H, 2A7H, 327H, 3A7H	30H	Bit4=1; changed to enable FIFO self-center. Bit1=0; changed to optimise TJAT PLL Bit0=0; changed to allow TJAT PLL normal operation
9	E1 FRMR Framing Alignment Options 030H, 0B0H, 130H, 1B0H, 230H, 2B0H, 330H, 3B0H	E2H	Bit7=1; changed to enable framing on CRC multiframe. Bit6=1; changed to disable search for signalling frame. Bit5=1; changed to enable for continuous check for CRC multiframe. Bit1=1; changed to enable excessive CRC error to force for re-framing.
10	E1 TRAN Configuration 040H, 0C0H, 140H, 1C0H, 240H, 2C0H, 340H, 3C0H	11H	Bit6=0; changed to disable signalling. Bit5=0; changed to disable signalling. Bit4=1; changed to enable generation of CRC multiframe. Bit0=1; changed to disable signalling data insertion
11	RPSC Configuration 05CH, 0DCH, 15CH, 1DCH, 25CH, 2DCH, 35CH, 3DCH	03H	Bit1=1; changed for indirect access. Bit0=1; changed to enable per-channel functions.
12	RPSC Channel Indirect Data Buffer 05FH, 0DFH, 15FH, 1DFH, 25FH, 2DFH, 35FH, 3DFH 05EH, 0DEH, 15EH, 1DEH, 25EH, 2DEH, 35EH, 3DEH	(data loop sequence) (address loop sequence, with Bit7=0 must)	RPSC Configuration for Channelized E1. A sequence of writing address and data into registers is required to set per-timeslot indirect registers. **For all eight physical links, all timeslots 0 (TS0) must have Bit6=1 in indirect register 20H to generate gap in Clock**

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			Master mode. Write 40H into indirect registers 20H. All other indirect per-timeslot registers (TS1 to TS31) are written with 00H. See data sheet [2] for explanation.
13	TPSC Configuration 060H, 0E0H, 160H, 1E0H, 260H, 2E0H, 360H, 3E0H	03H	Bit1=1; changed for indirect access. Bit0=1; changed to enable per-channel functions.
14	TPSC Channel Indirect Data Buffer 063H, 0E3H, 163H, 1E3H, 263H, 2E3H, 363H, 3E3H 062H, 0E2H, 162H, 1E2H, 262H, 2E2H, 362H, 3E2H	(data loop sequence) (address loop sequence, with Bit7=0 must)	TPSC Configuration for Channelized E1. A sequence of writing address and data into registers is required to set per-timeslot indirect registers. **For all eight physical links, all timeslots 0 (TS0) must have Bit6=1 in indirect register 20H to generate gap in Clock Master mode. Write 40H into indirect registers 20H.** All other indirect per-timeslot registers (TS1 to TS31) are written with 00H. See data sheet [2] for explanation.

	QDSX Register	Hex Value	Description
15	000H, 040H, 080H, 0C0H	01H	Bit0=0; changed for E1 receiver
16	001H, 041H, 081H, 0C1H	01H	Bit0=0; changed for E1 transmitter
17	02CH, 06CH, 0ACH, 0ECH 02EH, 06EH, 0AEH, 0EEH 02FH, 06FH, 0AFH, 0EFH 02CH, 06CH, 0ACH, 0ECH	00H (loop sequence) (loop sequence) 80H	A sequence of writing data into registers is required to shape E1 line waveform as required per ANSI-T1.102. See TABLE 5 on page 22 (in this document) and data sheet [1] for explanation.

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8.3.4 TOCTL Boot

If TOCTL is detected, program writes to registers as shown in TABLE 7 below. TOCTL is set to Clock Master mode, Cahnnelized T1, with a clock gap at bit F.

NOTE: this table was tested with TOCTL Rev E, packaged in PQFP-128.

TABLE 7. Power-up Register Initialization with TOCTL

Item	TOCTL Register	Hex Value	Description
1	Receive Line Options 000H, 080H, 100H, 180H, 200H, 280H, 300H, 380H	08H	Bit 3 = 1; AUTOYELLOW enabled. This enables auto insertion of RAI (remote alarm indication, yellow alarm) if Red Alarm is detected in ingress direction.
2	Ingress Interface Options 001H, 081H, 101H, 181H, 201H, 281H, 301H, 381H	00H	Bit 7=0 and Bit 6=0; changed to select Clock Master and NxDS0 mode.
3	Egress Interface Options 005H, 085H, 105H, 185H, 205H, 285H, 305H, 385H	00H	Bit 7=0 and Bit 6=0; changed to select Clock Master and NxDS0 mode.
4	Transmit Timing Options 007H, 087H, 107H, 187H, 207H, 287H, 307H, 387H	0BH	Bit 3=1 and Bit 2=0; changed to set reference source for TJAT Bit 1=1 and Bit 0=1; changed to generate a jitter free 1.544MHz clock reference from crystal oscillator XCLK/24
5	RJAT Configuration 013H, 093H, 113H, 193H, 213H, 293H, 313H, 393H	21H	Bit 1=0; RJAT PLL control.
6	TJAT Configuration 01BH, 09BH, 11BH, 19BH, 21BH, 29BH, 31BH, 39BH	21H	Bit 1=0; TJAT PLL control.
7	FRMR Configuration 020H, 0A0H, 120H, 1A0H, 220H, 2A0H, 320H, 3A0H	90H	Bit 7=1; changed to set ratio of error to total bits before out of frame (2 of 6). Bit 4=1; changed to set extended super frame format.

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8	ALMI Configuration 02CH, 0ACH, 12CH, 1ACH, 22CH, 2ACH, 32CH, 3ACH	10H	Bit4=1; changed to set extended super frame format.
9	TPSC Configuration 030H, 0B0H, 130H, 1B0H, 230H, 2B0H, 330H, 3B0H	03H	Bit1=1; changed for indirect access. Bit0=1; changed to enable per-channel functions.
10	TPSC Channel Indirect Data Buffer 033H, 0B3H, 133H, 1B3H, 233H, 2B3H, 333H, 3B3H 032H, 0B2H, 132H, 1B2H, 232H, 2B2H, 332H, 3B2H	(data loop sequence) (address loop sequence, with Bit7=0 must)	TPSC Configuration for Channelized T1. A sequence of writing address and data into registers is required to set per-timeslot indirect registers. **For all eight physical links, all timeslots TS1 to TS24 must have all bits set to 0 in Clock Master mode. Write 00H into indirect registers 01H-48H.** See data sheet [3] for explanation.
11	SIGX Configuration 040H, 0C0H, 140H, 1C0H 240H, 2C0H, 340H, 3C0H	04H	Bit2=1; changed to set extended super frame format.
12	XBAS Configuration 044H, 0C4H, 144H, 1C4H, 244H, 2C4H, 344H, 3C4H	10H	Bit4=1; changed to set extended super frame format.
13	RPSC Configuration 050H, 0D0H, 150H, 1D0H, 250H, 2D0H, 350H, 3D0H	03H	Bit1=1; changed for indirect access. Bit0=1; changed to enable per-channel functions.
14	052H, 0D2H, 152H, 1D2H, 252H, 2D2H, 352H, 3D2H 053H, 0D3H, 153H, 1D3H, 253H, 2D3H, 353H, 3D3H	(data loop sequence) (address loop sequence, with Bit7=0 must)	RPSC Configuration for Channelized T1. A sequence of writing address and data into registers is required to set per-timeslot indirect registers. **For all eight physical links, all timeslots TS1 to TS24 must have Bit2=1 in indirect registers 01H**

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			to 18H to generate ICLK in Clock Master mode. Write 04H into indirect registers 01H-18H. All other indirect per-timeslot registers are written with 00H. See data sheet [3] for explanation.
QDSX Registers			
	QDSX Register	**Hex Value**	**Description**
15	02CH, 06CH, 0ACH, 0ECH 02EH, 06EH, 0AEH, 0EEH 02FH, 06FH, 0AFH, 0EFH 02CH, 06CH, 0ACH, 0ECH	00H (loop sequence) (loop sequence) 80H	A sequence of writing data into registers is required to shape DS11 line waveform as required per ANSI-T1.102. Data values depend on cable length chosen. See TABLE 5 above and data sheet [1] for explanation.

8.4 Homologation Software

NOTE: This may be relevant to reference design (evaluation card) sampled to PMC-Sierra's customers. The firmware (software) programmed into the on-board ROM (U13) has homologation related code removed. Interrupts are not enabled.

8.4.1 State Matrix

Software was developed specifically for CTR 4/ETS 300 011 conformance. The software consists of an interrupt service routine to monitor the state of the Evaluation card. The states are defined in ITU I.431 and are summarized below:

- F1: Normal Operation

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- network timing is available
- user receives normal operational frames (NOF) with associated CRC bits
- user transmits NOF with associated CRC bits and CRC error bits (E bits) if a CRC error is detected

- F2: Fault condition 1
  - network timing is available
  - user receives frames with RAI bit set and associated CRC bits
  - user transmits NOF with associated CRC bits and CRC error bits (E bits) if a CRC error is detected
- F3: Fault condition 2
  - network timing is not available
  - user detects loss of signal (which includes loss of frame alignment)
  - user transmits frames with RAI bit set and associated CRC bits
- F4: Fault condition 3
  - network timing is not available
  - user detects AIS
  - user transmits frames with RAI bit set and associated CRC bits
- F5: Fault condition 4
  - network timing is available
  - user receives frames with RAI bit set and associated CRC bits
  - user receives continuous CRC error bits set low denoting error
  - user transmits NOF with associated CRC bits and CRC error bits (E bits) if a CRC error is detected

The EOCTL has several interrupt bits that detect the states defined above. They are the RAI, RED, AIS and RAICCRC for fault conditions 1, 2, 3 and 4 respectively.

To activate the interrupts, the interrupt enable bits must be set. Register 032h FRMR Framing Status Interrupt Enable contains the enables for RAI, RED and AIS. This register is set to the value 0x8C. Register 03Eh FRMR Frame Pulse/Alarm Interrupt Enable contains the enable for RAICCRC. These bits can

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then be monitored, either by interrupt service routines or polling, to update the state.

8.4.2 Basic Frame and CRC MultiFrame

The software also initialized the EOCTL specifically for ETSI standards. ETSI standards test the robustness of the device's ability to frame to the basic frame and CRC multiframe. The framing recommendations are defined in ITU G.706.

The recommendations state that the device must be able to declare loss of frame when:

- Three incorrect frame alignment signals are received.
- Bit 2 of timeslot 0 of NFAS frames is received in error on three consecutive occasions.

The recommendations state that the device must be able to declare loss of multiframe when:

- Two valid CRC multiframe alignment signals cannot be found within 8 ms or four multiframes.

The EOCTL is software configurable and contains registers that can set the criterion above. Register 031H is set to 0xE2. This enables the EOCTL to frame to the CRC multiframe, and reframe based on multiframe errors. Also, Register 032H is set to 0x40. This sets the criterion for basic frame alignment.

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9 IMPLEMENTATION DESCRIPTION

9.1 Printed Circuit Board Layout

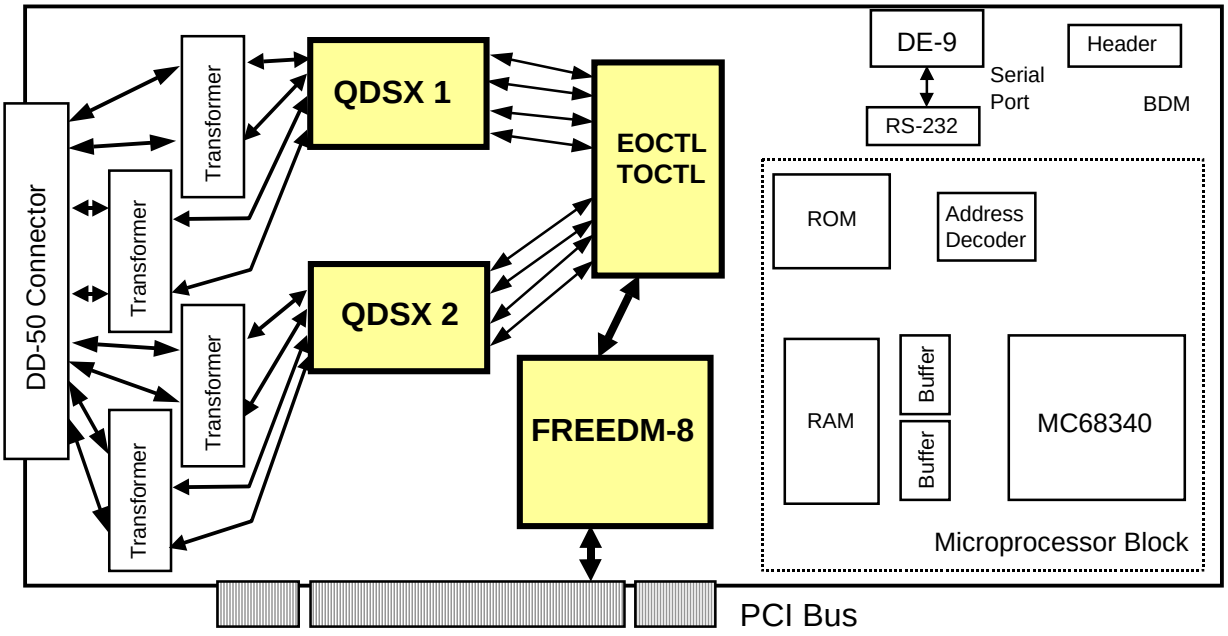
9.1.1 Card Size and Component Placement

The card size conforms to the height and length constraints for a PCI add-in card as specified in the PCI specification. This card must be operable with the computer cover closed and therefore the line interface inputs (E1/T1) must be accessible at the front of the Evaluation Card (back of the PC). The serial port and BDM port are accessible inside the PC with the cover open.

The dimension of the card conforms to the 5V PCI Card, with mounting holes located as per the specification

The card floor plan is shown in figure below.

FIGURE 31. Card Floorplan



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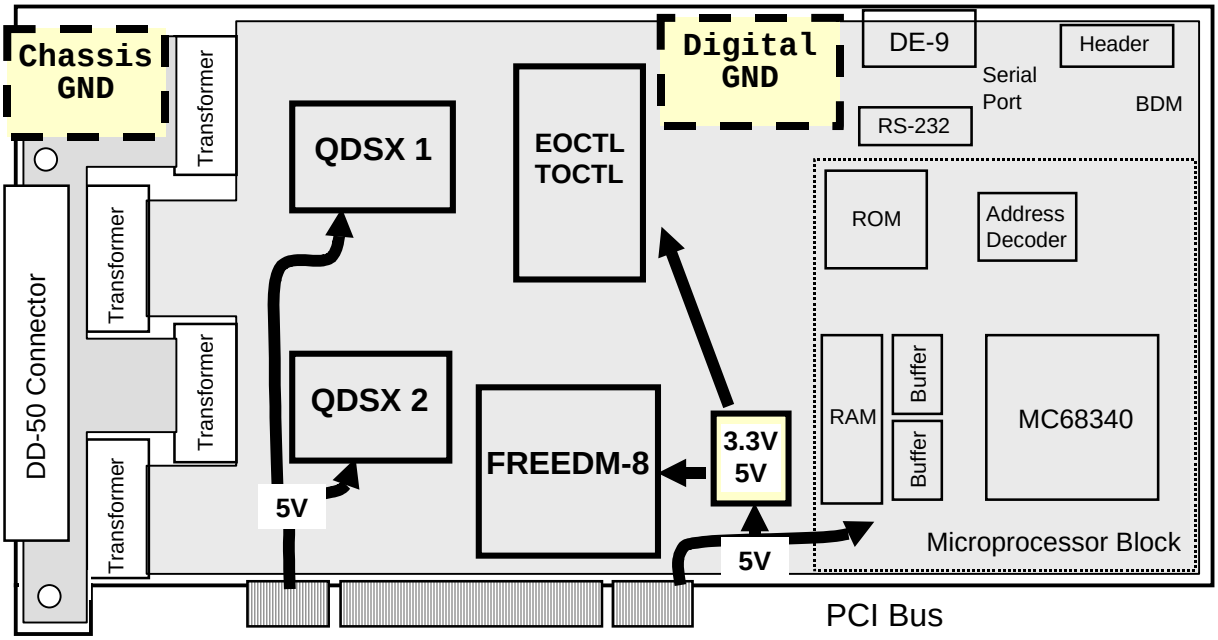
9.1.2 Ground and Power Planes

FIGURE 32. Ground and Power Planes



The ground plane is divided into two islands: the “Chassis GND”, and “Digital GND”.

The “Chassis GND” is connected to a metal bracket holding the card inside the PC. This bracket must have a very good metallic connection to the PC chassis to minimize EMI radiation. The Chassis GND has no connection to any other ground planes. A very distinct clearance between the two planes must be provided underneath the transformers to eliminate common mode coupling from noisy PCI Bus environment into E1/T1 twisted pair lines.

All other components are connected to a single ground plane. The PCB card has two layers of copper dedicated to ground. These ground planes connects to the PCI Bus connector. The +5V connects to associated pins on the same connector. The +5V rail has dedicated filtering elements (ferrite beads, serial resistors and capacitors) associated with power pins on different devices. Example of a filtering entity is shown in FIGURE 11 in previous chapter.

The FREEDM and EOCTL devices need a 3.3V supply, that is derived from an on-board 5/3.3V linear regulator.

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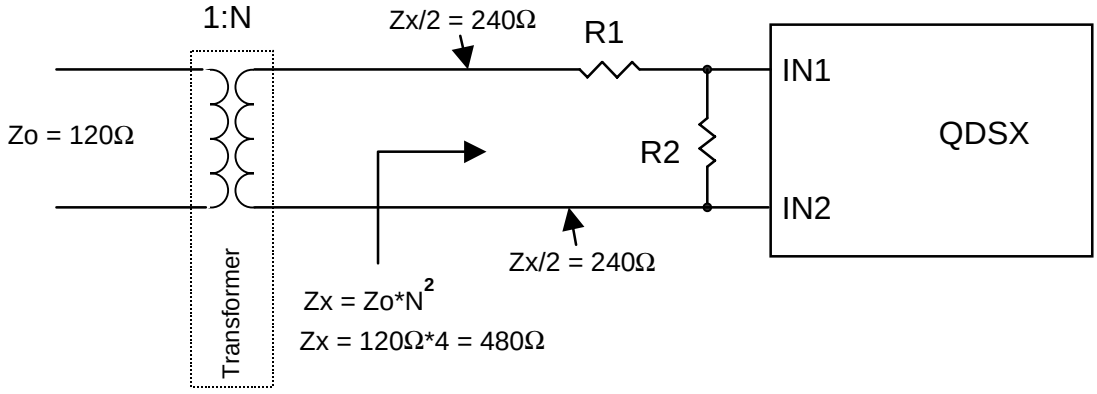
If the EMI is an issue for the particular design, it is recommended to have filtering elements associated with power rail dedicated to each line interface device (QDSX). Filter prevents coupling of a noise on power rails to line receivers and drivers.

9.1.3 Layer Stacking and Transmission Line Impedance Control

The PCB Card has a total of six layers: layers 1, 3 and 6 are for signals, layers 2 and 5 for ground, and layer 4 for power. The dimension of the card conforms to the 5V PCI Raw Card.
Example of layer configuration and characteristic impedance calculation is shown below.

The trace layout on the E1/DS-1 interface side is not critical due to limited frequency spectrum of transmitted and received signals. However, it's good engineering practice to keep transmission lines at appropriate impedance and with minimum crosstalk at line interfaces. The impedance of lines interfacing with QDSX devices is different for receive and transmit sides due to different transformer ratios.

FIGURE 33. Receive Trace Impedance for E1 Interface.



The characteristic impedance on the secondary side of the 2:1 transformer for E1 line interface is calculated as follows (N=2):

$Zx = Zo*N^2 = 120\Omega * 4 =$ **480Ω**
Resistors value have to meet requirement: R1 + R2 = **480Ω**

Each trace connecting the transformer and the QDSX device is ½ the Zx value (Zx=240Ω) . However, circuit has to support DS-1 interface also, where

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characteristic impedance Zo = 100Ω Therefore, the trace impedance can be calculated as an average of both values:

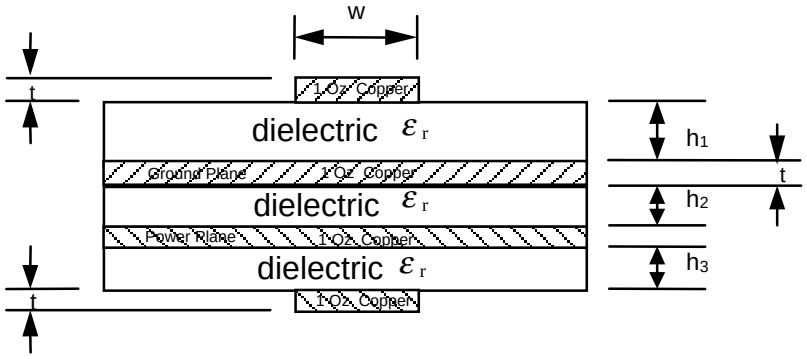
Zx_trace = {((120 + 100)/2)* 4}/2 = 210Ω

The E1 receiver interface has to meet a Return Loss specification shown in ITU-G.703 Section 6.3.3.

The transmit interface Return Loss is not specified in ITU-G.703. Good engineering practice is to keep line impedance close to characteristic impedance also. Transformer ratio is 1.36:1 and that means that Zx must be less than 120Ω Final calculation (average of E1/DS-1) gives the transmitter trace impedance at 30Ω The internal QDSX transmitter impedance is low and is about 2.5Ω

Following is a short introduction to printed circuit design in applications, where a high-speed clock and data lines with edges as fast as a couple of nanoseconds are required. Proper termination on both ends of transmission line is required to avoid edge distortion due to back-reflection. Wrong termination of high-speed lines contributes to overall EMI radiation from the Card and may cause problems if a customer's design is subject to FCC EMI Class A/B testing.

FIGURE 34. PCB Cross Section (Example).



where

ε_r = relative dielectric constant, nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected. For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric.

w = width of copper

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The PCB related parameters are shown in the following table:

TABLE 8. Printed Circuit Board Parameters (Example).

Parameters	Nominal
Board Thickness (mil)	62 (including copper thickness)
dielectric thickness between layers 1 and 2 (mil) (h1)	10
dielectric thickness between layers 2 and 3 (mil) (h2)	33
dielectric thickness between layers 3 and 4 (mil) (h3)	10
Relative dielectric constant	4.2

To reduce signal degradation due to reflection and radiation, the traces that carry high-speed signals should be treated as micro strip transmission lines with controlled impedance and matched resistive termination. The trace impedance is calculated using the formula:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

Parameter	Data
ε_r	4.2
h1 (mil)	10
T (mil) (2 Oz copper)	2.88
Zo (Ohm)	50
W (mil)	16

Given a characteristic impedance Zo, the dielectric thickness h1 is proportional to trace width. A small h1 will result in the traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board for a given trace impedance and adequate trace width should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication.

Using the same h1, thickness of copper, and dielectric constant, a 16 mil traces has a characteristic impedance of approximately 50Ω while an 6 mil trace has a characteristic impedance of 75Ω

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The above calculation shows that with a standard PCB thickness, the trace width and layout may not be able to support trace impedance from 30Ω to 210Ω required by the Evaluation Card. More sophisticated means of trace impedance control may be required, or impedance has to be compromised, to meet requirement of lower cost and simplified PCB layout.

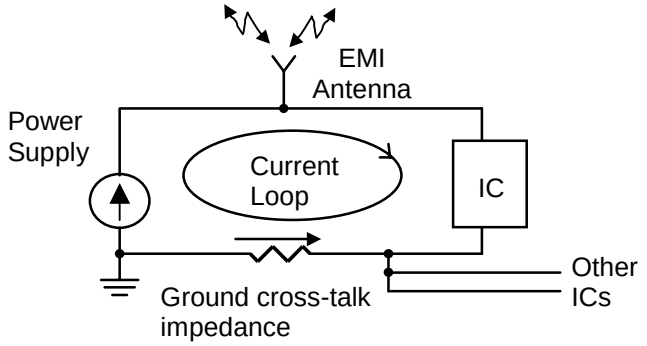
9.1.4 Decoupling, Bypassing and Bulk Capacitors

Decoupling capacitors provide localized switching current required by the power pins they connect to. Bypassing capacitors also remove unwanted power supply noise before it can enter sensitive areas.

Bulk capacitors are used to maintain a constant DC voltage and provide switching currents required by all components.

The power distribution loop of an IC is illustrated below.

FIGURE 35. Current Loop Model Without Decoupling Capacitor.



Without any capacitors in parallel, the IC will attempt to draw a large switching current directly from the power supply, which could be located far away. The inductance on the power and ground plane will limit this instantaneous current drawn. As a result, the voltage at the IC's power pin will drop and the output will ramp up more slowly. EMI radiation may be emitted from the PCB. Furthermore, since EMI is a function of loop area and frequency, the larger the loop area and the higher the frequency, the more significant the EMI. A symbolic antenna shows bi-directional EMI coupling to-from the trace.
A loop current creates ground crosstalk voltage across the ground impedance also.

Adding decoupling capacitors breaks the current loop into several smaller loops as illustrated below:

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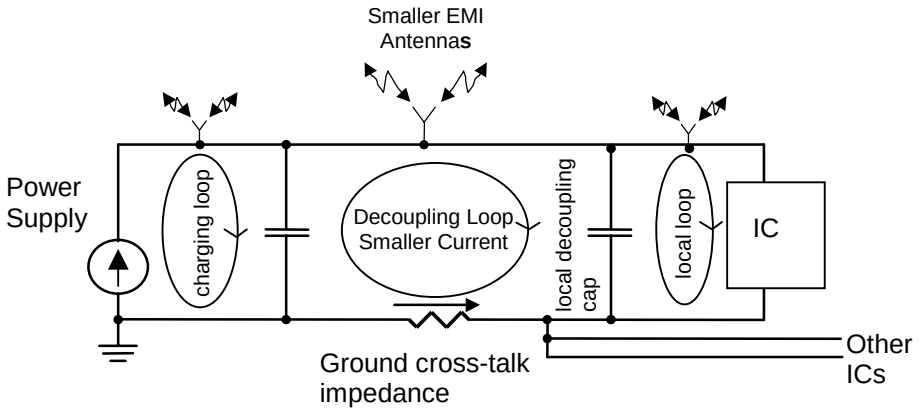
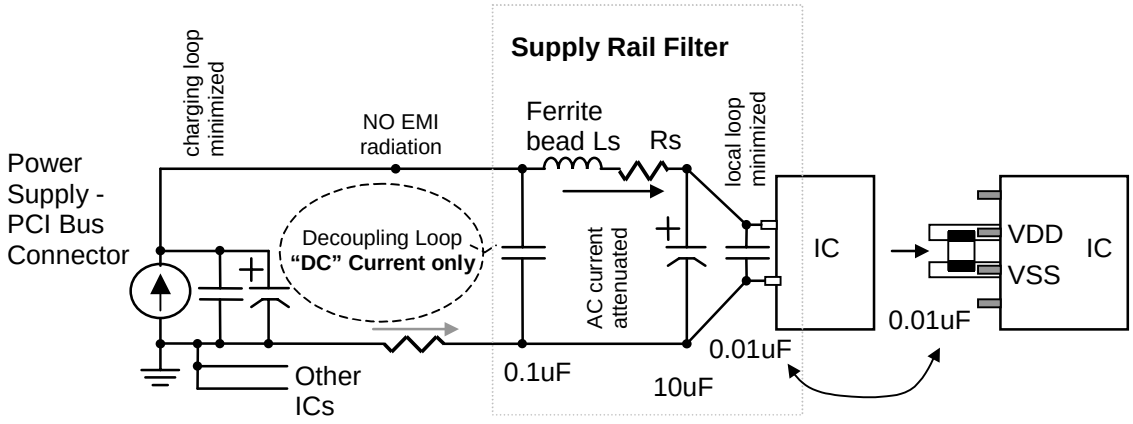
FIGURE 36. Current Loop Model With Decoupling Capacitors.



The local loop is created as a result of a decouple capacitor placed next to the IC's power pin. The bulk power supply decoupling capacitor is charged by a local power supply via the charging loop. Charging the local decoupling capacitors via the bulk decoupling capacitor creates the decoupling loop. However, as it is shown above, smaller EMI radiation (antennas) still exists. The ground AC crosstalk is not gone as well.

EMI sensitive applications have to use more complex solutions. One of them is to employ ferrite beads, serial resistors and capacitors as shown in figure below.

FIGURE 37. Current Loop Model With Power Rail Filter.



The supply rail Π type low pass filter consists of ferrite bead Ls, serial resistor Rs and decoupling capacitors (10uF, 0.1uF and 0.01uF). Present SMD technology allows a small body 0.01uF capacitors to be placed across 0.5mm pitch pinout of the decoupled IC. A tantalum 10uF capacitor helps to reduce lower frequency

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noise, e.g.: switching power supply noise, digital noise. The end effect of the power supply filtering is to provide a “decoupling loop” that supplies a “DC” current with a small residual high frequency AC current. This eliminates EMI and minimizes ground impedance AC crosstalk. In addition proper placing of noisy devices across a ground plane reduces crosstalk also.

Power supply filtering capacitors are placed as close as possible to the PCI Bus connector pins. In order for the power supply decoupling capacitors to maintain a relatively constant DC voltage, it must be able to supply all the charging current demands of the local decoupling capacitors.

9.1.5 Calculation of Decoupling Capacitor Values

In order for local decoupling capacitors to be effective, they must provide the least impedance at the switching frequency of the IC; otherwise, they will not discharge at all because the switching current will come from other lower impedance paths (and possibly larger loops). Therefore, one must choose a decoupling capacitor that has a resonant frequency (where it has the lowest impedance) same as (or close to) the frequency of the switching, and place the decoupling capacitor as close to the power pin as possible to reduce trace inductance. In addition, the local decoupling capacitor must be large enough to provide the instantaneous current with tolerable voltage drop. The decoupling capacitance, required per VDD pin, could be calculated using the following formula:

$$C = I \Delta t / \Delta V$$, where

C = total capacitance in Farads

I = instantaneous switching current in Amps

Δt = the time duration of the switching current

ΔV = maximum allowed voltage drop on VDD supply

Instantaneous current (I) depends on the capacitive load of each output. The duration of the switching current depends on the capacitive load. The digital signals of the evaluation card uses approximately 75 Ohm traces. When an output switches, it sees a 75 Ohm characteristic impedance in series with output resistance. As the load charges up exponentially, the amount of current required decreases until it reaches a steady state. To calculate the largest current demand of an output, one must know its output impedance. However, for CMOS devices, the output impedance changes as the output changes. As an approximation, a QDSX output will require 50 mA of switching current for charging a 50 pF load from 0 to 5 volts in 5ns.

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Using this figure, for a VDD pin supplying 4 outputs, each of which requires 50 mA for 5 ns, and a maximum allowable voltage spike of 100 mV, the capacitance required is: 4 * 50mA * 5ns / 100mV = 0.01 uF.
A 0.01 uF capacitor can be used in this case. That capacitor is placed across VDD and VSS pins.

9.1.6 PCI Interface

The reference design card supports a 32-bit PCI local bus interface. The PCI edge connector is a universal type allowing it to be plugged into a motherboard that supports either the 5V or the 3.3V signaling environments. However, not all computers provide +3.3V and therefore a +5V to +3.3V linear regulator is required.

This reference design does not have “hot insertion” capability and therefore the PC must be powered down before Card is plugged-in or removed from a motherboard.

9.2 Schematic

The following is a description of the key functional components shown in the schematics. The actual schematics are included in Appendix A.

Page 1 of the schematic shows all five main blocks of the Reference Design. However, schematic contains total of nine pages, because the Allegro/Syslab/Concept CAD schematic capture program allows to include multiple schematic pages in a single block. That feature simplifies drawing.

The net node names on each schematic page are shown with \I or without \I suffix. The only exception is the Page 1 – all net nodes are shown without suffix \I on this Page.
The net names, placed on the Page 2 through Page 9, with the \I suffix show connections between the main five blocks. The same nod names (with suffix \I removed) are shown on the Page 1.
The net node names shown on the Page 2 through Page 9 without suffix (\I) may connect any node inside the same block; e.g. net name “ASB on Page 8 and Page 9 inside block “MICRO INTERFACE”.

9.2.1 Page 1: Root Drawing

This page provides a block view of the interface signals between each block. Blocks are drawn in order to show data flow. At the top left corner E1/T1 LINE INTERFACE block terminates external data lines. Data (and clock) flows through

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QDSX, EOCTL/TOCTL and FREEDM-8 blocks. The FREEDM-8 block is the system interface. The MICRO INTERFACE is a supporting block and it is placed at the bottom of the schematic Page 1.

The following notes are provided:

- The reset signal from the microprocessor is routed to each device except the FREEDM-8. The FREEDM-8 is reset via the PCI bus, whenever the system is reset, or whenever the FREEDM-8 is reset under software control.
- An on-board microprocessor block provides an interface to program each of the EOCTL and QDSXs registers. It also provides a separate interrupt line for each of the QDSXs and the EOCTL/TOCTL.
- The FREEDM-8 is programmed via a host processor at the PCI Interface.
- A JTAG chain connects the FREEDM-8, the EOCTL's, the QDSX, and the MC68340.
- The clock timing circuit is included in the EOCTL/TOCTL (Page 5). The QDSX devices have dedicated lines XCLK_QSSX1 and XCLK_QDSX2

9.2.2 Sheet 2: E1/DS-1 LINE INTERFACE with DD-50 Connector

This Page 2 shows the physical interface to the Reference Design. The interface connector is a 50 pin D-Sub (DD-50) metal shell connector. The external mating plug is not shown on the schematic. Refer to this document for cable attachment pin-out.

The DD-50 connector provides an interface to the eight E1/DS-1 twisted pair lines. On the system side the interface lines are connected to the QDSX device (PM4314).

Characteristic impedance for E1 or DS-1 line interface is controlled with assembled resistors.

9.2.3 Sheet 3 and 4: QDSX - E1/DS-1 Line Interface Device

These Pages 3 and 4 show two QDSX devices (PM4314).

- Digital VDD is supplied from a common +5V plane. Each pin has associated 0.01 uF capacitor.
- Each analog RAVD and TAVD is supplied with RC networks to minimize the effects of interference from the power supply.

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- Series termination resistors in clock lines are provided to reduce the effects of reflections on signal edges.

9.2.4 Sheet 5: EOCTL/TOCTL AND CLOCK - E1/T1 Framer

This Page 5 shows an E1/T1 framing device EOCTL/TOCTL. Page includes also a clock distribution circuit.

The EOCTL device is assembled on the E1 line interface version of the Evaluation Card. TOCTL device is assembled on the T1 line interface version of the Evaluation Card. Crystal oscillator has appropriate frequency as required per E1 or T1 version.

Eight pairs of data/clock lines in ingress direction and eight pairs of data/clock in egress direction interfaces to FREEDM-8 (Page 6). Lines terminate at the IC as a single line buses. Clock lines TCLK<7..0> originate at the EOCTL/TOCTL device and are fed to slaved FREEDM-8.

Filtering capacitors are used on all EOCTL/TOCTL power pins for de-coupling the power supply noise.

Series termination resistors are provided on incoming clock lines (TLCLK and RLCLK) to reduce the effects of reflections on the signal edges.

The crystal oscillator provides clock signal to the EOCTL/TOCTL and QDSX devices. Series resistor and filtering capacitors are used to reduce noise to/from other circuitry on the Reference Design.

The 8-bit buffer is used to drive separate impedance controlled traces (75 ohm) to each of the EOCTL and QDSX device pins. Please refer to section 2.5 in this document for further information on the clock frequency.

9.2.5 Page 6: FREEDM-8 AND PCI BUS Interface

This sheet provides the frame relay processor using the PM7366 (FREEDM-8).

The PCI Interface is run to a card edge connector. The 3.3V power pins at the edge connector are not used since the commonly available motherboards do not provide power to the 3.3V pins and/or do not provide a 3.3V connector (or combined 5V/3.3V connector) on the motherboard. Instead, the power supply is provided by regulation of +5V as described at the schematic Page 7.

The PCI Bus provides two reset pins TRST# (A1) and RST# (A16). The RST# line is connected to FREEDM-8 and other devices.

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9.2.6 Page 7: FREEDM-8 - Power Supply

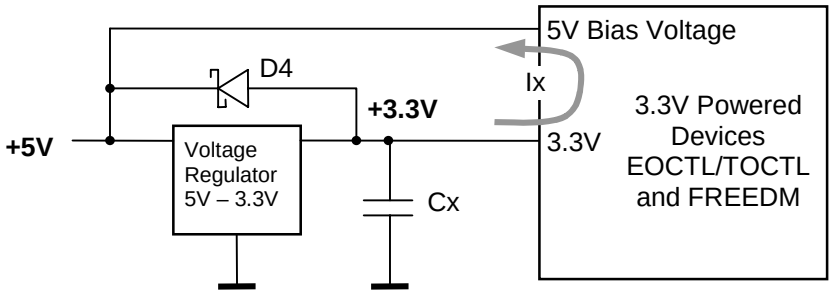
This sheet contains the 3.3V and the 5V power supplies for the Reference Design board. It also includes the bulk de-coupling capacitors for the PCI Bus connector.

- A+5V (VCC, VDD) is supplied from a PCI Bus connector. Optional power entry may be required if total current source exceeds the PCI Bus connector limits (for more information on current limits see reference [10]). The green LED D9 is used to signal presence of the +5V.
- A linear voltage regulator provides +3.3 V for the FREEDM-8 and EOCTL devices. The regulator LT11084_3_3V is supplied with +5V a decoupling capacitor. The green LED D3 is used to signal presence of the +3.3V.

NOTE: Green LEDs are employed to show presence of the supply voltage. However, the LEDs operate with wide voltage range on 5V or 3.3V rails, and emission of light can not be used as the only mean of a voltage level verification.

A Schottky diode is connected across 3.3V linear voltage regulator.

FIGURE 38. Schottky Diode.



The diode D4 ensures that the 3.3V will never be 0.5V above the 5V Bias Voltage lines during power-up and power-down cycles. If the 3.3V rail exceeds the 5V rail by 0.7V a permanent damage to the integrated circuit will result, as current Ix flows from a 3.3V rail and Cx through the IC into the 5V rail. Capacitor Cx represents the total added capacitance of filtering components.

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9.2.7 Sheet 8: MICROPROCESSOR INTERFACE – On-board MC68340

This sheet contains a 25MHz MC68340 microprocessor, a serial interface for user control and monitoring, a reset circuit, and a debug connector for software development. The following notes are provided for this sheet:

- MAX202 (U21) (+5V supply only, low cost) is used for the RS232 interface.
- A 3.6864MHz oscillator shown as Y4 is used for the RS232 interface.
- The reset circuit (based on 47HC03) resets the MC68340 and provides RSTB\I to reset all other devices.
- Background Debug Monitor (BDM) connector J20 is used for software development. Note that pin BKPTB must be pulled-up to VCC (through 4.7K). It is recommended that pin BERRB be pulled up also in a similar fashion. CLKOUT from the MC68340 needs to be connected to a test point (header connector) to be used with the BDM interface.
- XFC pin of the MC68340 needs to be de-coupled with 0.1uF to ground.
- XTAL must be left open if external oscillator used for EXTL, which is the case in this reference design
- VCCSYN needs to be pulled up to VCC and run through a power noise filter.
- MODCK has to be low on reset (a pull-down resistor is used)
- To avoid unintended coupling, pin floating, oscillations, all unused inputs are terminated with 4.7kΩ
- De-coupling Capacitors of 0.1uF (SMD 0603 size) are used for each power pin of the MC68340.

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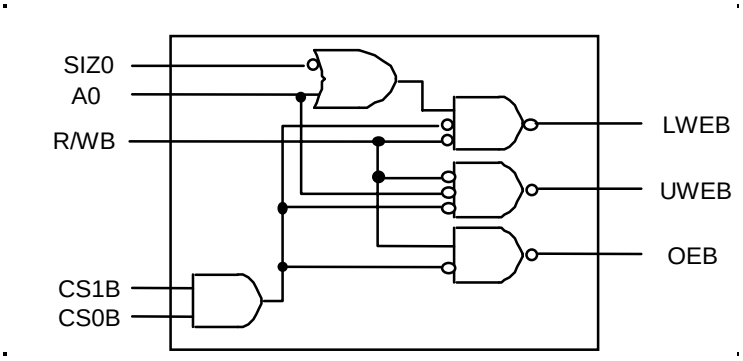
9.2.8 Sheet 9: MICROPROCESSOR INTERFACE - Decode Logic

This sheet contains decode logic for the MC68340 that is necessary to interface to the SRAM, the EPROM, the four EOCTL's and both QDSXs. The following notes are provided for this sheet:

- Address lines A_M0 through A_M17 of the MC68340 address bus are connected to external circuitry. The line drivers provided by U19/U20 serve to minimize loading of the MC68340 address outputs. To minimize nummber of different line transceivers, bi-directional devices are used for some buffers and for other transceivers where bidirectional devices are a must. The propagation delay for signals passed through the line drivers is within the maximum of 10ns for address valid to address strobe (AS) asserted, or for address valid to chip select (CS0, CS1, CS2, CS3) asserted.
- The data lines D_M[8..15] of the MC68340 are buffered with U17/U18 transceivers. One of the devices provides data path to the QDSXs and EOCTL/TOCTL. The other one serves microprocessor's memory devices.
- The 128k-word of SRAMs consisting of U14 and U15 is driven for read or write access by decode logic within a 22V10 PAL shown as U22.
- The address (chip select) decode logic is contained within a single PAL device U22. Internal logic is shown in FIGURE 39 and FIGURE 40 (below). Control lines originate on the MC68340 processor.

FIGURE 39. PAL Logic for Control Lines to SRAM



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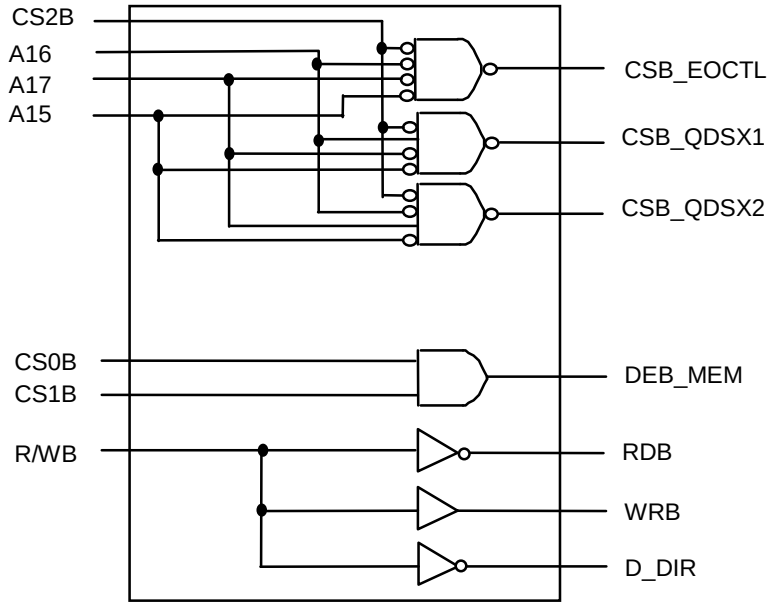
Note: CS1B and CS0B are AND'ed together (i.e. either CS0B or CS1B asserted) since the MC68340 always asserts CS0B during code download into SRAM using the background debug monitor, while it asserts CS1B during normal SRAM accesses. This applies to the case where only the SRAM is being used (typically during code development). If the ROM is used (which is selected by CS0B), then this AND gate should be removed, and only CS1B should be used here.

- CS0B of the MC68340 provides an active low chip select to the ROM shown as U13.
- CS2B of the MC68340 provide an active low chip select to the EOCTL/TOCTL and the QDSXs using the decode logic shown in FIGURE 40. The decode logic is implemented by the 22V10 PAL shown as U22 in the schematic. The RDB and WRB signals are also derived from the R/WB signal.
- The decode logic (below) also provides an output enable to the data transceiver U18 connected to the SRAM and ROM. CS2B is used as the output enable to the data transceiver U17.

FIGURE 40. PAL Logic for Control Lines



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- Wait states are required during read accesses to EOCTL and QDSX devices. The data sheet specifies a maximum propagation delay of 80ns, which implies that 1 wait-state is necessary to interface the MC68340 with each of these. The wait-state is programmed via a register within the MC68340 such that whenever the CS2B is active there is one wait-state inserted.

9.3 PCB Modification

The Revision 1 evaluation card must have some nets rewired and some wire jumpers may be visible. Make sure modifications are in place after handling and shipping.

Schematic marked Issue 1.1 has all errors removed and can be used error free as a reference for future designs.

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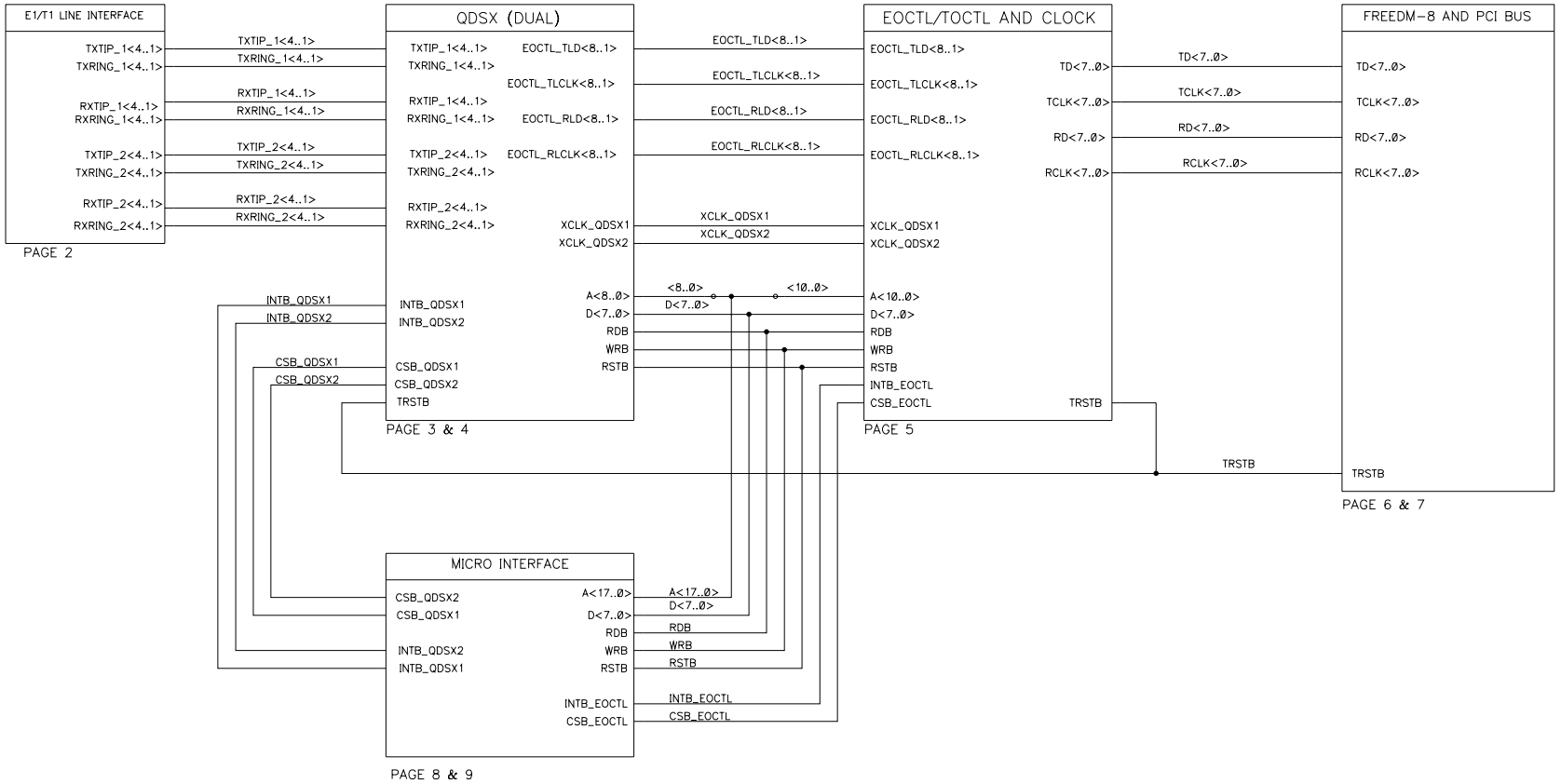
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



PRELIMINARY – SUBJECT TO CHANGE WITHOUT NOTICE

PAGE 1

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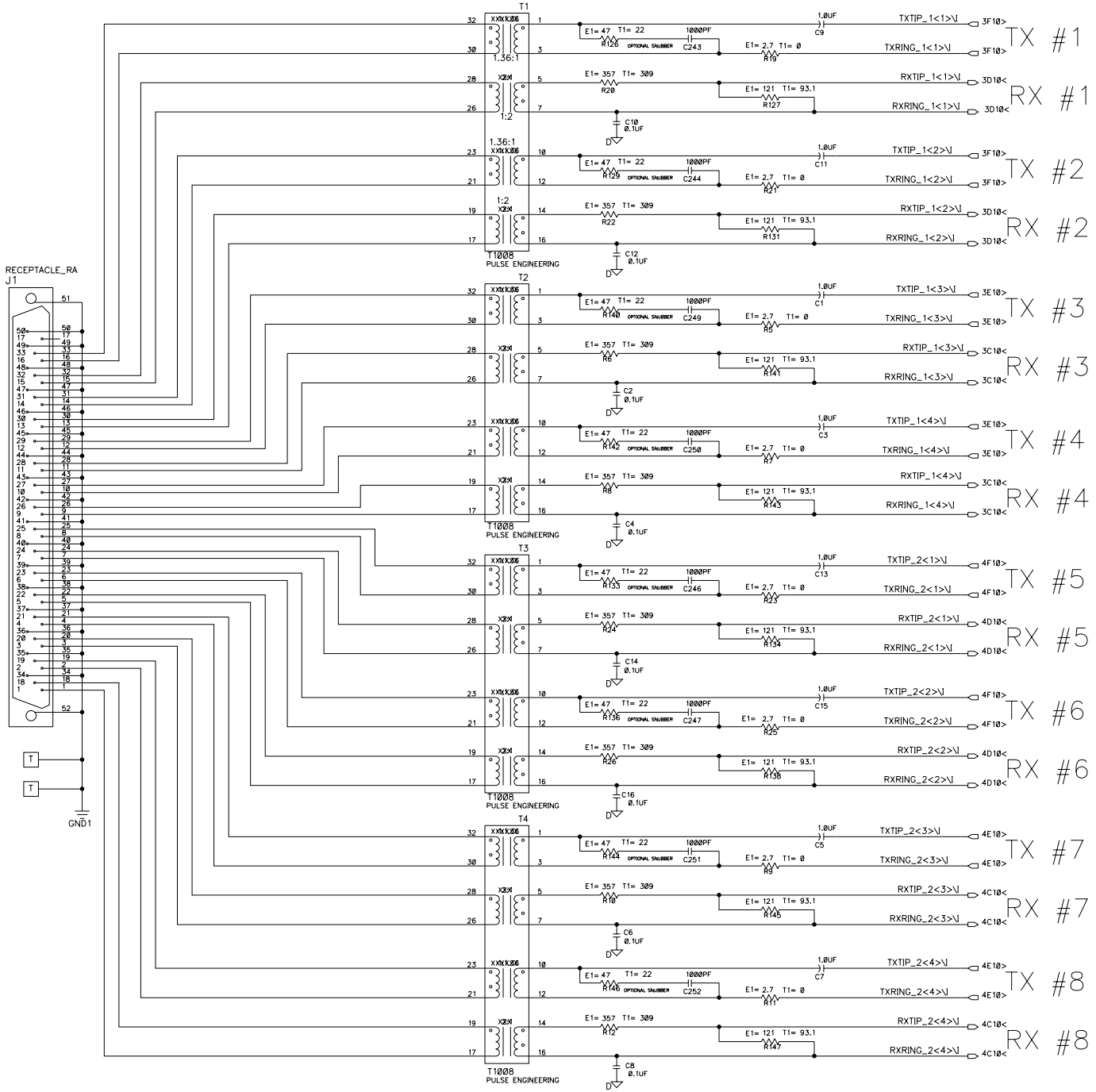
LAST_MODIFIED=Wed Aug 12 17:51:32 1998

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980474 *PRELIMINARY*	ISSUE: 1.1
TITLE: EOCTL/TOCTL REFERENCE DESIGN ROOT DRAWING	DATE: JULY/98
ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 1 OF 9



REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

E1/T1 LINE INTERFACE

TRANSMIT/RECEIVE

PRELIMINARY – SUBJECT TO CHANGE WITHOUT NOTICE

PAGE 2

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LAST_MODIFIED=Fri Aug 28 12:02:51 1998

PMC-Sierra, Inc.

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ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 2 OF 9

REVISIONS				
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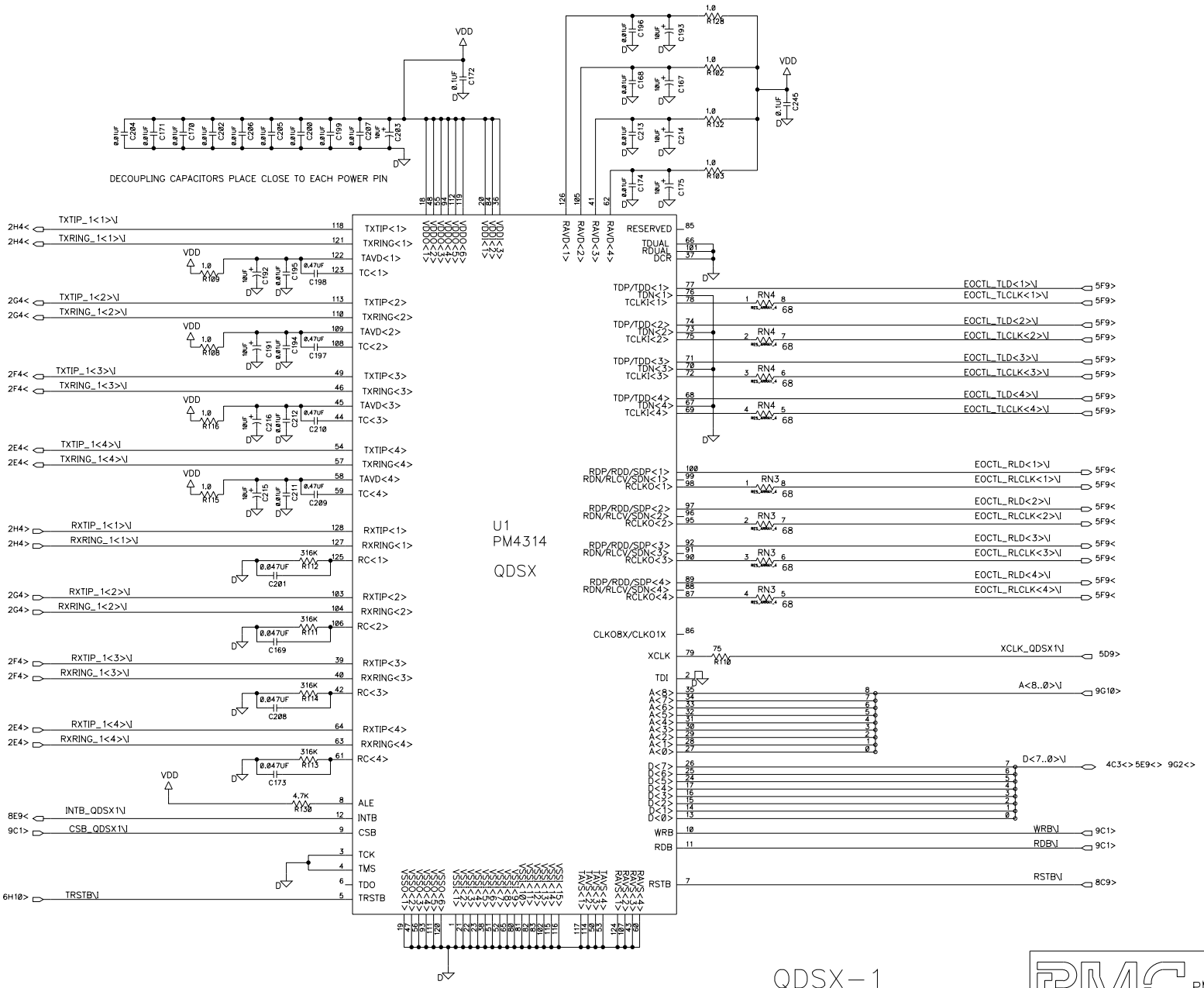

QDSX–1

PLS CHECK PIN 36 STATUS

PAGE 3

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LAST_MODIFIED=Fri Aug 28 12:02:58 1998

PMC-Sierra, Inc.

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ENGINEER: PMC_SIERRA INC. (WT)	PAGE: 3 OF 9

REVISIONS				
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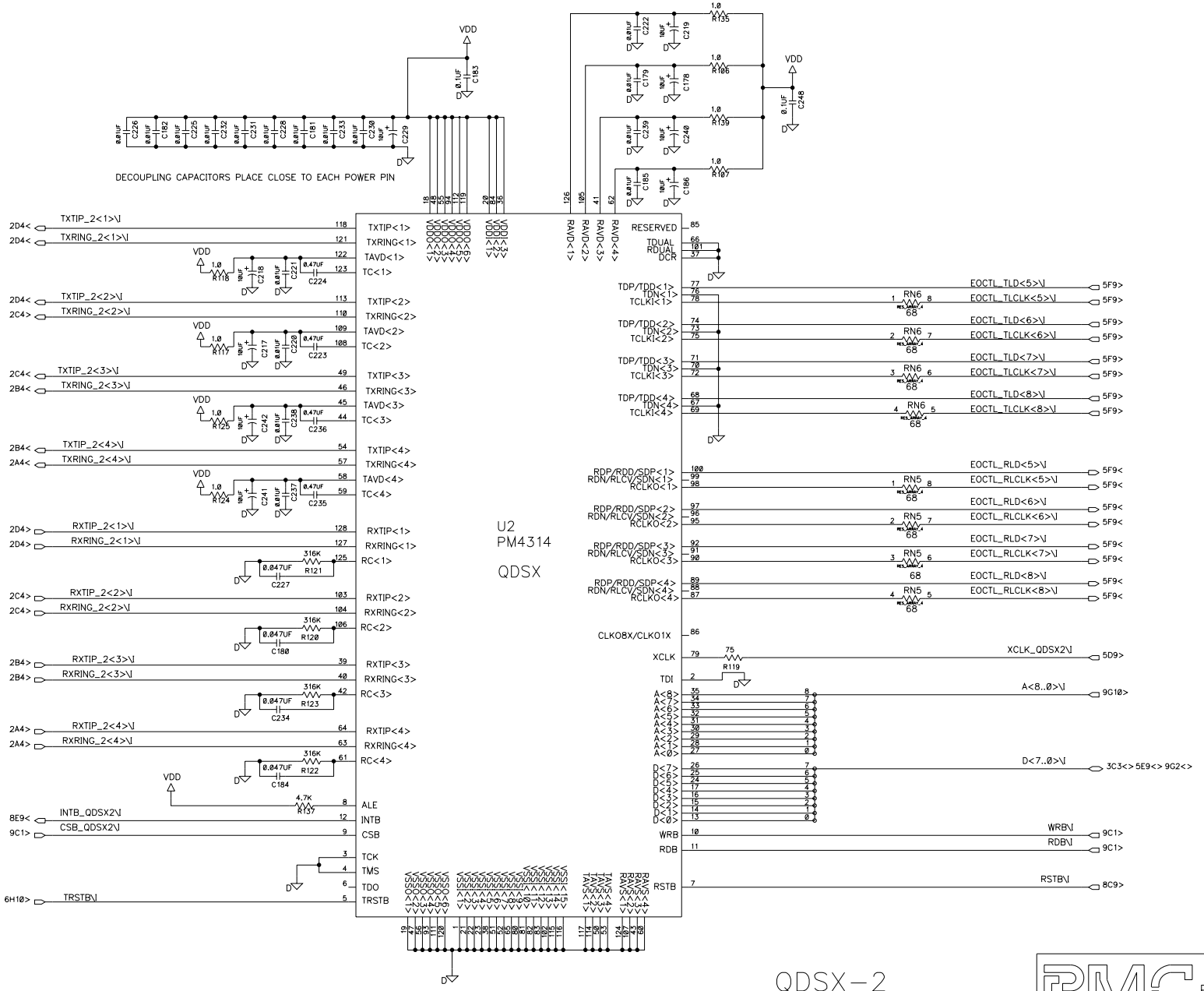

QDSX-2

PLS CHECK PIN 36 STATUS

PAGE 4

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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980474 *PRELIMINARY*	ISSUE: 1.1
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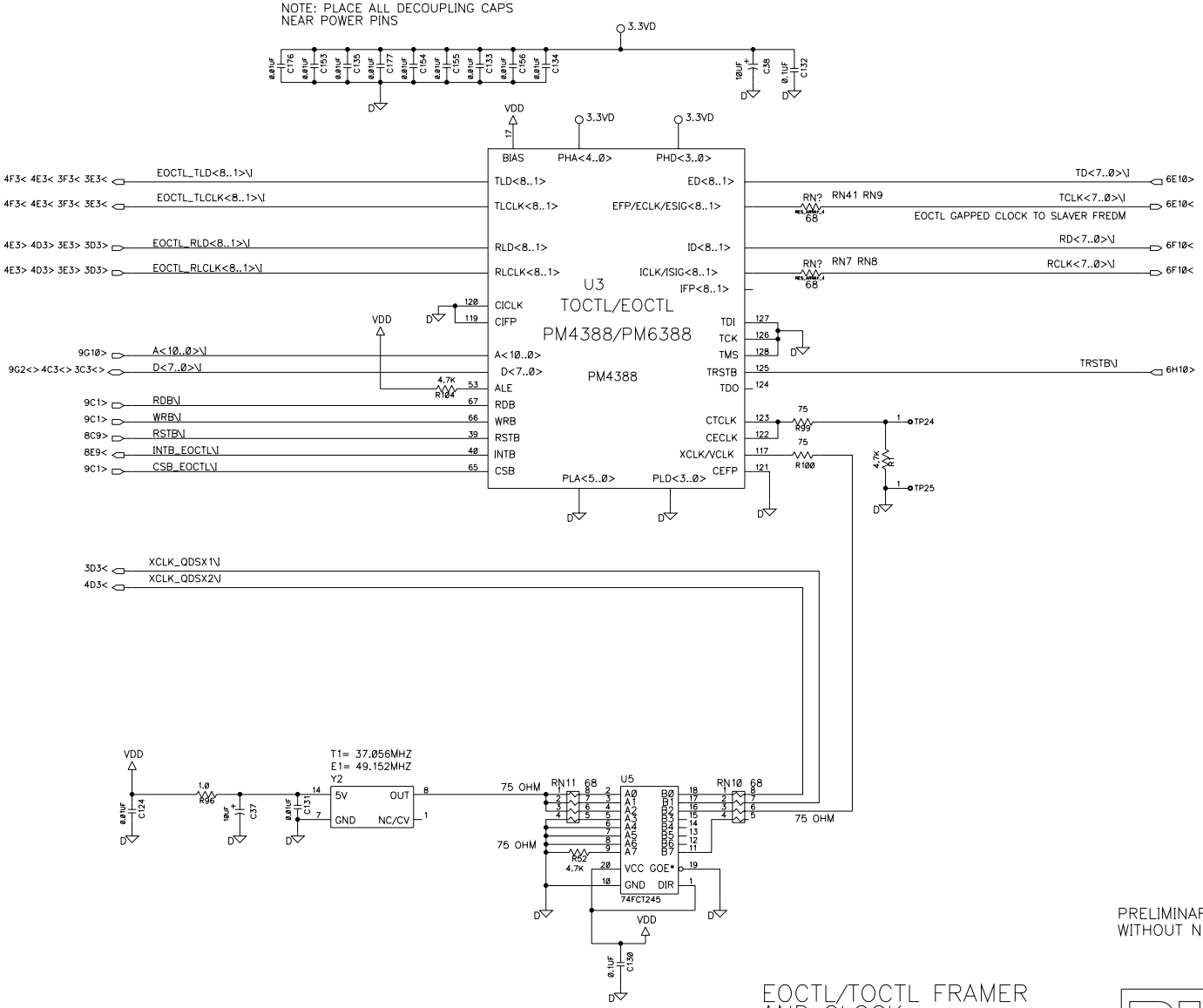
ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 4 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

EOCTL/TOCTL E1/T1 FRAMER



PRELIMINARY – SUBJECT TO CHANGE WITHOUT NOTICE

EOCTL/TOCTL FRAMER AND CLOCK

PAGE 5

DRAWING

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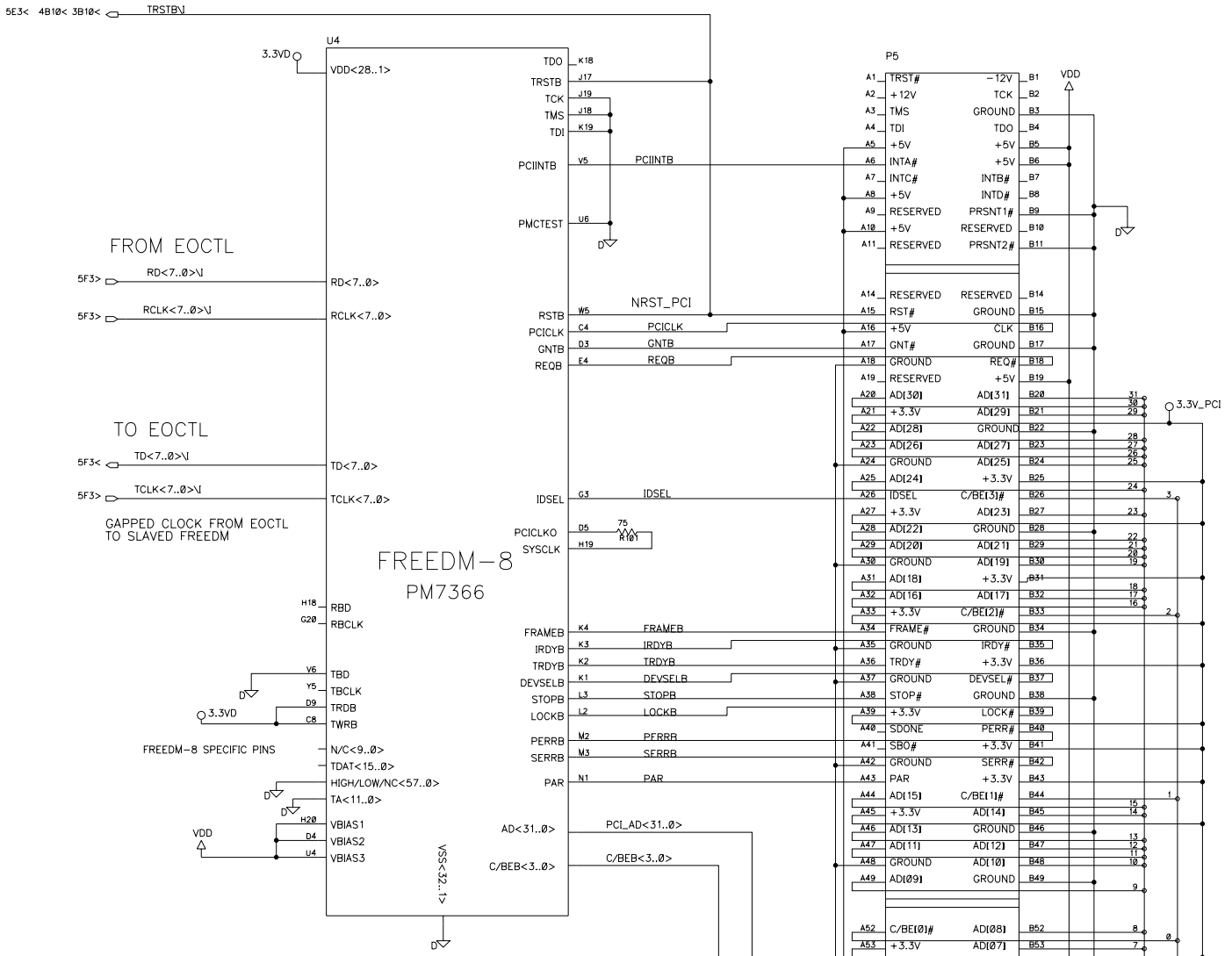
LAST_MODIFIED=Fri Aug 28 12:02:54 1998

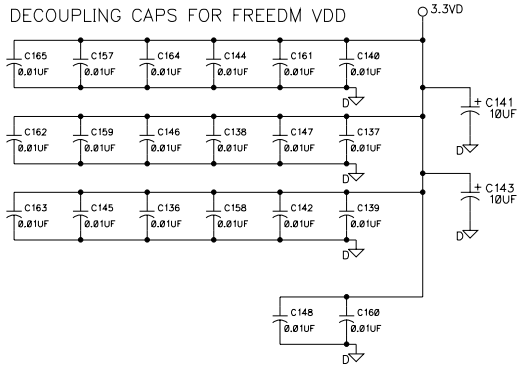
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980474 *PRELIMINARY*	ISSUE: 1.1
TITLE: EOCTL/TOCTL REFERENCE DESIGN SINGLE EOCTL	DATE: JULY/98
ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 5 OF 9

FREEDM AND PCI CONNECTOR

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





NOTE

CHECK THE LATEST PCI SPEC FOR
COMPONENT AND LAYOUT RESTRICTIONS FOR:

1. DATA TRACE MAXIMUM LENGTH
2. CLOCK (CLK) TRACE MAXIMUM LENGTH
3. TRACE IMPEDANCE CONTROL

PAGE 6

DRAWING
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ABBREV=FREEDM
LAST_MODIFIED=Fri Aug 28 12:02:45 1998

PRELIMINARY – SUBJECT TO CHANGE
WITHOUT NOTICE

PMC-Sierra, Inc.

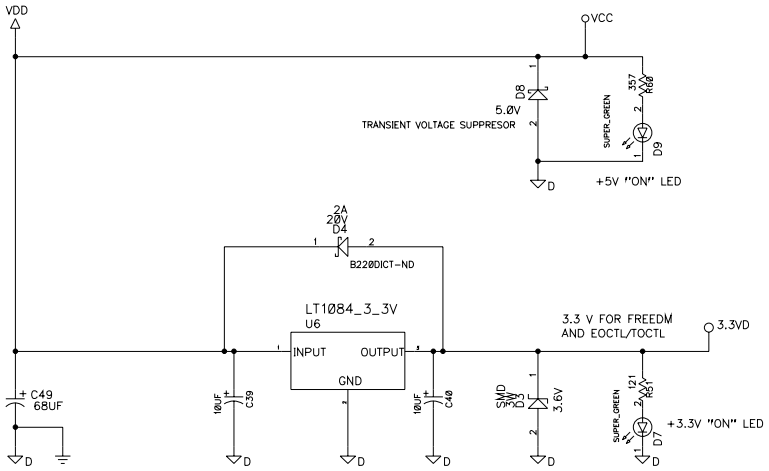
DOCUMENT NUMBER: PMC-980474	ISSUE: 1.1
TITLE: EOCTL/TOCTL REFERENCE DESIGN FREEDM SHT 1/2	DATE: JULY/98
ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 6 OF 9

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

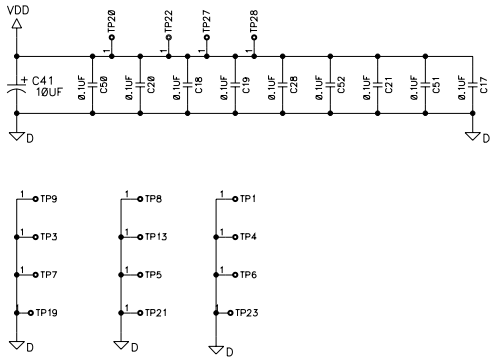
POWER AND DECOUPLING

NOTE:
DECOUPLING CAPS ARE USED FOR
PCI BUS POWER RAIL.
THEY SHOULD BE PLACED IN SUCH A WAY THAT
AT LEAST AN AVERAGE OF 0.01UF PER
VCC PIN IS ACHIEVED.

+5V FOR FREEDM AND EOCTL/TOCTL
IS AWAYS FED FROM THE PCI BUS



A SINGLE GROUND PLANE USED



PRELIMINARY – SUBJECT TO CHANGE
WITHOUT NOTICE

FREEDM-8 – POWER SUPPLY

PAGE 7

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LAST_MODIFIED=Fri Aug 28 12:02:48 1998

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980474	ISSUE: 1.1
TITLE: EOCTL/TOCTL REFERENCE DESIGN FREEDM PAGE 2/2	DATE: JULY/98
ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 7 OF 9

MICROPROCESSOR CIRCUIT

REVISIONS				
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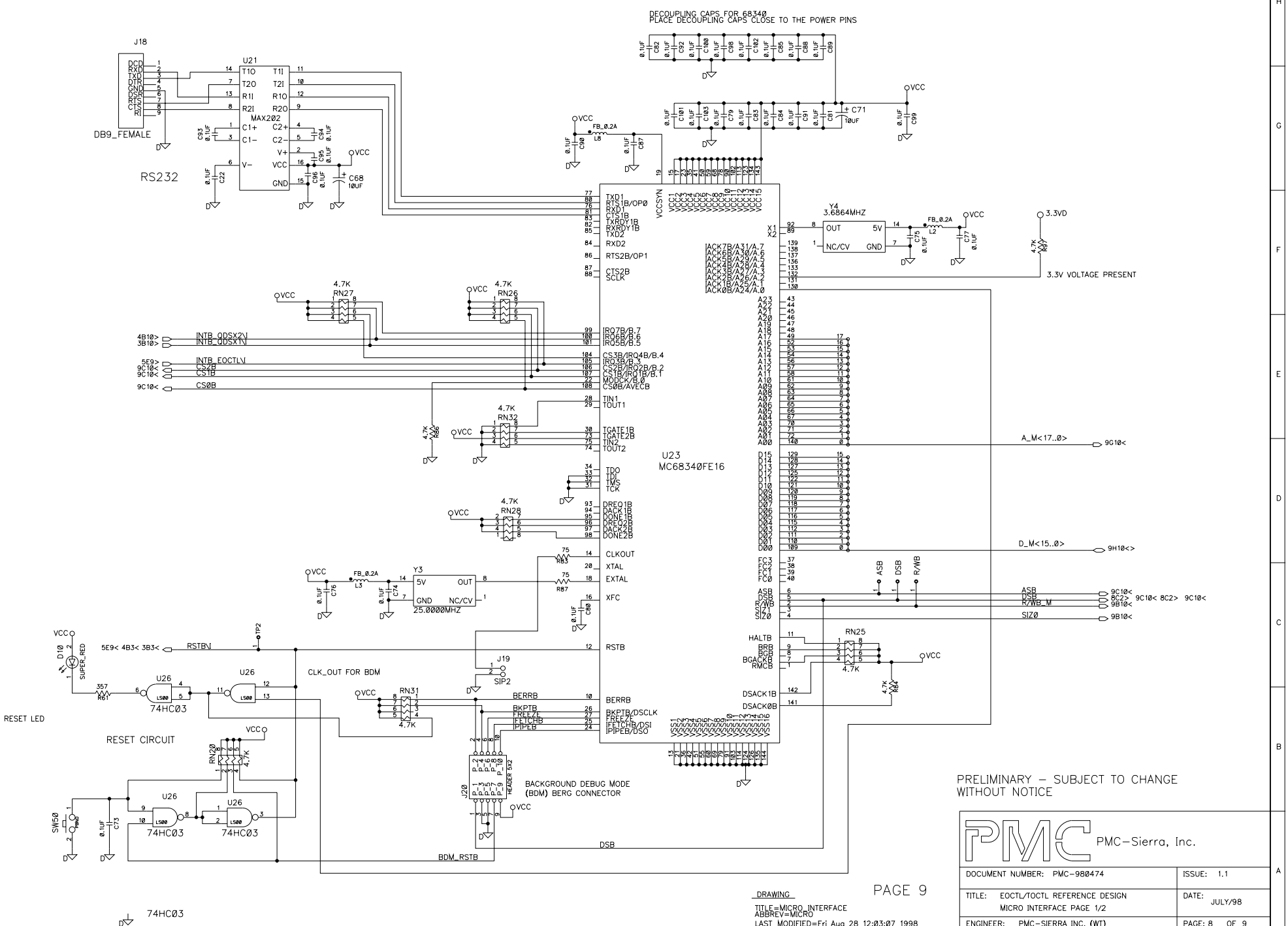

PRELIMINARY – SUBJECT TO CHANGE WITHOUT NOTICE

PAGE 9

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LAST_MODIFIED=Fri Aug 28 12:03:07 1998

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980474	ISSUE: 1.1
TITLE: EOCTL/TOCTL REFERENCE DESIGN MICRO INTERFACE PAGE 1/2	DATE: JULY/98
ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 8 OF 9

MICROPROCESSOR MEMORY

REVISIONS				
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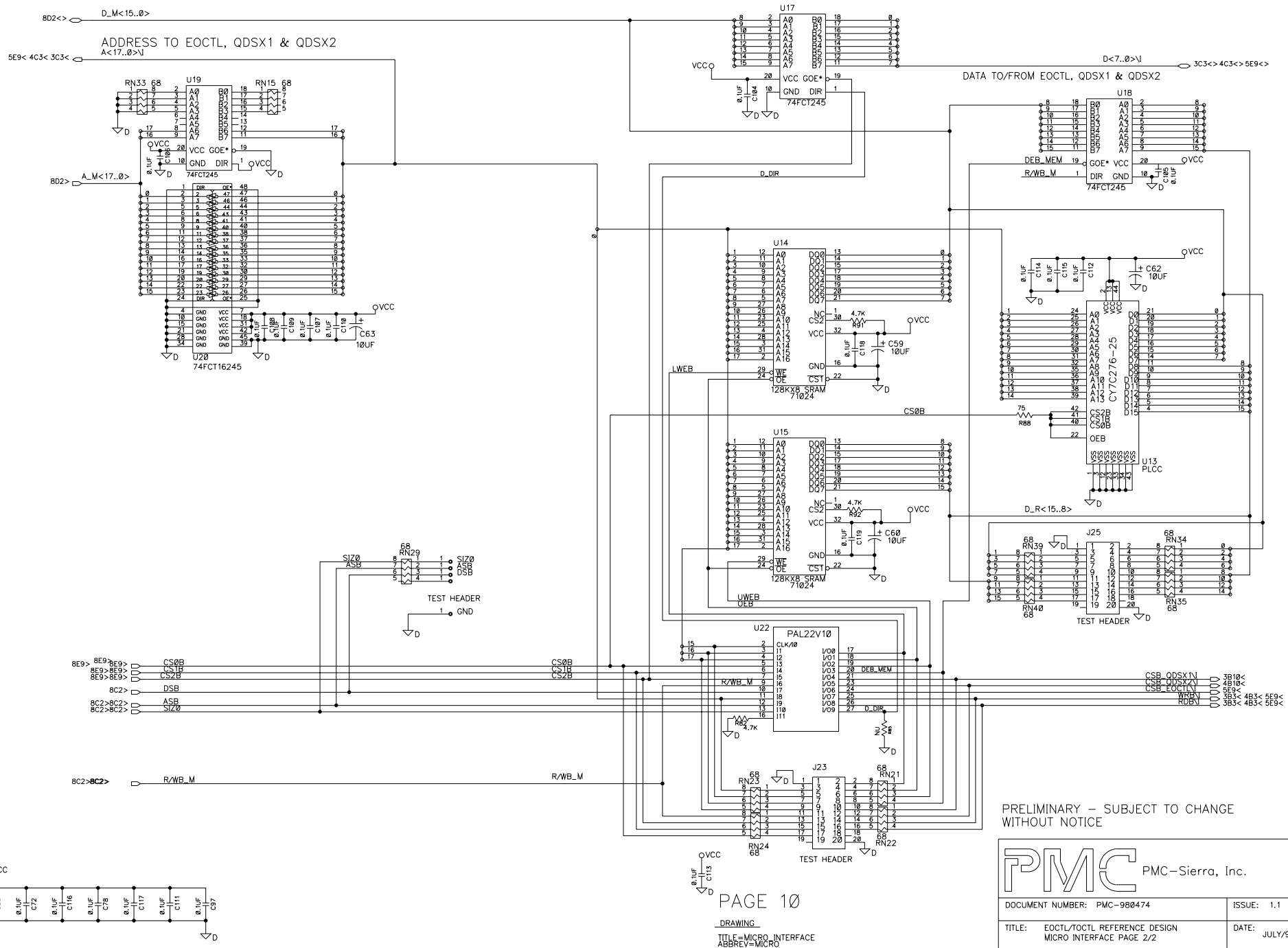

PRELIMINARY – SUBJECT TO CHANGE WITHOUT NOTICE

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-980474	ISSUE: 1.1
TITLE: EOCTL/TOCTL REFERENCE DESIGN MICRO INTERFACE PAGE 2/2	DATE: JULY/98
ENGINEER: PMC-SIERRA INC. (WT)	PAGE: 9 OF 9

PAGE 10

DRAWING

TITLE=MICRO_INTERFACE
ABBREV=MICRO
LAST_MODIFIED=Fri Aug 28 12:03:12 1998

10 GLOSSARY

Bit Stuffing	A process in data communications protocols, where a string of "one" bits in the data payload is broken by an inserted "zero". The idea of inserting the zero is to ensure that no flag control character is found in the user payload.
CRC	Cyclic Redundancy Check: Check sums generated from recursive algorithms that can be used to determine the integrity of data by a receiver. Certain CRC algorithms allow the receiver to detect as well as correct certain number of bit errors.
DLCI	Data Link Connection Identifier (DLCI). The frame relay virtual circuit number corresponding to a particular destination which is part of the frame relay header and is usually ten bits long. The DLCI is typically associated with particular PVC on the network.
DS-0	Digital Service, level 0. There are 24 DS-0 channels in a DS-1. Each DS-0 has a bandwidth of 64 kbit/s.
DS-1	Digital Service, level 1: It is 1.544 Mbit/s in North America. In channelized mode, each DS-1 consists of 24 DS-0 channels. In unchannelized mode, each DS-1 has a full-duplex bandwidth of 1.544 Mbit/s.
DS-3	Digital Service, level 3. DS-3 is equivalent to 28 DS-1 channels. It operates at 44.736 Mbit/s.
DSLAM	Digital Subscriber Loop Access Multiplexer.
E1	Digital Service, level 1. It is 2.048 Mbit/s in Europe.
FCS	Frame Check Sequence. Bits added to the end of a frame for error detection. In bit-oriented protocols, a frame check sequence is a 16-bit field added to the end of a frame that contains transmission error-checking information.
Flag	In synchronous transmission, a flag is a pattern of "01111110" used to mark the beginning and end of a frame.
FRAD	Frame Relay Access Device.

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Frame	A frame is also referred to as a "packet" and is a logical transmission unit. A frame consists of a group of data bits in a specific format. Generally, a flag is used at each end of the frame to delimit the start and end of the frame.
Frame Relay	The term "frame relay" is used in multiple contexts and can be used to refer to a switching technology, an interface standard or a set of data services.
Full-Duplex	Refers to simultaneous transmission in two directions.
FUNI	Frame Relay User Network Interface.
HDLC	High Level Data Link Control. A standard bit-oriented protocol developed by ITU.
HSSI	High Speed Serial Interface.
ISP	Internet Service Provider.
Multiplexer	Electronic equipment, which allows two or more signals to pass over one communication, circuit.
NAP	Network Access Point.
OSI	Open System Interconnect. An ISO publication that defines seven independent layers of communication protocols. Each layer enhances the communication services of the layer just below it and shields the layer above it from the implementation details of the lower layer.
OSI Model	The only internationally accepted framework of standards for communication between different systems made by different vendors. The OSI model organizes the communications process into the following seven layers: Layer 1 - Physical Layer Layer 2 - Data Link Layer Layer 3 - Network Layer Layer 4 - Transport Layer Layer 5 - Session Layer Layer 6 - Presentation Layer Layer 7 - Application Layer
Packet	A packet is also referred to as a "frame" and is a logical transmission unit.
PCI	Peripheral Component Interconnect.

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POP	Point of Presence. In telecommunication, POP refers to the physical place within a LATA where a long distance carrier interfaces with the network of the local exchange carrier.
UNI	User Network Interface. The physical and electrical demarcation point between the user and the public network service provider.

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11 APPENDIX A. PAL VHDL TEXT FILE

11.1 ROM Version of PAL

The VHDL text file for ROM version of the U22 PAL device is shown below.

```
-- EOCTL/TOCTL with FREEDM-8 reference design ver1.0
-- 22V10 PAL U22 for operation with ROM
--
-- Function:
--      logic for chip selects
-- Author:
--      PMC-Sierra Inc. (WT)
-- History:
--      Aug 04, 1998    Created.
-- Description:
--      Generates Chip selects, read, write and address enable
--


USE work.rtlpkg.all;
USE work.cypress.all;
ENTITY u22_pal IS
PORT   (
a15, a16, a17, cs0b, cs1b, cs2b, rwb, dsb, a0, asb, siz0: IN BIT;
lweb, oeb, uweb, deb_mem, csb_qdsx1, csb_qdsx2, csb_eoctl, wrb, rdb,
rdb1: OUT BIT);

ATTRIBUTE order_code of u22_pal:ENTITY is "PAL22V10D-25JC";
ATTRIBUTE part_name of u22_pal:ENTITY IS "C22V10";
ATTRIBUTE pin_numbers of u22_pal:ENTITY IS
 "a15:2  " &
 "a16:3  " &
 "a17:4  " &
 "cs0b:5     " &
 "cs1b:6     " &
 "cs2b:7     " &
 "rwb:9     " &
 "dsb:10     " &
 "a0:11     " &
 "asb:12     " &
 "siz0:13     " &
 "lweb:17     " &
 "oeb:18     " &
```


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```
 "uweb:19     " &
 "deb_mem:20     " &
 "csb_qdsx1:21    " &
 "csb_qdsx2:23     " &
 "csb_eoctl:24     " &
 "wrb:25     " &
 "rdb:26     " &
 "rdb1:27     " ;
END u22_pal;

ARCHITECTURE behavior OF u22_pal IS
--
BEGIN
 lweb <= not(((not siz0)or(a0))and(not cs1b)and(not rwb));
 oeb  <= not ( rwb and (not cs1b));
 uweb  <= not ((not rwb) and (not a0) and (not cs1b));
 deb_mem <= cs0b and cs1b;
 csb_eoctl <= not ((not cs2b) AND (not a15) AND (not a16) AND (not a17));
 csb_qdsx1 <= not ((not cs2b) AND (not a15) AND (    a16) AND (not a17));
 csb_qdsx2 <= not ((not cs2b) AND (not a15) AND (not a16) AND (    a17));
 wrb <= rwb;
 rdb <= NOT rwb;
 rdb1 <= NOT rwb;
END behavior;
```


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11.2 BDM Version of PAL

The VHDL text file for BDM version of the U22 PAL device is shown below.

```
-- EOCTL/TOCTL with FREEDM-8 reference design ver1.0
-- 22V10 PAL U22 for operation with BDM
--
-- Function:
--      logic for chip selects
-- Author:
--      PMC-Sierra Inc. (WT)
-- History:
--      Aug 04, 1998    Created.
-- Description:
--      Generates Chip selects, read, write and address enable
--


USE work.rtlpkg.all;
USE work.cypress.all;
ENTITY u22_pal IS
PORT   (
a15, a16, a17, cs0b, cs1b, cs2b, rwb, dsb, a0, asb, siz0: IN BIT;
lweb, oeb, uweb, deb_mem, csb_qdsx1, csb_qdsx2, csb_eoctl, wrb, rdb,
rdb1: OUT BIT);

ATTRIBUTE order_code of u22_pal:ENTITY is "PAL22V10D-25JC";
ATTRIBUTE part_name of u22_pal:ENTITY IS "C22V10";
ATTRIBUTE pin_numbers of u22_pal:ENTITY IS
 "a15:2  " &
 "a16:3  " &
 "a17:4  " &
 "cs0b:5     " &
 "cs1b:6     " &
 "cs2b:7     " &
 "rwb:9     " &
 "dsb:10     " &
 "a0:11     " &
 "asb:12     " &
 "siz0:13     " &
 "lweb:17     " &
 "oeb:18     " &
 "uweb:19     " &
 "deb_mem:20     " &
 "csb_qdsx1:21    " &
 "csb_qdsx2:23     " &
```


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```
 "csb_eoctl:24     " &
 "wrb:25     " &
 "rdb:26     " &
 "rdb1:27     " ;
END u22_pal;

ARCHITECTURE behavior OF u22_pal IS
--
BEGIN
 lweb <= not(((not siz0)or(a0))and(not(cs1b and cs0b))and(not rwb));
 oeb  <= not ( rwb and (not(cs1b and cs0b)));
 uweb  <= not ((not rwb) and (not a0) and (not(cs1b and cs0b)));
 deb_mem <= cs0b and cs1b;
 csb_eoctl <= not ((not cs2b) AND (not a15) AND (not a16) AND (not a17));
 csb_qdsx1 <= not ((not cs2b) AND (not a15) AND (    a16) AND (not a17));
 csb_qdsx2 <= not ((not cs2b) AND (not a15) AND (not a16) AND (    a17));
 wrb <= rwb;
 rdb <= not rwb;
 rdb1 <= not rwb;
END behavior;
```


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12 APPENDIX B. SCHEMATICS

Schematic hardcopy is attached.

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13 APPENDIX C: BILL OF MATERIALS

13.1 Bill of Materials for E1 Interface with EOCTL

TABLE 9. E1 Interface with EOCTL

Item	Description	Vendor Part No.	Reference Designator	Qty
1	QDSX, E1/T1 Short Haul Line Interface IC	PM4314 PMC-Sierra Inc.	U1, U2	2
2	**E1 BOARD.** EOCTL, OCTAL E1 FRAMER, PQFP_128	PM6388 PMC-Sierra Inc.	U3	1
3	FREEDM-8 (FRAME RELAY PROTOCOL ENGINE AND DATA LINK MANAGER)	PM7366	U4	1
4	LINEAR VOLTAGE REGULATOR, 3.3V, 3A, TO-220	LT1084-3.3 LINEAR TECHNOLOGY	U6	1
5	NON-INV OCTAL TRANSCEIVER (SOIC-20)	PI74FCT245ATS-ND DIGI-KEY	U5, U17, U18, U19	4
6	CYPRESS 16K X 16 PROM, PLCC44	CY7C276-25JC CYPRESS ARROW-ELECTRONICS	(U13) – MOUNTED INTO SOCKET	1
7	128K BY 8 STATIC RAM	IDT71024S15TY FAI ELECTRONICS	U14, U15	2
8	NON-INV 16-BIT BUFFER (SSOP-48)	PI74FC16245ATV-ND DIGI-KEY	U20	1
9	RS2332 TRANSCEIVER	MAX202CPP-ND DIGI-KEY	U21	1
10	QUAD 2 INPUT NAND GATE OC (SOIC –14)	CD74HCT03M	U26	1
11	MC68340 MOTOROLA CPU, 25MHz, PQFP144	MC68340FE25E FAI-ELECTRONICS	U23	1
12	PAL DEVICE, PLCC-28	PALCE22V10H-25JC FAI-ELECTRONICS	(U22)– MOUNTED INTO SOCKET	1
13	DD-50 D-SUB CONNECTOR, METAL SHELL, RIGHT ANGLE, PCB MOUNT	M24308/23-35 ITT/CANNON 95F6022 NEWARK	J1	1
14	DE-9 D-SUB CONNECTOR, STRAIGHT PCB MOUNT	A2100-ND DIGI-KEY	J18	1
15	PLCC SOCKET, 28 PIN, SMD	A2141-ND DIGI-KEY	U22	1
16	PLCC SOCKET, 44 PIN, SMD	A2142-ND DIGI-KEY	U13	1
17	OPTIONAL BDM 1x2 HEADER	ANY	J19	(1)
18	2x5 SHROUDED HEADER	92N3713 NEWARK	J20	1
19	SINGLE PIN TEST HEADER	ANY	TP1-TP28	28

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20	**E1/T1 BOARD OPTIONAL SNUBBER**: CERAMIC CAPACITOR-1000PF, 50V, X7R	PCC102BVCT-ND DIGI-KEY	C243,C244,C246, C247,C249-C252	(8)
21	CERAMIC CAPACITOR 0.01UF, 16V, YV5, 0603	PCC103BVTR-ND DIGI KEY	C124, C131, C133-C140, C142, C144-C148, C153-C165, C168, C170, C171, C174, C176, C177, C179, C181, C182, C185, C194-C196, C199, C200, C202, C204-C207, C211-C213, C220-C222, C225, C226, C228, C230-C233, C237-C239	65
22	CERAMIC CAPACITOR 0.047UF, 25V, X7R, 0603	VJ0603Y473KXXMX VISHAY NEWARK	C169, C173, C180, C184, C201,C208, C227, C234	8
23	CERAMIC CAPACITOR-0.1UF, 25V, Y5V, 0603	VJ0603Y104KXXMX VISHAY NEWARK	C2, C4, C6, C8, C10, C12, C14, C16, C17-C21, C28, C50, C51, C52, C72-C119, C130, C132, C172, C183, C245, C248	71
24	CERAMIC CAPACITOR 0.47UF, 16V, X7R, 0805	EMK212BJ474KG TAYIO YUDEN	C197, C198, C209, C210, C223, C224, C235, C236	8
25	CERAMIC CAPACITOR 1UF, 16V, X7R, 1206	EMK316BJ105KF-T TAYIO YUDEN	C1, C3, C5, C7, C9, C11, C13, C15	8
26	CAPACITOR-10UF, 6.3V, TANTALUM THE, SMD	PCS1106CT-ND DIGI-KEY	C37-C41,C59, C60, C62, C63, C68, C71, C141, C143,C167,C175, C178,C186, C191-C193,C203, C214-C219,C229, C240-C242,	31
27	CAPACITOR-68UF, 6.3V, TANTALUM THE	PCT1686CT-ND DIGI-KEY	C49	1
28	TRANSIENT VOLTAGE SUPPRESSOR, 5V	SA5.0AGICT-ND DIGI-KEY	D8	1
29	ZENER DIODE, 3.6V, 1W, SMD	1SMB5914BT3 NEWARK	D3	1
30	SCHOTTKY DIODE, 2A, 20V, SMB_2	B220DICT-ND DIGI-KEY	D4	1
31	FERRITE BEAD, 0.2A, 1206	240-1019-1-ND DIGI-KEY	L2,L3,L8	3
32	LED-RED, PCB MOUNTED	LU60361CT-ND DIGI-KEY	D10	1
33	LED-GREEN, PCB MOUNTED	LU60355CT-ND DIGI-	D7, D9	2

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		KEY		
34	OSC_TTL DIP-25.0000M HZ, 100 PPMA	CTX176-ND DIGI-KEY	Y3	1
35	OSC_TTL DIP-3.6864MH Z, 100 PPM, A	CTX154-ND DIGI-KEY	Y4	1
36	**E1 BOARD:** CRYSTAL OSC CMOS,-49.152MHZ, 50 PPM, DIP8	MB050H-49.152MHZ MMD	Y2	1
37	RESET SWITCH	P8009S-ND DIGI-KEY	SW50	1
38	E1/T1 LINE INTERFACE QUAD TRANSFORMER	T1008 PULSE ENGINEERING	T1, T2, T3, T4	4
39	RESISTOR, 1 OHM, 5%, 0805	P1.0BCT-ND DIGI-KEY	R96, R102, R103, R106-R109, R115-R118, R124, R125, R128, R132, R135, R139	17
40	**E1 BOARD OPTIONAL SNUBBER:** RESISTOR, 47 OHM, 5%, 0805	P47ACT-ND DIGI-KEY	**E1 BOARD OPTIONAL SNUBBER:** R126, R129, R133, R136, R140, R142, R144, R146	(8)
41	**E1 BOARD:** RESISTOR, 18 OHM, 5%, 0805	P18ACT-ND DIGI-KEY	**E1 BOARD:** R5, R7, R9, R11, R19, R21, R23, R25	8
42	RESISTOR, 75 OHM, 5%, 0805	P75ACT-ND DIGI-KEY	R81,R83,R87, R88, R99-R101, R110, R119	9
43	RESISTOR ARRAY 4x68 OHM, SMD 1206	Y468CT-ND DIGI-KEY	RN3-RN11, RN33-RN35, RN39-RN41	15
44	RESISTOR ARRAY 4x4.7K OHM, SMD 1206	Y4472CT-ND DIGI-KEY	RN20, RN25-RN28, RN31, RN32	7
45	**E1 BOARD:** RESISTOR, 121 OHM, 1%, 0805	P121CCT-ND DIGI-KEY	**E1 BOARD:** R127, R131, R134, R138, R141, R143,R145, R147	9
46	RESISTOR, 121 OHM, 1%, 0805	P121CCT-ND DIGI-KEY	R51	1
47	**E1 BOARD:** RESISTOR, 357 OHM, 1%, 0805	P357CCT-ND DIGI-KEY	**E1 BOARD:** R6,R8, R10, R12,R20,R22, R24,R26,	8
48	RESISTOR, 357 OHM, 1%, 0805	P357CCT-ND DIGI-KEY	R60,R61	2
49	RESISTOR- 4.7K, 5%, 0805	P4.7KACT-ND DIGI-KEY	R1, R52, R82, R84-R86, R91, R92, R97, R104, R130, R137	12
50	RESISTOR-316K, 1%, 0805	P316KCCT-ND DIGI-KEY	R111-R114, R120-R123	8
51	PCI BUS CARD BRACKET	PER PMC-SIERRA DRAWING	PMC-BRACKET1	1

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52	SCREW, 4-40 x ¼	ANY	SCREW1, SCREW2	2
53	NUT, 4-40 x ¼	ANY	NUT1, NUT2	2
55	RESISTOR, 0 OHM, 5%, 0805	0805, ANY BRAND	R79	1
Following Parts are external to the Evaluation Card				
54	DD-50 D-SUB CONNECTOR, METAL SHELL, STRAIGHT, (SOLDER CUP)	1492 SPC 92N3449 NEWARK	P61	(1)
55	DD-50 D-SUB METAL SHELL SET, STRAIGHT	51N1298 NEWARK	HW1	(1)
56	D-SUB CONNECTOR MOUNTING SCREW SET	ANY	HW2	(1)
57	SHIELDED TWISTED PAIR, 18CM LONG	TBD	HW3-HW18	(16)
58	ADC BANTAM CONNECTORS	PC-834-J-RED ELECTROSONIC	J51-J58	(8)
59	ADC BANTAM CONNECTORS	PC-834-J-BLUE ELECTROSONIC	J59-J66	(8)
60	HEAT SHRINK TUBING, BLUE, RED AND BLACK	ANY		
Following Parts are used for troubleshooting microprocessor circuit and are not assembled on the Evaluation Card				
61	TEST RECEPTACLE, CONNECTOR NOT ASSEMBLED	A3103-ND DIGI-KEY	(J23, J25)	(2)
62	TEST HEADER. CONNECTOR ATTACHED TO A TEST CABLE	A3107-ND DIGI-KEY	(J101, 102)	(2)
45	RESISTOR ARRAY 4x68 OHM, SMD 1206	Y468CT-ND DIGI-KEY	RN15, RN21, RN22, RN23, RN24, RN29,	6

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13.2 Bill of Materials for DS-1 Interface with TOCTL

Item	Description	Vendor Part No.	Reference Designator	Qty
1	QDSX, E1/T1 Short Haul Line Interface IC	PM4314 PMC-Sierra Inc.	U1, U2	2
2	**T1 BOARD.** TOCTL, OCTAL T1 FRAMER, PQFP_128	PM4388 PMC-Sierra Inc.	U3	1
3	FREEDM-8 (FRAME RELAY PROTOCOL ENGINE AND DATA LINK MANAGER)	PM7366	U4	1
4	LINEAR VOLTAGE REGULATOR, 3.3V, 3A, TO-220	LT1084-3.3 LINEAR TECHNOLOGY	U6	1
5	NON-INV OCTAL TRANSCEIVER (SOIC-20)	PI74FCT245ATS-ND DIGI-KEY	U5, U17, U18, U19	4
6	CYPRESS 16K X 16 PROM, PLCC44	CY7C276-25JC CYPRESS ARROW ELECTRONICS	(U13) – MOUNTED INTO SOCKET	1
7	128K BY 8 STATIC RAM	IDT71024S15TY FAI ELECTRONICS	U14, U15	2
8	NON-INV 16-BIT BUFFER (SSOP-48)	PI74FC16245ATV-ND DIGI-KEY	U20	1
9	RS2332 TRANSCEIVER	MAX202CPP-ND DIGI-KEY	U21	1
10	QUAD 2 INPUT NAND GATE OC (SOIC –14)	CD74HCT03M	U26	1
11	MC68340 MOTOROLA CPU, 25MHz, PQFP144	MC68340FE25E FAI-ELECTRONICS	U23	1
12	PAL DEVICE, PLCC-28	PALCE22V10H-25JC FAI-ELECTRONICS	(U22)– MOUNTED INTO SOCKET	1
13	DD-50 D-SUB CONNECTOR, METAL SHELL, RIGHT ANGLE, PCB MOUNT	M24308/23-35 ITT/CANNON 95F6022 NEWARK	J1	1
14	DE-9 D-SUB CONNECTOR, STRAIGHT PCB MOUNT	A2100-ND DIGI-KEY	J18	1
15	PLCC SOCKET, 28 PIN, SMD	A2141-ND DIGI-KEY	U22	1
16	PLCC SOCKET, 44 PIN, SMD	A2142-ND DIGI-KEY	U13	1

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17	OPTIONAL BDM 1x2 HEADER	ANY	J19	(1)
18	2x5 SHROUDED HEADER	92N3713 NEWARK	J20	1
19	SINGLE PIN TEST HEADER	ANY	TP1-TP28	28
20	**E1/T1 BOARD OPTIONAL SNUBBER**: CERAMIC CAPACITOR-1000PF, 50V, X7R	PCC102BVCT-ND DIGI-KEY	C243,C244,C246, C247,C249-C252	(8)
22	CERAMIC CAPACITOR 0.01UF, 16V, YV5, 0603	PCC103BVTR-ND DIGI KEY	C124, C131, C133-C140, C142, C144-C148, C153-C165, C168, C170, C171, C174, C176, C177, C179, C181, C182, C185, C194-C196, C199, C200, C202, C204-C207, C211-C213, C220-C222, C225, C226, C228, C230-C233, C237-C239	65
23	CERAMIC CAPACITOR 0.047UF, 25V, X7R, 0603	VJ0603Y473KXXMX VISHAY NEWARK	C169, C173, C180, C184, C201,C208, C227, C234	8
24	CERAMIC CAPACITOR-0.1UF, 25V, Y5V, 0603	VJ0603Y104KXXMX VISHAY NEWARK	C2, C4, C6, C8, C10, C12, C14, C16, C17-C21, C28, C50, C51, C52, C72-C119, C130, C132, C172, C183, C245, C248	71
25	CERAMIC CAPACITOR 0.47UF, 16V, X7R, 0805	EMK212BJ474KG TAYIO YUDEN	C197, C198, C209, C210, C223, C224, C235, C236	8
26	CERAMIC CAPACITOR 1UF, 16V, X7R, 1206	EMK316BJ105KF-T TAYIO YUDEN	C1, C3, C5, C7, C9, C11, C13, C15	8
27	CAPACITOR-10UF, 6.3V, TANTALUM THE, SMD	PCS1106CT-ND DIGI-KEY	C37-C41,C59, C60, C62, C63, C68, C71, C141, C143,C167,C175, C178,C186, C191-C193,C203, C214-C219,C229, C240-C242,	31
28	CAPACITOR-68UF, 6.3V, TANTALUM THE	PCT1686CT-ND DIGI-KEY	C49	1

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29	TRANSIENT VOLTAGE SUPPRESSOR, 5V	SA5.0AGICT-ND DIGI-KEY	D8	1
30	ZENER DIODE, 3.6V, 1W, SMD	1SMB5914BT3 NEWARK	D3	1
31	SCHOTTKY DIODE, 2A, 20V, SMB_2	B220DICT-ND DIGI-KEY	D4	1
32	FERRITE BEAD, 0.2A, 1206	240-1019-1-ND DIGI-KEY	L2,L3,L8	3
33	LED-RED, PCB MOUNTED	LU60361CT-ND DIGI-KEY	D10	1
34	LED-GREEN, PCB MOUNTED	LU60355CT-ND DIGI-KEY	D7, D9	2
35	OSC_TTL DIP-25.0000M HZ, 100 PPMA	CTX176-ND DIGI-KEY	Y3	1
36	OSC_TTL DIP-3.6864MH Z, 100 PPM, A	CTX154-ND DIGI-KEY	Y4	1
37	**T1 BOARD:** CRYSTAL OSC CMOS, 37.056MHZ, 50 PPM DIP8,	MB050H-37.056MHZ MMD	Y2	1
38				
39	RESET SWITCH	P8009S-ND DIGI-KEY	SW50	1
40	E1/T1 LINE INTERFACE QUAD TRANSFORMER	T1008 PULSE ENGINEERING	T1, T2, T3, T4	4
41	RESISTOR, 1 OHM, 5%, 0805	P1.0BCT-ND DIGI-KEY	R96, R102, R103, R106-R109, R115-R118, R124, R125, R128, R132, R135, R139	17
42	**T1 BOARD OPTIONAL SNUBBER:** RESISTOR, 22 OHM, 5%, 0805	P22ACT-ND DIGI-KEY	**T1 BOARD OPTIONAL SNUBBER:** R126, R129, R133, R136, R140, R142, R144, R146	(8)
43	**T1 BOARD:** RESISTOR, 0 OHM, 5%, 0805	0805, ANY BRAND	**T1 BOARD:** R5, R7, R9, R11, R19, R21, R23, R25	8
44	RESISTOR, 75 OHM, 5%, 0805	P75ACT-ND DIGI-KEY	R81,R83,R87, R88, R99-R101, R110, R119	9
45	RESISTOR ARRAY 4x68 OHM, SMD 1206	Y468CT-ND DIGI-KEY	RN3-RN11, RN33-RN35, RN39-RN41	15
46	RESISTOR ARRAY 4x4.7K OHM, SMD 1206	Y4472CT-ND DIGI-KEY	RN20, RN25-RN28, RN31, RN32	7
47	**T1 BOARD:** RESISTOR, 93.1 OHM, 1%, 0805	P93.1CCT-ND DIGI-KEY	**T1 BOARD:** R127, R131, R134, R138, R141, R143,R145, R147	8
48	RESISTOR,	P121CCT-ND DIGI-	R51	1

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	121 OHM, 1%, 0805	KEY		
49	**T1 BOARD:** RESISTOR, 309 OHM, 1%, 0805	P309CCT-ND DIGI-KEY	**T1 BOARD:** R6, R8, R10, R12, R20, R22, R24, R26,	8
50	RESISTOR, 357 OHM, 1%, 0805	P357CCT-ND DIGI-KEY	R60,R61	2
51	RESISTOR- 4.7K, 5%, 0805	P4.7KACT-ND DIGI-KEY	R1, R52, R82, R84-R86, R91, R92, R97, R104, R130, R137	12
52	RESISTOR-316K, 1%, 0805	P316KCCT-ND DIGI-KEY	R111-R114, R120-R123	8
53	PCI BUS CARD BRACKET	PER PMC-SIERRA DRAWING	PMC-BRACKET1	1
54	SCREW, 4-40 x ¼	ANY	SCREW1, SCREW2	2
55	RESISTOR, 0 OHM, 5%, 0805	0805, ANY BRAND	R79	1
Following Parts are external to the Evaluation Card				
56	DD-50 D-SUB CONNECTOR, METAL SHELL, STRAIGHT, SOLDER CUP	1492 SPC 92N3449 NEWARK	P61	(1)
57	DD-50 D-SUB METAL SHELL SET, STRAIGHT	51N1298 NEWARK	HW1	(1)
58	D-SUB CONNECTOR MOUNTING SCREW SET	ANY	HW2	(1)
59	SHIELDED TWISTED PAIR, 30CM LONG	TBD	HW3-HW18	(16)
60	ADC BANTAM CONNECTORS	PC-834-J-RED ELECTROSONIC	J51-J58	(8)
61	ADC BANTAM CONNECTORS	PC-834-J-BLUE ELECTROSONIC	J59-J66	(8)
62	HEAT SHRINK TUBING, BLUE, RED AND BLACK	ANY		
Following Parts are used for troubleshooting microprocessor circuit and are not assembled on the Evaluation Card				
63	TEST RECEPTACLE, (CONNECTOR NOT ASSEMBLED)	A3103-ND DIGI-KEY	(J23, J25)	(2)
64	TEST HEADER. CONNECTOR ATTACHED TO A TEST CABLE	A3107-ND DIGI-KEY	(J101, 102)	(2)
65	RESISTOR ARRAY 4x68 OHM, SMD 1206	Y468CT-ND DIGI-KEY	RN15, RN21, RN22, RN23, RN24, RN29,	6

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PMC 980474 Issue date January 1999