PM7366

FREEDM-8

CHANNELIZING J2 DATA STREAMS WITH THE FREEDM-8 AND S/UNI-QJET

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1 BACKGROUND

The PM7366 FREEDM-8 Frame Engine and Datalink Manager device is a monolithic integrated circuit that implements HDLC processing, and PCI Bus memory management functions for a maximum of 128 bi-directional channels.

Eight bi-directional ports are available to receive and transmit HDLC data over 128 bidirectional channels. Received data is then processed and stored into host memory via DMA transfers over the PCI bus interface. Transmit data is taken from host memory and transmitted out over the selected channels and links.

Two general modes of operation are available - channelized and unchannelized. During unchannelized mode, each unchannelized port is assigned to a single HDLC channel. During channelized mode, arbitrary timeslots can be assigned to comprise a single HDLC channel, allowing greater flexibility in bandwidth allotment. Without modification, the FREEDM-8 may be configured to transmit and receive over eight E1 or T1 data links. However, as the FREEDM-8 relies on gaps in transmit and receive clocks to recognize frame boundaries, J2 frames may also be channelized by the FREEDM-8 in E1 mode so long as presentation of the data is consistent with the expected E1 streams in the following respects:

1. Thirty-one contiguous 64 kbit/sec timeslots are sampled or output by each port within each frame.

2. Transmit and receive clocks are gapped during framing bits (no framing bits are sampled).

Frame boundaries of the incoming and outgoing data are determined by gaps in transmit and receive clocks that exceed a programmable time threshold.

The S/UNI-QJET is an ATM user network interface with four bi-directional ports that can be set to operate in J2, E3 or T3 modes. In framer only, J2 mode, the S/UNI-QJET detects J2 frame boundaries and outputs signals in sync with the data stream to indicate frame boundary positions. To interface the S/UNI-QJET with the FREEDM-8 to channelize J2 thus requires additional logic to de-multiplex J2's 98 timeslots of data per frame to four 31 timeslot E1 frames using these signals. Four E1 frames are required as this is the minimum number of E1 frames that can accommodate the data payload of one J2 frame. Any HDLC channel may then be comprised of arbitrary timeslots within one of the E1 streams arriving on a single port. This application note describes a method to perform the required de-multiplexing and multiplexing. Note that this scheme

allows channelizing of timeslots 97 and 98 of the J2 frame. However, these timeslots are regularly used for signaling and will be overwritten, in the transmit direction, by the S/UNI-QJET unless the J2SIGTHRU bit is set to '1' in the S/UNI-QJET FRMR LOF Status register. For more information see [1] PM7346 S/UNI-QJET Data Sheet, Issue 4.

1.1 REFERENCES

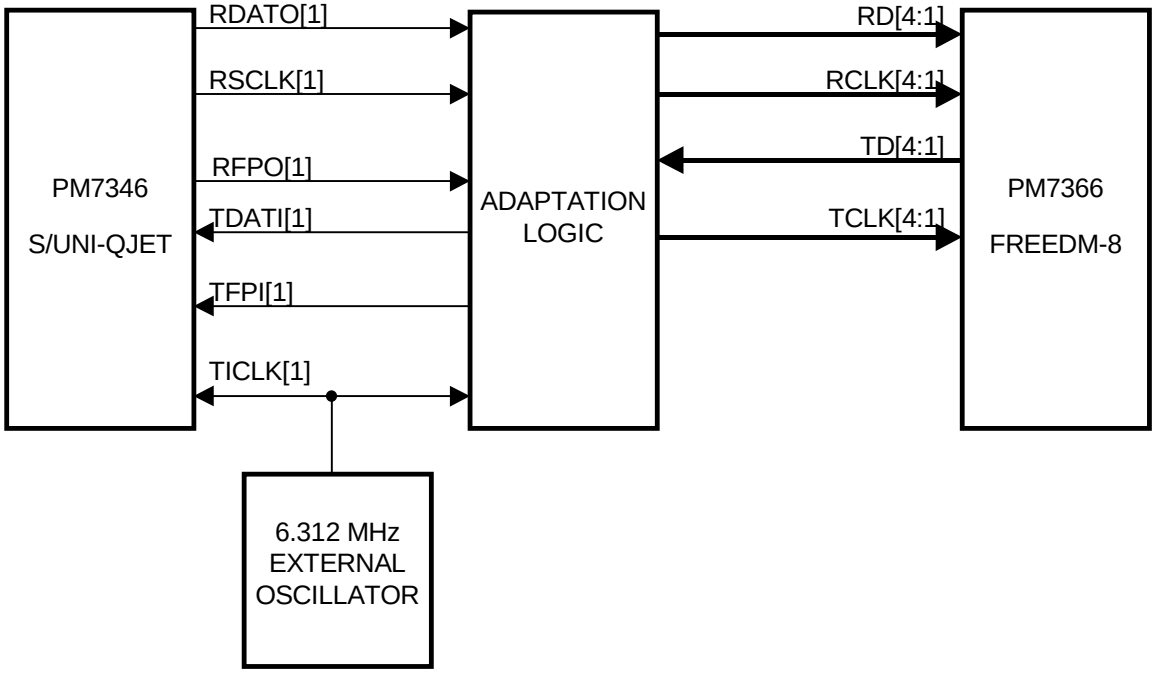
[1] PMC-960835, PMC-Sierra Inc., PM7346 S/UNI-QJET Data Sheet, Issue 4, December, 1997.

[2] PMC-970930, PMC-Sierra Inc., PM7366 FREEDM-8 Data Sheet, Issue 1, September, 1997

2 PIN CONNECTIONS

One J2 data link requires four E1 data links to accommodate its bandwidth. This means that, one bi-directional J2 port is linked through glue logic, to four of the FREEDM-8's E1 ports. Each FREEDM-8 port has four signals used in this implementation – RCLK, RD, TCLK, and TD. Each S/UNI-QJET port has six signals used in this implementation – RSCLK, RDATO, RFPO, TICLK, TFPI, and TDATI. Figure 1 below illustrates the connections between the S/UNI-QJET, glue logic, and the FREEDM-8.

Figure 1 - Pin Connections for a Single Channelized J2 Link



The receive data output from the S/UNI-QJET (RDATO[1]) is connected in common to RD of each of 4 FREEDM-8 ports. The clock signal from the external 6.312 MHz oscillator is fed to the TICLK input of the S/UNI-QJET. All other signals between the S/UNI-QJET and the FREEDM-8 are passed through the adaptation logic.

3 J2 RECEIVE CHANNELIZATION

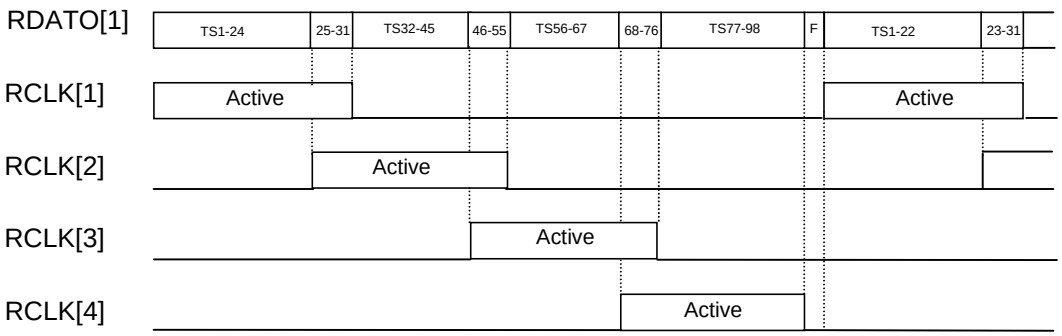
This section describes the timing and circuitry for receiving channelized J2 streams using the FREEDM-8 and S/UNI-QJET devices.

3.1 Functional Receive Timing

In the receive direction, the data from RDATO[1] of the S/UNI-QJET is connected to four of the RD[x] pins of the FREEDM-8. Data from the S/UNI-QJET port is then selectively sampled by RD[1] to RD[4]. This is done by selectively applying the receive clocks for each of RD[1] to RD[4] (assuming RD[4:1] are selected) during the desired timeslots. Each port receives this clock signal for a duration of 31 timeslots.

In the implementation presented here, port 1 samples timeslots 1 to 31, port 2 samples timeslots 23 to 53; port 3 samples timeslots 46 to 76, and port 4 samples timeslots 68 to 98 for each J2 frame. The functional timing is shown below in Figure 2.

Figure 2 - J2 Receive Timing Diagram



RDATO[1], the data from the S/UNI-QJET, is delivered to each of the four FREEDM-8 RD pins in common. RCLK[4:1] show the activity of the clock on the RCLK pins of each of the four FREEDM-8 ports.

For each port the 31 contiguous timeslots on each of these four ports compose an E1 frame for that port. The long clock inactivity between the sampling periods for each port serve to indicate frame boundaries to the FREEDM-8.

In this implementation, timeslots appearing on two ports will be ignored by the lower order port (timeslots sampled by both ports 1 and 2 will be ignored by port 2, for example). This is a feature of the J2 channelization scheme (the

FREEDM-8 should be programmed to ignore timeslots according to this scheme), and should not be confused with the port priority used by the FREEDM-8 device where timeslots from lower numbered ports are processed before those from higher numbered ports.

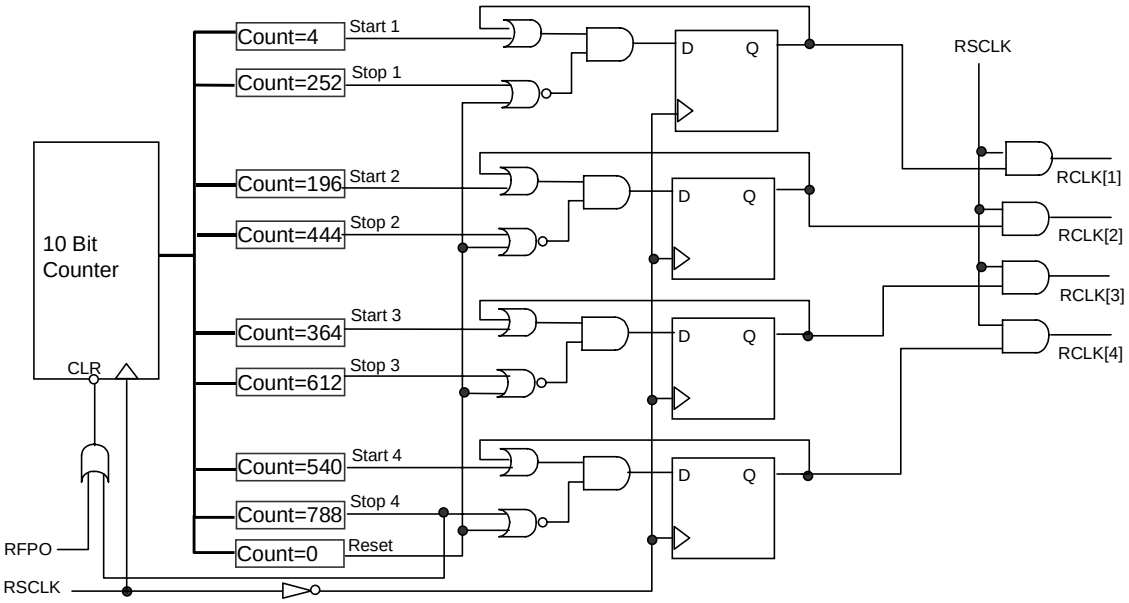
Note that although ports 1 to 4 are used in this scheme, any four of the FREEDM-8 ports may be used to substitute for any of the ports in this example. Also, the times of clock activity on the second and third ports may be adjusted to allow more flexible allotment of timeslots to channels. For example, assigning timeslots 24 and 32 to the same channel is not possible in this implementation as timeslot 24 is sampled only by port one, while timeslot 32 is sampled only by port two (see Figure 2). By changing the active time for the second port so that it is active during timeslots 24 to 54 instead of timeslots 25 to 55, timeslots 24 and 32 are both sampled by the second port and may thus be assigned to the same channel. The timeslots ignored by the FREEDM-8 should also be changed to reflect the desired channelization. For example, if overlapping timeslots between ports one and two are to be channelized with other timeslots sampled by port two, overlapping port one data should be ignored instead of overlapping port two data. The active time for a port may be changed by changing the start and stop times of the corresponding receive clock.

3.2 Receive Logic Implementation

Logic to perform the above clock allotment must be able to count the number of bits that have been sampled by the FREEDM-8 as well as change clock allotment based on the current count. An AND gate array is used to control gating of the clock to the FREEDM-8's ports. The S/UNI-QJET is programmed to output RSCLK. Allotment of the clock to a port is done by performing an AND operation between a gating signal for a particular port and the clock. The result of the operation is passed to the RCLK input of the corresponding port.

A single 10 bit counter is used to keep track of bit position within the J2 frames. D flip flops are used to control the output of each gating signal. Setting and resetting of these flip flops is done at count values that reflect the desired position in the J2 frame where each clock should start and stop. The logic is shown below in Figure 3.

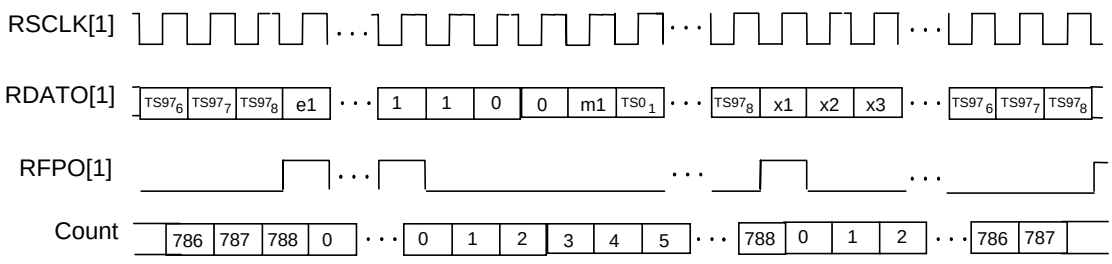
Figure 3 -J2 Receive Logic Implementation



The signals RSCLK, and RFPO are signals from the S/UNI-QJET's J2 port while the RCLK[4:1] signals are the receive clocks passed to the FREEDM-8. Reset of the counter and D flip flops occur every J2 frame boundary. The counter is synchronously reset on the first framing bit of each frame by the RFPO signal. The start and stop signals are decoded from the current count, and pulse for one clock period to set and reset the D flip flops, respectively. Feedback is used by each D flip flop to sustain gating signals until the stop signal is applied.

After reset, the counter keeps track of the frame position beginning with the first framing bit as '0'. Therefore, the clock is applied to the first port following the count of '4' (indicating the fifth framing bit) for the FREEDM-8 to sample the first data bit. Timing of the count value, RSCLK, RDATO, and RFPO is shown in figure 4 below.

Figure 4 - S/UNI-QJET Receive Timing



The clock for the first port is stopped when the counter has counted 31 timeslots of data, or 248 bits after the clock began, at count 252. Similarly, the clocks for ports two, three and four start at count 196, 364, and 540 respectively and stop at count 444, 612, and 788 respectively. The start and stop times for the clocks to ports two and three may be changed by an integer number of timeslots so long as the number of timeslots between the stop and start time of each clock is 31 and all the data bits of the J2 frame (except the framing bits) are sampled at least once.

The value of the counter represents the J2 bit position last sampled by the FREEDM-8 plus 5, and is updated on the rising edge on which the FREEDM-8 performs it's sampling. In relation to the data output by the S/UNI-QJET, the count represents the J2 bit position currently output by the S/UNI-QJET plus 5, and is updated half a clock cycle after the output from the S/UNI-QJET is updated.

FREEDM-8 samples inputs on the rising edge of RCLK. To avoid sampling of spurious signals by the FREEDM-8 when clock gating signals are applied, gating signals are generated on the falling edge of RSCLK. This prevents the generation of any rising edges on RCLK[X] when gating signals are applied as the product will always be zero when RSCLK is low.

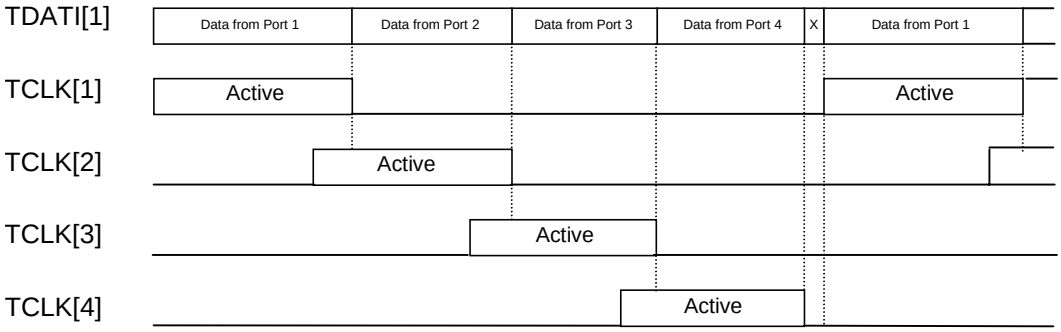
4 J2 TRANSMIT CHANNELIZATION

This section describes the timing and circuitry for transmitting channelized J2 streams using the FREEDM-8 and S/UNI-QJET devices.

4.1 Transmit Functional Timing

In the transmit direction, the data from the four FREEDM-8 transmit output ports is sampled and then multiplexed on to the first S/UNI-QJET transmit input port. Transmit clock signals must be delivered to each of the FREEDM-8's ports in exactly the same alignment to the J2 frame as in the receive direction. The source for the data that is passed to the S/UNI-QJET port is selected using the gating signals used for allotting the transmit clock. However, only one data source can be selected at any time, and in this implementation, where data is output by two ports, the higher order (lower numbered) port takes precedence. The functional transmit timing is shown below in Figure 5.

Figure 5 - J2 Transmit Timing Diagram



TDATI[1] shows the source of data passed to the S/UNI-QJET's TDATI[1] pin. TCLK[4:1] show the activity of the clock on the TCLK pins of each of the FREEDM-8 ports. X marks the framing bit times of the J2 frame.

The data source is switched after timeslots 31, 53, and 76. The first FREEDM-8 port is selected as the data source at the beginning of every J2 frame. The long clock inactivity between the active clock periods for each port serve to indicate frame boundaries to the FREEDM-8.

For timeslots that are not passed to the S/UNI-QJET (corresponding to timeslots that are ignored in the receive direction), the FREEDM-8 is programmed to output a programmable byte pattern into these timeslots.

Note that although ports 1 to 4 are used in this example, any four of the FREEDM-8 ports may be used to substitute for any of the ports in this example. Also, the times of clock activity on the second and third ports may be adjusted to allow more flexible allotment of timeslots to channels. For example, assigning timeslots 24 and 32 to the same channel is not possible in this implementation as timeslot 24 is output only by port one, while timeslot 32 is output only by port two. By changing the active time for the second port so that it is active during timeslots 24 to 54 instead of timeslots 25 to 55, timeslots 24 and 32 are both output by the second port and may thus be assigned to the same channel. The logic in the box labeled 'Data Selector' in figure 6 is used to select the data source. This logic should also be modified to reflect the desired channelization. For example, if overlapping timeslots between ports one and two are to be channelized with other timeslots sampled by port two, overlapping port two data should be passed to the S/UNI-QET instead of overlapping port one data. The active time for a port may be changed by changing the start and stop times of the corresponding transmit clock.

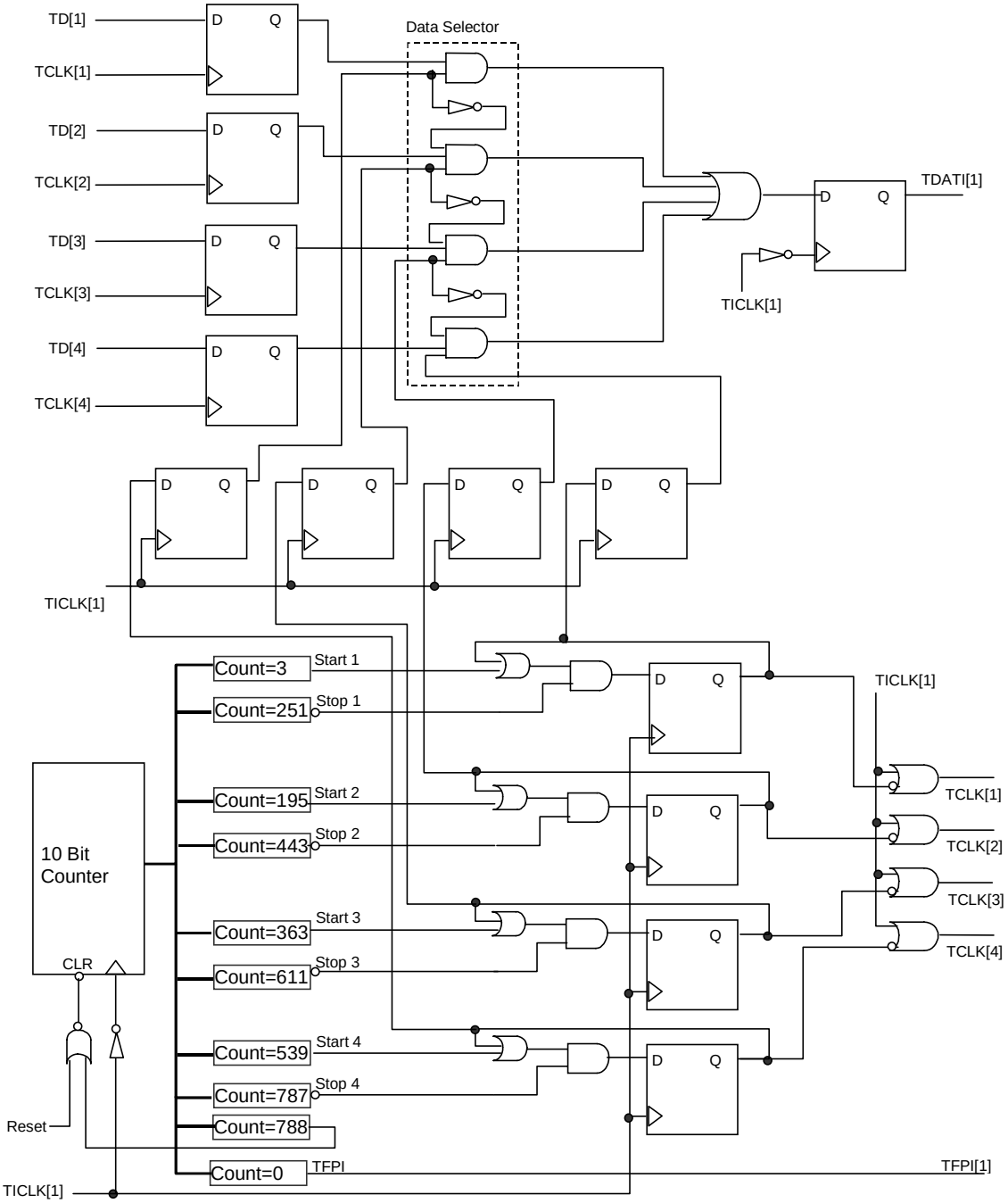
4.2 Transmit Logic Implementation

Clock allotment for the transmit direction is identical to that of the receive direction. An AND gate array is used to control gating of the clock to the FREEDM-8's ports. The S/UNI-QJET is programmed to use TFPI as a framing reference. Allotment of the clock to a port is done by performing an OR operation between an inverted gating signal for a particular port and the clock. The result of the operation is passed to the TCLK input of the corresponding port.

In addition to allotting the clock, the transmit logic must also multiplex data from the four FREEDM-8 ports to the S/UNI-QJET port. Data to be transmitted from the FREEDM-8 is sampled by input flip flops and then multiplexed to a single output flip flop by logic using the clock gating signals to select the source. The multiplexed stream is clocked by another flip flop before output to help ensure synchronization with the clock. This operation results in a propagation delay of one clock cycle for the data.

A single 10 bit counter is used to keep track of bit position within the J2 frames. D flip flops are used to control the output of each gating signal. Setting and resetting of these flip flops is done at count values that reflect the desired position in the J2 frame where each clock should start and stop. A separate reset input may be used to put the counter into a known state on start up. The logic is shown below in Figure 6.

Figure 6 -J2 Transmit Logic Implementation



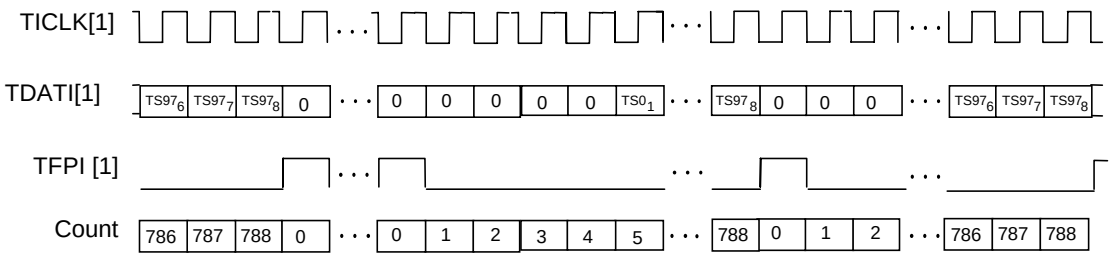
The signals TICLK[1], and TFPI[1] are signals sent to the S/UNI-QJET J2 port while the TCLK[4:1] and TD[4:1] are signals for the FREEDM-8's four ports. Reset of the counter and D flip flops occurs every J2 frame boundary. The

counter synchronously resets itself every 789 bits. The start and stop signals are decoded from the current count and pulse for one clock period to set and reset the D flip flops, respectively. The values at which the stop and start signals are applied is one less than those of the corresponding receive count. This causes the FREEDM-8 to output data one clock cycle early (relative to the TFPI pulse), compensating for the one clock cycle delay of the transmit data passing through the multiplexing logic. Feedback is used by each D flip flop to sustain gating signals until the stop signal is applied.

The four AND gates in the box labeled “Data Selector” are used with delayed clock gating signals to select the current data source. The delay of the clock gating signals is required to synchronize the source selection with the data, as the incoming data is delayed by input flip flops. Inverters are used to keep only a single data source gated when two TCLK signals are active. The inverters inhibit the gating of data from lower order ports (higher numbered ports) when a port of the next higher order (one number lower) is active.

After reset, the counter keeps track of the frame position beginning with the first framing bit as ‘0’. Therefore, the clock is applied to the first port following the count of ‘3’ (indicating the fourth framing bit) for the FREEDM-8 to output the first data bit one cycle early. During framing bit times, the TDATI[1] pin is at logic ‘0’. Timing of the count value, TICLK, TDATI, and TFPI is shown in figure 7 below.

Figure 7 - S/UNI-QJET Transmit Timing



The clock for the first port is stopped when the counter has counted 31 timeslots of data, or 248 bits after the first flip flop was set, at count 251. Similarly, the clocks for ports two, three and four start at count 195, 363, and 539 respectively; and stop at count 443, 611, and 787 respectively. The start and stop times for the clocks to ports two and three may be changed by an integer number of timeslots so long as the number of timeslots between the stop and start time of each clock is 31 and all the data bits of the J2 frame (except the framing bits) are sampled at least once. Multiplexing of the input data must also be altered to reflect this change.

The value of the counter represents the J2 bit position currently available at the output of the FREEDM-8 plus 4, and is updated at the same time as the FREEDM-8's output. In relation to the data sampled by the S/UNI-QJET, the count represents the J2 bit position currently available at the input of the S/UNI-QJET plus 5, and is updated at the same time as the data present at the input of the S/UNI-QJET.

FREEDM-8 updates outputs on the falling edge of TICLK. To avoid output of spurious signals by the FREEDM-8 when clock gating signals are applied, gating signals are generated on the rising edge of TICLK. This prevents the generation of any falling edges on TCLK[X] when gating signals are applied as the sum will always be high when TICLK is high.

5 DISCLAIMER

The logic and methodology presented in this document are correct to the best of our knowledge, but is preliminary. To date, this logic has not been simulated or verified in the lab. Therefore, there is no guarantee that the presented logic will work as specified.

NOTES

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