SATURN Quad User Network Interface for J2/E3/T3

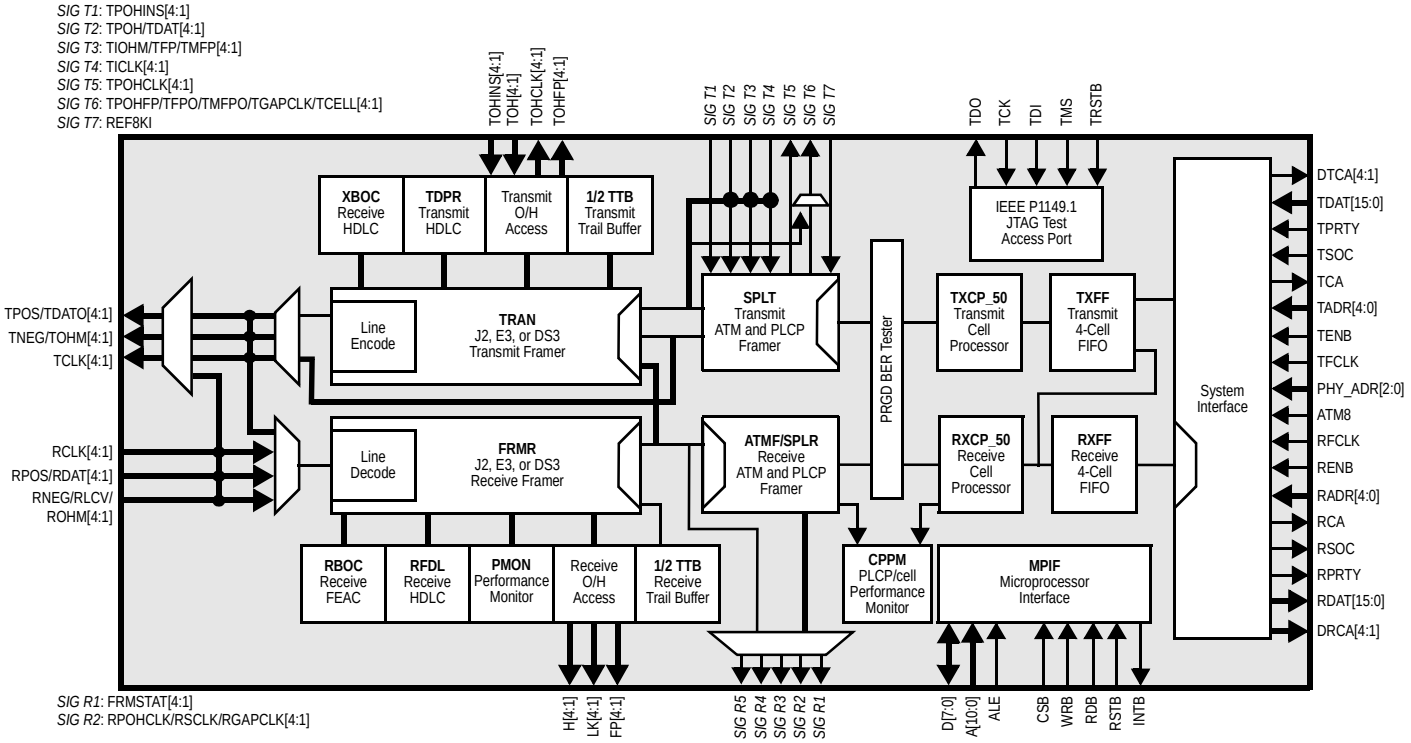
FEATURES

- Single-chip quad ATM User Network Interface (UNI) operating at 44.736 Mbit/s, 34.368 Mbit/s, and 6.312 Mbit/s conforming to ATMF-95-1207R1, ATMF-94-0406R5, and AF-PHY-0029.000. Each line can be individually configured for the desired rate.
- Each quadrant provides on-chip DS3, E3 (G.751 and G.832), and J2 framers and can be configured to be used solely as a framer. When configured in framer mode, gapped transmit and receive clocks can be generated for interfaces that need access to only payload data bits.
- Supports bypass of the internal framers and supports connections to an arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s, which enables the S/UNI-QJET to be used as a quad ATM cell delineator.
- Implements ATM direct-cell mapping into T1, DS3, E1, E3, and J2 transmission systems according to ITU-T Recommendation G.804.
- Provides a SCI-PHY™ and 50 MHz UTOPIA Level 2 compliant 8- or 16-bit ATM-PHY Interface.
- Implements the Physical Layer Convergence Protocol (PLCP) for T1 and DS3 transmission systems according to the ATM Forum UNI Specification and ANSI TA-TSY-000773, TA-TSY-000772, and E1 and E3 transmission systems according to the ETSI 300-269 and ETSI 300-270.
- Implements the ATM physical layer for Broadband ISDN according to ITU-T Recommendation I.432.
- Uses the PM4341 T1XC, PM6341 E1XC, PM4351 COMET, PM4344 TQUAD, PM6344 EQUAD, and PM4314 QDSX T1 and E1 framer/line interface chips for T1 and E1 applications.
- Provides programmable pseudo-random test pattern generation, detection, and analysis features.
- Provides integral transmit and receive HDLC controllers with 128-byte FIFO depths.
- Provides performance monitoring counters suitable for accumulation periods of up to 1 second.
- Provides an 8-bit microprocessor interface for configuration, control and status monitoring.
- Provides a standard 5-signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power 3.3 V CMOS technology with 5 V-tolerant inputs.
- Available in a high density 256-pin SBGA package (27 mm by 27 mm).
- Rated for industrial temperature operation.

APPLICATIONS

- ATM or Frame Relay Switches, Multiplexers, and Routers
- SONET/SDH Mux DS3/E3 Tributary Interfaces
- PDH Mux DS3/E3/J2 Line interfaces
- DS3/E3/J2 Digital Cross-Connect Interfaces
- DS3/E3/J2 PPP Internet Access Interfaces
- DS3/E3/J2 Frame Relay Interfaces

BLOCK DIAGRAM



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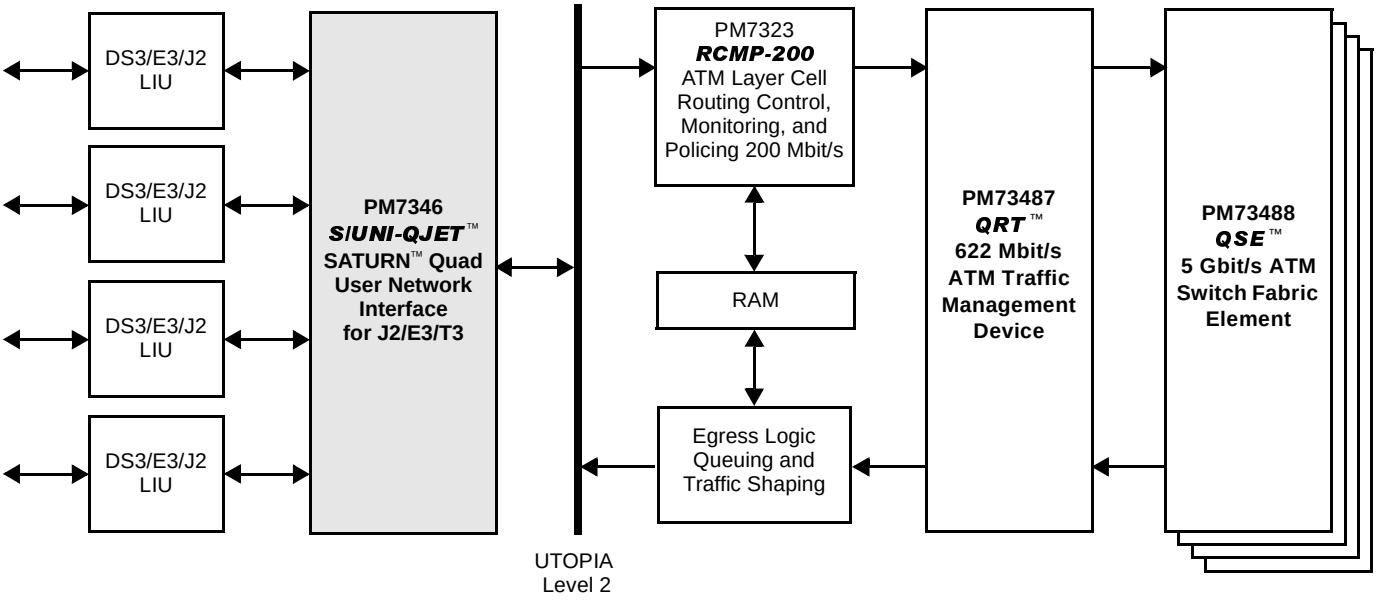
TYPICAL APPLICATIONS

QUAD DS3/E3/J2 ATM PORT CARD



STS-3 CARRYING THREE UNCHANNELIZED DS3s PROVIDING PPP OR FRAME RELAY SERVICE

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To order documentation, send email to: document@pmc-sierra.com or contact the head office, Attn: Document Coordinator

All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

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