PM7346

S/UNI-QJET

Comparison of PLPP, S/UNI-PDH, and S/UNI-QJET register space

Issue 1: November, 1996

CONTENTS

LIST OF TABLES

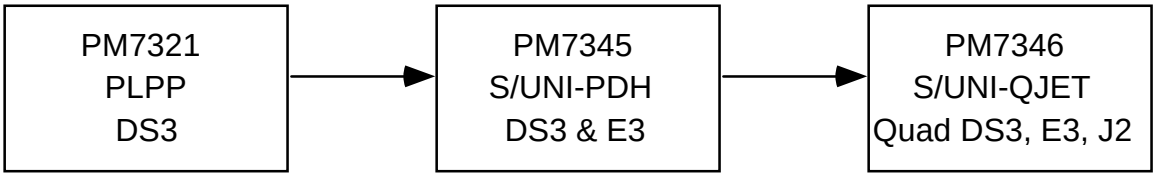
REFERENCES

- PMC-Sierra, Inc, "PM7321 PLPP T3 Framer / Transceiver", Data Book, Issue 7, PMC-910812, December 1995
- PMC-Sierra, Inc, "PM7321 PLPP T3 Framer / Transceiver", Data Book Errata.
- PMC-Sierra, Inc, "PM7345 S/UNI-PDH Saturn User Network Interface for Plesiochronous Digital Hierarchy", Data Book, Issue 5, PMC-931011, April 1995
- PMC-Sierra, Inc, "PM7345 S/UNI-PDH Saturn User Network Interface for Plesiochronous Digital Hierarchy", Data Book Errata.
- PMC-Sierra, Inc, "PM7346 S/UNI-QJET Saturn Quad User Network Interface for J2/E3/T3", Data Book, Issue 1, PMC-960835, August 1996

OVERVIEW

This document provides information to help migrate designs using the PM7321 PLPP or PM7345 S/UNI-PDH devices to a design using the PM7346 S/UNI-QJET. The document explains the differences and similarities between the register spaces of the devices' functional blocks. Specific references are made to register names, bit names and their locations in each of the three devices. A diagram illustrating the transition between devices is provided below.

Figure 1. History of PMC-Sierra ATM PHY devices for DS3, E3, and J2



The PM7321 PLPP is an ATM physical layer processor with integrated DS3 framing. PLCP sublayer DS1, DS3, E1, and E3 processing is supported as is ATM cell delineation.

The PM7345 S/UNI-PDH is an ATM physical layer processor with integrated DS3 and E3 framing, with support for PLCP sublayer DS1, DS3, E1, and E3 processing and ATM cell delineation.

The PM7346 S/UNI-QJET is a four channel ATM physical layer processor with integrated DS3, E3, and J2 framing, with support for PLCP sublayer DS1, DS3, E1, and E3 processing and ATM cell delineation.

This document is not intended as a replacement for reading the associated data books. It is intended only to assist developers who are already familiar with the PLPP or S/UNI-PDH. Since the S/UNI-QJET data book is preliminary, information regarding that device is subject to change. In the event of conflict between this document and the current issue of the data book, the data book shall be considered correct.

REGISTER COMPARISON BY FUNCTIONAL BLOCK

A block by block comparison of the register space in the PLPP, S/UNI-PDH, and S/UNI-QJET is presented below. Because the S/UNI-QJET is a four channel device, each register address represents four registers in the format xYY, where x is an integer from 0 to 3. For example, the DS3 FRMR Configuration register is located at address x30H in the S/UNI-QJET. For each of the four quadrants, x30H represents 030H, 130H, 230H, and 330H. Where possible, register addresses are given in a base - offset notation to illustrate the similarities between the three devices.

FRMR Block

The PLPP has only a DS3 FRMR block. Because the S/UNI-PDH frames both E3 and DS3 signals, the device has two FRMR blocks. Similarly, the S/UNI-QJET frames to J2, E3, and DS3 signals, hence the device has three FRMR blocks.

DS3 FRMR Block

This section compares the DS3 FRMR blocks of the PLPP, S/UNI-PDH, and S/UNI-QJET.

Table 1. DS3 FRMR Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base Address (Hex)	08	08	x30
Configuration	00	00	00
Interrupt Enable	01	01	01
Additional Config	N/A	01*	01*
Interrupt Status	02	02	02
Status	02	02	02

* The Additional Configuration registers in the S/UNI-PDH and S/UNI-QJET reside in the same location as the Interrupt Enable registers. They provide additional configuration for the DS3 FRMR block. Access to this register is selected by the ACE bit (bit 7) in the DS3 FRMR Status register in the S/UNI-PDH or in the S/UNI-QJET.

PLPP DS3 FRMR BLOCK

All bits available in the DS3 FRMR block of the PLPP are available in both the S/UNI-PDH and S/UNI-QJET.

S/UNI-PDH DS3 FRMR BLOCK

Additional bits MBDIS, FDET, & AISPAT in the configuration register and REDE, REDI, & REDV in the interrupt enable, interrupt status, and status register are provided that are not available in the PLPP. These bits are also available in the S/UNI-QJET.

S/UNI-QJET DS3 FRMR BLOCK

Additional bits MBDIS, FDET, & AISPAT in the configuration register and REDE, REDI, & REDV in the interrupt enable, interrupt status, and status register are provided that are not available in the PLPP. These bits are also available in the S/UNI-PDH.

E3 FRMR Block

This section compares the E3 FRMR blocks of the S/UNI-PDH and S/UNI-QJET. The PLPP does not have an E3 FRMR block.

Table 2. E3 FRMR Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base Address (Hex)	Not Applicable	60	x38
Framing options	Not Applicable	00	00
Maintenance options	Not Applicable	01	01
Interrupt enable	Not Applicable	02	02
Interrupt indication & status	Not Applicable	03	03
Maintenance int. enable	Not Applicable	04	04
Maintenance int. indication	Not Applicable	05	05
Maintenance status	Not Applicable	06	06

S/UNI-PDH E3 FRMR BLOCK

All the bit positions and functionality of the S/UNI-PDH are available in the S/UNI-QJET.

S/UNI-QJET E3 FRMR BLOCK

The S/UNI-QJET E3 FRMR block is functionally equivalent to the S/UNI-PDH E3 FRMR block. The E3 FRMR was revised for the S/UNI-QJET;- it frames within 250µs in E3 G.832 format, in compliance with ITU-T G.783 and ATM Forum's E3 requirements.

J2 FRMR Block

Since the J2 FRMR is unique to the S/UNI-QJET, its register space will not be discussed here.

TRAN Block

The PLPP has only a DS3 TRAN block. Similarly, the TRAN block of the S/UNI-PDH consists of two TRAN blocks (for DS3 and E3). As with the FRMR block, the TRAN block of the S/UNI-QJET consists of three TRAN blocks (for DS3, E3, and J2).

DS3 TRAN Block

This section compares the DS3 TRAN blocks of the PLPP, S/UNI-PDH, and S/UNI-QJET.

Table 3. DS3 TRAN Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base Address (Hex)	20	20	x34
Configuration	00	00	00
Diagnostic	01	01	01

PLPP DS3 TRAN BLOCK

All bits available in the DS3 TRAN block of the PLPP are available in both the S/UNI-PDH and S/UNI-QJET.

S/UNI-PDH DS3 TRAN BLOCK

The DS3 TRAN block of the S/UNI-PDH is identical to the DS3 TRAN blocks of the PLPP and S/UNI-QJET.

S/UNI-QJET DS3 TRAN BLOCK

The DS3 TRAN block of the S/UNI-QJET is identical to the DS3 TRAN blocks of the PLPP and S/UNI-PDH.

E3 TRAN Block

This section compares the E3 TRAN blocks of the S/UNI-PDH and S/UNI-QJET. The PLPP does not have an E3 TRAN block.

Table 4. E3 TRAN Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base Address (Hex)	Not Applicable	68	x40
Framing options	Not Applicable	00	00
Status and diagnostics	Not Applicable	01	01
BIP-8 Error mask	Not Applicable	02	02
Maintenance	Not Applicable	03	03

S/UNI-PDH E3 TRAN BLOCK

The E3 TRAN block of the S/UNI-PDH is identical to the TRAN block of the S/UNI-QJET.

S/UNI-QJET E3 TRAN BLOCK

The E3 TRAN block of the S/UNI-QJET is identical to the TRAN block of the S/UNI-PDH.

PMON Block

This section compares the PMON blocks of the PLPP, S/UNI-PDH, and S/UNI-QJET.

Table 5. PMON Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base Address	10	10	x10
Change of meters	00	00	00
Interrupt Enable	01	01	01
Reserved	02	02	02
Reserved	03	03	03
LCV Count LSB	04	04	04
LCV Count MSB	05	05	05
FERR Count LSB	06	06	06

FERR Count MSB	07	07	07

Table 5. PMON Block - continued

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
LCVS/EXZS/IEC Count LSB	08	08	08
LCVS/EXZS/IEC Count MSB	09	09	09
Base Address	10	10	x10
PERR Count LSB	0A	0A	0A
PERR Count MSB	0B	0B	0B
CPERR Count LSB	0C	0C	0C
CPERR Count MSB	0D	0D	0D
FEBE Count LSB	0E	0E	0E
FEBE Count MSB	0F	0F	0F

PLPP PMON BLOCK

The LCVS count registers are a count of the number of DS3 information blocks (i.e. 85 bits) with line code violations. The functionality of this counter is slightly different in the S/UNI-PDH and S/UNI-QJET PMON blocks. All other registers in the PMON block are identical to the PMON registers in the S/UNI-PDH and S/UNI-QJET.

S/UNI-PDH PMON BLOCK

The PMON block of the S/UNI-PDH is identical to the PMON block of the S/UNI-QJET. The EXZS count registers are a count of the number of blocks with excessive zeros. The functionality of this counter is slightly different from the PLPP. Exactly what these registers count as excessive zeros is determined by the DALGO, SALGO, EXZDET, EXZSO, and BPVO bits in the DS3 FRMR Additional Configuration register (register 09H when ACE=1). In E3 G.832 tandem connection mode, this register represents the incoming error counts (IEC). However, it is not expected that tandem connection is used in most S/UNI-PDH applications (see register 68H). Please refer to the S/UNI-PDH documentation for correct use of the PMON block.

S/UNI-QJET PMON BLOCK

The PMON block of the S/UNI-QJET is identical to the PMON block of the S/UNI-PDH. The EXZS count registers are a count of the number of blocks with excessive zeros. The functionality of this counter is slightly different from the PLPP. Exactly what these registers count as excessive zeros is determined by the DALGO, SALGO, EXZDET, EXZSO, and BPVO bits in the DS3 FRMR Additional Configuration register (register x09H when ACE=1). In E3 G.832 tandem connection mode, this register represents the incoming error counts (IEC). However, it is not expected that tandem connection is used in most S/UNI-QJET applications (see register 40H). It should be noted that the QJET PMON counts will not increment when the selected FRMR is out of frame (OOF). Please refer to the S/UNI-QJET documentation for correct use of the PMON block.

RBOC Block

This section compares the PMON blocks of the PLPP, S/UNI-PDH, and S/UNI-QJET.

Table 6. RBOC Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base address (Hex)	06	06	x98
Configuration / IE	00	00	00
Interrupt status	01	01	01

PLPP RBOC BLOCK

All the functionality of this block is available in the S/UNI-PDH and S/UNI-QJET RBOC blocks.

S/UNI-PDH RBOC BLOCK

This block is functionally equivalent to the RBOC blocks in the PLPP and S/UNI-QJET.

S/UNI-QJET RBOC BLOCK

This block is functionally equivalent to the RBOC blocks in the PLPP and S/UNI-PDH.

XBOC Block

This section compares the PMON blocks of the PLPP, S/UNI-PDH, and S/UNI-QJET.

Table 7. XBOC Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base address (Hex)	27	27	x9A
XBOC Code	00	00	00

PLPP XBOC BLOCK

All the functionality of this block is available in the S/UNI-PDH and S/UNI-QJET XBOC blocks.

S/UNI-PDH XBOC BLOCK

This block is functionally equivalent to the XBOC blocks of the PLPP and S/UNI-QJET. Care should be taken not to confuse FEAC[0:5] for the RBOC with FEAC[0:5] for the XBOC.

S/UNI-QJET XBOC BLOCK

This block is functionally equivalent to the XBOC blocks of the PLPP and S/UNI-PDH. Care should be taken not to confuse FEAC[0:5] for the RBOC with FEAC[0:5] for the XBOC.

RFDL/RDLC Block

This section compares the RFDL blocks of the PLPP, S/UNI-PDH, and RDLC block of the S/UNI-QJET.

Table 8. RFDL/RDLC Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base address (Hex)	0C	0C	x50
Configuration	00	00	00
Enable / status	01	01	01
Status	02	02	02
Data	03	03	03

The PLPP and S/UNI-PDH both use the same RFDL block. In the S/UNI-QJET, however, the RFDL block is replaced with a new block called the RDLC. The functional descriptions for the RFDL blocks of PLPP and S/UNI-PDH, and the RDLC block of the S/UNI-QJET are given below.

PLPP RFDL BLOCK

The Facility Data Link Receiver (RFDL) Block is a microprocessor peripheral used to receive LAPD/HDLC frames on the C-bit parity Path Maintenance Data Link.

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 4-byte FIFO buffer. The RFDL Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the RFDL Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three (programmable count) bytes are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

S/UNI-PDH RFDL BLOCK

The Facility Data Link Receiver (RFDL) Block is a microprocessor peripheral used to receive LAPD/HDLC frames on the DS3 C-bit parity Path Maintenance Data Link, on the

E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the S/UNI-PDH Data Link and FERF Control register), or on the G.751 Network Use bit.

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 4-byte FIFO buffer. The RFDL Status register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the RFDL Status register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three (programmable count) bytes are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

S/UNI-QJET RDLC BLOCK

The RDLC is a microprocessor peripheral used to receive LAPD/HDLC frames on any serial HDLC bit stream that provides data and clock information such as the DS3 C-bit parity Path Maintenance Data Link, the E3 G.832 Network Requirement byte or the General Purpose data link (selectable using the RNETOP bit in the S/UNI-QJET Data Link and FERF/RAI Control register), the E3 G.751 Network Use bit, or the J2 m-bit Data Link.

The RDLC detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives packet data, and calculates the CRC-CCITT frame check sequence (FCS).

In the address matching mode, only those packets whose first data byte matches one of two programmable bytes or the universal address (all ones) are stored in the FIFO. The two least significant bits of the address comparison can be masked for LAPD SAPI matching.

Received data is placed into a 128-level FIFO buffer. An interrupt is generated when a programmable number of bytes are stored in the FIFO buffer. Other sources of interrupt are detection of the terminating flag sequence, abort sequence, or FIFO buffer overrun.

The Status register contains bits which indicate the overrun or empty FIFO status, the interrupt status, and the occurrence of first flag or end of message bytes written into the FIFO. The Status register also indicates the abort, flag, and end of message status of the data just read from the FIFO. On end of message, the Status register indicates the FCS status and if the packet contained a non-integer number of bytes.

Although the S/UNI-QJET registers in Table 8 above are similar to the PLPP and S/UNI-PDH registers of the same name, the documentation on the S/UNI-QJET RDLC block should be read to ensure correct usage.

XFDL/TDPR Block

This section compares the XFDL blocks of the PLPP, S/UNI-PDH, and TDPR block of the S/UNI-QJET.

Table 9. XFDL/TDPR Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base address Hex)	24	24	x58
Configuration	00	00	00
Interrupt status	01	01	04
Transmit Data	02	02	05

The PLPP and S/UNI-PDH both use the same XFDL block. In the S/UNI-QJET, however, the XFDL block is replaced with a new block called the TDPR. The functional descriptions for the RFDL blocks of PLPP and S/UNI-PDH, and the RDLC block of the S/UNI-QJET are given below.

PLPP XFDL BLOCK

The Facility Data Link Transmitter (XFDL) provides a serial data link for the C-bit parity path maintenance data link. The XFDL is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) is appended, followed by flags. If the XFDL Transmit Data register underflows, an abort sequence is automatically transmitted.

When enabled, the XFDL continuously transmits flags (01111110). Data bytes to be transmitted are written into the XFDL Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the microprocessor to write the next byte. After the last data frame byte, the FCS (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag sequences.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the XFDL Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR signal.

When the XFDL is disabled, a logical 1 is inserted in the path maintenance data link.

S/UNI-PDH XFDL BLOCK

The Facility Data Link Transmitter (XFDL) provides a serial data link for the C-bit parity path maintenance data link in DS3, the serial Network Operator byte or the General Purpose datalink in G.832 E3, or the National Use bit datalink in G.751 E3. The XFDL is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) is appended, followed by flags. If the XFDL Transmit Data register underflows, an abort sequence is automatically transmitted.

When enabled, the XFDL continuously transmits flags (01111110). Data bytes to be transmitted are written into the XFDL Transmit Data register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the microprocessor to write the next byte. After the last data frame byte, the FCS (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag sequences.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the XFDL Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDR signal.

When the XFDL is disabled, a logical 1 is inserted in the path maintenance data link.

S/UNI-QJET TDPR BLOCK

The Facility Data Link Transmitter (TDPR) provides a serial data link for the C-bit parity path maintenance data link in DS3, the serial Network Operator byte or the General Purpose datalink in G.832 E3, the National Use bit datalink in G.751 E3, or the m-bit datalink in J2. The TDPR is used under microprocessor control to transmit HDLC data frames. It performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, and abort sequence insertion. Upon completion of the message, a CRC-CCITT frame check sequence (FCS) is appended, followed by flags. If the TDPR transmit data FIFO underflows, an abort sequence is automatically transmitted.

When enabled, the TDPR continuously transmits flags (01111110). Data bytes to be transmitted are written into the TDPR Transmit Data register. A 128-byte FIFO is available to store data for transmission. The TDPR automatically transmits complete packets in its FIFO or when its FIFO has surpassed an upper threshold. Transmission will stop once the FIFO depth has fallen below the upper threshold and the last complete packet has been transmitted. After the last data byte of the packet, the FCS (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The TDPR then returns to the transmission of flag sequences.

Interrupts can be generated if the FIFO underflows while transmitting a packet, when the FIFO level has fallen below a lower threshold, when the FIFO is full, or if the FIFO is overrun.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort sequences.

Abort characters can be continuously transmitted at any time by setting a control bit. During packet transmission, an underrun situation can occur if data is not written to the TDPR Transmit Data register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the UDRI register bit.

When the TDPR is disabled, a logical 1 (Idle) is inserted in the path maintenance data link.

Refer to the S/UNI-QJET data book for correct usage of the TDPR functional block.

SPLR / SPLT Blocks

This section compares the SPLR and SPLT blocks of the PLPP, S/UNI-PDH and S/UNI-QJET.

Table 10. SPLR / SPLT Blocks

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base address (Hex)	28	28	x08
SPLR Configuration	00	00	00
SPLR Interrupt enbl	01	01	01
SPLR Interrupt stat	02	02	02
SPLR status	03	03	03
SPLT Configuration	04	04	04
SPLT Control	05	05	05
SPLT Diagnostics	06	06	06
SPLT F1 octet	07	07	07

PLPP SPLR / SPLT BLOCKS

These blocks are functionally equivalent to the SPLR / SPLT blocks of the S/UNI-PDH and S/UNI-QJET. Bit 0 of the SPLT Configuration register is the EXT bit. The functionality for this bit is provided in a different manner in the S/UNI-QJET.

S/UNI-PDH SPLR / SPLT BLOCKS

This block is functionally equivalent to the SPLR / SPLT blocks of the PLPP and S/UNI-QJET. Bit 0 of the SPLT Configuration register is the EXT bit. The functionality for this bit is provided in a different manner in the S/UNI-QJET.

S/UNI-QJET SPLR / SPLT BLOCKS

This block is functionally equivalent to the SPLR / SPLT blocks of the S/UNI-PDH and PLPP, with the exception of bit 0 in the SPLT Configuration register. In the S/UNI-QJET, this register is reserved and must be programmed to logic 0 for proper operation. Equivalent functionality for this bit is provided by setting TRFM[1:0] in the Transmit Configuration register to a binary value of 11. Cell octet byte alignment can be enabled or disabled by using the TOCTA bit (bit 5 of register x00H).

CPPM Block

This section compares the CPPM blocks of the S/UNI-PDH and S/UNI-QJET. Because some registers that were part of the CPPM block on the PLPP and S/UNI-PDH are part of different blocks of the S/UNI-QJET, register addresses in Table 11 are not given in the Base - offset notation of previous tables.

Table 11. CPPM Block

Register Function	PLPP Register Address (Hex)	S/UNI-PDH Register Address (Hex)	S/UNI-QJET Register Address (Hex)
Loss of Clock	30	30	x07
Change of meter	31	31	x21
B1 error count LSB	32	32	x22
B1 error count MSB	33	33	x23
FER count LSB	34	34	x24
FER count MSB	35	35	x25
FEBE count LSB	36	36	x26
FEBE count MSB	37	37	x27
HCSE count MSB	38	38	x69
HCSE count LSB	39	39	x6A
Idle cell count MSB	3A	3A	x6E
Idle cell count	-	-	x6F
Idle cell count LSB	3B	3B	x70
Receive cell count LSB	3C	3C	x6B
Receive cell count	-	-	x6C
Receive cell count MSB	3D	3D	x6D
Transmit cell count LSB	3E	3E	x86
Transmit cell count	-	-	x87
Transmit cell count MSB	3F	3F	x88

PLPP CPPM BLOCK

Register 30H in the PLPP is used to monitor all clock signals within the CPPM.

HCS error counts for the PLPP are a total of all header header check sequence error counts. The counts are stored in registers 38H and 39H. Note that there is an errata for the PLPP regarding this counter.

The PLPP uses two registers for each of the Idle cell, received cell, and transmitted cell counts. The size of these registers is expanded by one register in the S/UNI-QJET.

There is no indication of changes to the transmit, receive, idle, or HCS counts in register 31H of the PLPP.

S/UNI-PDH CPPM BLOCK

Register 30H in the S/UNI-PDH is used to monitor all clock signals within the CPPM.

HCS error counts for the S/UNI-PDH are either *uncorrectable* or *correctable*, depending on the HCSCNTSEL bit of register 5H. The counts are stored in registers 38H and 39H. Note that there is an errata for the S/UNI-PDH regarding this counter.

The S/UNI-PDH uses two registers for each of the Idle cell, received cell, and transmitted cell counts. The size of these registers is expanded by one register in the S/UNI-QJET.

There is no indication of changes to the transmit, receive, idle, or HCS counts in register 31H of the S/UNI-PDH.

S/UNI-QJET CPPM BLOCK

Register x07H in the S/UNI-QJET is the clock activity monitor, and can be used to monitor all clock signals within the S/UNI-QJET, not just the CPPM.

HCS error counts in the S/UNI-QJET are recorded in registers x69H and x6AH. Register x69H holds the number of *corrected* HCS error events, and register x6AH holds the number of *uncorrected* HCS error events. These registers are part of the RXCP_50 block in the S/UNI-QJET.

The registers for idle cell, received cell, and transmitted cell counts are expanded to use 3 registers in the S/UNI-QJET. The idle and received cell counts are part of the RXCP_50 block, and the transmitted cell counts are part of the TXCP_50 block.

RXCP Block

This section compares the RXCP blocks of the PLPP, S/UNI-PDH and S/UNI-QJET. Because the base - offset notation is not appropriate for this table, register addresses are provided in a register - bit notation instead.

Table 12a. RXCP Block Bits

Bit Name	PLPP Register - Bit	S/UNI-PDH Register - Bit	S/UNI-QJET Register - Bit
FIFORST	40 - 0	40 - 0	x62 - 0
OOCDV	40 - 1	40 - 1	x64 - 7
DSCR	40 - 2	40 - 2	x60 - 6, x60 - 7
BLOCK	40 - 3	40 - 3	x61-5, x61-7
HCK	40 - 4	40 - 4	Not Available
HCSADD	40 - 5	40 - 5	x60 - 2
HCSDQDB	40 - 6	40 - 6	x60 - 1
HCSPASS	40 - 7	40 - 7	x61 - 6
DELIN	41 - 0	41 - 0	x61 - 2, 61 - 3
DETHYST[0:1]	41 - 1:2	41 - 1:2	x61 - 0:1
FIXPAT	Always AA/55H	41 - 3	Not Available
LCD	Perform Manually	41 - 4	x64 - 6
LCDI	Perform Manually	41 - 5	x64 - 0
LCDE	Perform Manually	41 - 6	x63 - 0
REMPTY4	Not available	41 - 7	x62 - 4
FUDRI	42 - 0	42 - 0	Not available
FOVRI	42 - 1	42 - 1	x64 - 1
COCAI	42 - 2	42 - 2	Not available
UHCSI	42 - 3	42 - 3	x64 - 2
OOCDI	42 - 4	42 - 4	x64 - 4
FIFOE	42 - 5	42 - 5	x63 - 1
HCSE	42 - 6	42 - 6	x63 - 2
OOCDE	42 - 7	42 - 7	x63 - 3
HECEN	Not available	53 - 0	x60 - 0
CHCSI	Not available	53 - 1	x64 - 3

Table 12b. RXCP Block Octet Registers

Register Function	PLPP Register Location (Hex)	S/UNI-PDH Register Location (Hex)	S/UNI-QJET Register Location (Hex)
Idle cell pattern H1	43	43	x67
Idle cell pattern H2	44	44	Not Available
Idle cell pattern H3	45	45	Not Available
Idle cell pattern H4	46	46	x67
Idle cell mask H1	47	47	x68
Idle cell mask H2	48	48	Not Available
Idle cell mask H3	49	49	Not Available
Idle cell mask H4	4A	4A	x68
User pattern H1	4B	4B	Not Available
User pattern H2	4C	4C	Not Available
User pattern H3	4D	4D	Not Available
User pattern H4	4E	4E	Not Available
User mask H1	4F	4F	Not Available
User mask H2	50	50	Not Available
User mask H3	51	51	Not Available
User mask H4	52	52	Not Available
LCD count threshold	Not Available	54	x65, x66

The RXCP block in the S/UNI-QJET is replaced by a new block called RXCP_50. The functional descriptions for RXCP and RXCP_50 blocks are given below, describing the differences between the RXCP block of the S/UNI-PDH and the RXCP_50 block of the S/UNI-QJET. Because there is not a one-to-one correspondence between registers in the RXCP and RXCP_50 blocks, Table 12 lists specific bit names instead. Some of the bits that were available in the RXCP block are not available in the RXCP_50 block. Some of the functional bits in the RXCP are included in several functional bits in the RXCP_50 block. Care should be taken to ensure correct usage of the RXCP_50 block.

PLPP RXCP BLOCK

The Receive Cell Processor (RXCP) Block integrates circuitry to support cell payload descrambling, header check sequence (HCS) verification and idle/unassigned cell filtering.

The RXCP operates upon a delineated cell stream. For PLCP based transmissions systems, cell delineation is performed by the SPLR. For non-PLCP based transmission systems, cell delineation is performed by the ATMF. Framing status indications from these blocks ensure that cells are not written to the RXFF while the SPLR is in the loss of frame state, or cells are not written to the RXFF while the ATMF is in the HUNT or PRESYNC states.

The RXCP descrambles the cell payload field using the self synchronizing descrambler with a polynomial of $x^{43} + 1$. The header portion of the cells is not descrambled. Note that cell payload scrambling is optional in the PLPP, and is required by CCITT Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are scrambled for the DS3 physical layer interface.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification, and CCITT Recommendation I.432.

The RXCP can be programmed to drop all cells containing an HCS error and/or to drop idle/unassigned cells. The idle/unassigned cell header pattern is completely programmable using four registers. Four header pattern mask registers are also provided.

A programmable hysteresis is provided when dropping cells based on HCS errors. When a cell with an HCS error is detected, the RXCP can be programmed to continue to discard cells until m (where m = 1, 2, 4, 8) cells are received with correct HCS. The mth cell is not discarded (see figure 4 of the PLPP data book, Issue 7, PMC-910812). Note that the dropping of cells due to HCS errors only occurs while the ATMF is in the SYNC state (for non-PLCP based transmission systems), or while the SPLR is in the in-frame state (for PLCP based transmission systems).

S/UNI-PDH RXCP BLOCK

The Receive Cell Processor (RXCP) Block integrates circuitry to support cell payload descrambling, header check sequence (HCS) verification and idle/unassigned cell filtering.

The RXCP operates upon a delineated cell stream. For PLCP based transmissions systems, cell delineation is performed by the SPLR. For non-PLCP based transmission systems, cell delineation is performed by the ATMF. Framing status indications from these blocks ensure that cells are not written to the RXFF while the SPLR is in the loss

of frame state, or cells are not written to the RXFF while the ATMF is in the HUNT or PRESYNC states.

The RXCP descrambles the cell payload field using the self synchronizing descrambler with a polynomial of $x^{43} + 1$. The header portion of the cells is not descrambled. Note that cell payload scrambling is optional in the S/UNI-PDH, yet is required by ITU-T Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are scrambled for the DS3 physical layer interface.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432.

The RXCP can be programmed to drop all cells containing an HCS error or to filter cells based on the HCS and/or the 4 octet cell header. Filtering according to a particular HCS and/or 4 octet header pattern is programmable through the RXCP configuration/control registers. More precisely, filtering is performed when filtering is enabled or when HCS errors are found when HCS checking is enabled. Otherwise, all cells are passed on regardless of any error conditions. Cells are blocked if the HCS pattern is invalid or if the filtering 'Match Pattern' and 'Match Mask' registers are programmed with a certain blocking pattern. Idle cells are not automatically filtered. If they are required to be filtered, then that filtering criterion (i.e. the Null cell pattern) must be programmed through the IDLE/Unassigned Cell Pattern and Mask registers. For ATM cells, Null cells (Idle cells) are identified by the standardized header pattern of 'H00, 'H00, 'H00 and 'H01 in the first 4 octets followed by the valid HCS octet. For PLCP cells, 'Null cells' (Idle cells) are identified by the standardized header pattern of 'B0xxxxxx, 'H00, 'H00, 'H00 in the first 4 octets followed by the valid HCS octet.

While the cell delineation state machine is in the SYNC state, the HCS verification circuit implements the state machine shown in "Figure 4 HCS Verification State Diagram" of the S/UNI-PDH data book, issue5, PMC-931011.

In normal operation, the HCS verification state machine remains in the 'Correction' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection' state.

A programmable hysteresis is provided when dropping cells based on HCS errors. When a cell with an HCS error is detected, the RXCP can be programmed to continue to discard cells until m (where m = 1, 2, 4, 8) cells are received with correct HCS. The mth cell is not discarded (see figure 4 of the S/UNI-PDH data book, Issue 5, PMC-931011). Note that the dropping of cells due to HCS errors only occurs while the ATMF is in the SYNC state (for non-PLCP based transmission systems), or while the SPLR is in the in-frame state (for PLCP based transmission systems).

Register 54H in the S/UNI-PDH contains the value for the LCD count threshold. This value is equal to *half* the number of cell periods the receive cell processpor must be out of delineation before LCD is declared. The LCD count is available in the S/UNI-QJET.

Registers 43H to 52H of the S/UNI-PDH represent cell patterns and match masks for the first 4 octets of the ATM cell. These octets are not directly available in the S/UNI-QJET.

S/UNI-QJET RXCP_50 BLOCK

The Receive Cell Processor (RXCP_50) Block integrates circuitry to support scrambled or unscrambled cell payloads, scrambled or unscrambled cell headers, header check sequence (HCS) verification, idle cell filtering, and performance monitoring.

The RXCP operates upon a delineated cell stream. For PLCP based transmissions systems, cell delineation is performed by the SPLR. For non-PLCP based transmission systems, cell delineation is performed by the ATMF. Framing status indications from these blocks ensure that cells are not written to the RXFF while the SPLR is in the loss of frame state, or cells are not written to the RXFF while the ATMF is in the HUNT or PRESYNC states.

The RXCP descrambles the cell payload field using the self synchronizing descrambler with a polynomial of $x^{43} + 1$. The header portion of the cells can optionally be descrambled also. Note that cell payload scrambling is enabled by default in the S/UNI-QJET as required by ITU-T Recommendation I.432, but may be disabled to ensure backwards compatibility with older equipment.

The HCS is a CRC-8 calculation over the first 4 octets of the ATM cell header. The RXCP verifies the received HCS using the accumulation polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the received HCS octet before comparison with the calculated result as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432.

The RXCP can be programmed to drop all cells containing an HCS error or to filter cells based on the HCS and/or the 4 octet cell header. Filtering according to a particular HCS and/or 4 octet header pattern is programmable through the RXCP configuration/control registers. More precisely, filtering is performed when filtering is enabled or when HCS errors are found when HCS checking is enabled. Otherwise, all cells are passed on regardless of any error conditions. Cells are blocked if the HCS pattern is invalid or if the filtering 'Match Pattern' and 'Match Mask' registers are programmed with a certain blocking pattern. ATM Idle cells are filtered by default. For ATM cells, Null cells (Idle cells) are identified by the standardized header pattern of 'H00, 'H00, 'H00 and 'H01 in the first 4 octets followed by the valid HCS octet. For PLCP cells, 'Null cells' (Idle cells) are identified by the standardized header pattern of 'B0xxxxxx, 'H00, 'H00, 'H00 in the first 4 octets followed by the valid HCS octet.

While the cell delineation state machine is in the SYNC state, the HCS verification circuit implements the state machine shown in "Figure 8 HCS Verification State Diagram" of the S/UNI-QJET data book, issue1, PMC-960835.

In normal operation, the HCS verification state machine remains in the 'Correction' state. Incoming cells containing no HCS errors are passed to the receive FIFO. Incoming single-bit errors are corrected, and the resulting cell is passed to the FIFO. Upon detection of a single-bit error or a multi-bit error, the state machine transitions to the 'Detection' state. Once in the 'Detection' state, any errors are treated as uncorrectable.

A programmable hysteresis is provided when dropping cells based on HCS errors. When a cell with an HCS error is detected, the RXCP_50 can be programmed to continue to discard cells until m (where m = 1, 2, 4, 8) cells are received with correct HCS. The mth cell is not discarded (see figure 6 of the S/UNI-QJET data book, issue1, PMC-960835). Note that the dropping of cells due to HCS errors only occurs while the ATMF is in the SYNC state (for non-PLCP based transmission systems), or while the SPLR is in the in-frame state (for PLCP based transmission systems).

Cell delineation can optionally be disabled, allowing the RXCP_50 to pass all data bytes it receives.

The LCD count threshold in the S/UNI-QJET is expanded to 10 bits, and is contained in registers 65H and 66H. In the S/UNI-QJET, the value represents the number of cell periods the receive cell processor must be out of cell delineation for before LCD is declared. This value is not multiplied by two as it is in the S/UNI-PDH.

HCK and FIXPAT are not provided in the S/UNI-QJET, as they are not useful features.

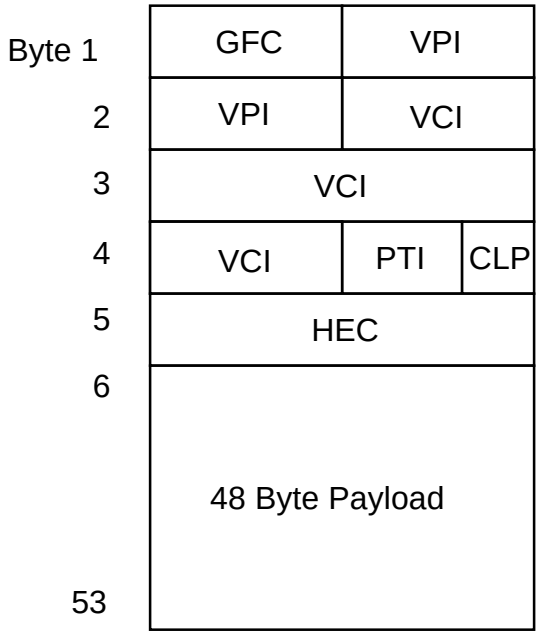
The DELIN bit is automatic in the S/UNI-QJET, with optional configuration provided by bits x61-2:3.

The FUDRI bit is not available to the S/UNI-QJET. Due to the way the RXCP_50 block is designed, an underrun cannot occur. If an overrun occurs, the RXCP_50 will not corrupt cells already in the FIFO.

The COCAI bit is not available to the S/UNI-QJET. An indication of a change in cell position is not important; an out of cell delineation (OOCD) is the only indication that is required.

Direct access is given to the ATM Cell header through the GFC, PTI, and CLP bits in register 67H. No access is given to the VPI or VCI. To illustrate the position of these bits in the ATM cell header, the ATM cell format in Figure 2 below.

Figure 2. ATM Cell format



TXCP Block

This section compares the TXCP blocks of the PLPP, S/UNI-PDH and S/UNI-QJET. Because the base - offset notation is not appropriate for this table, register addresses are provided in a register - bit notation instead.

Table 13a. TXCP Block Bits

Bit Name	PLPP Register - Bit	S/UNI-PDH Register - Bit	S/UNI-QJET Register - Bit
FIFORST	58 - 0	58 - 0	x80 - 0
DHCS	58 - 1	58 - 1	x81 - 1
SCR	58 - 2	58 - 2	x80 - 1, x80 - 5
FIFODP[0:1]	58 - 3:4	58 - 3:4	x81 - 2, x81 - 3
HCSADD	58 - 5	58 - 5	x80 - 2
HCSDQDB	58 - 6	58 - 6	x80 - 4
HCSINS	58 - 7	58 - 7	x80 - 3
FOVRI	59 - 1	59 - 1	x83 - 1
COCAI	59 - 2	59 - 2	x83 - 0
HCKI	59 - 3	59 - 3	Not available
TFULL4	Not available	59 - 4	x80 - 6
FIFOE	59 - 5	59 - 5	x83 - 6, x83 - 5
HCKE	59 - 6	59 - 6	Not available
FIXPAT	Always AA/55H	59 - 7	Not available

Table 13b. TXCP Block Octet Registers

Register Function	PLPP Register Location (Hex)	S/UNI-PDH Register Location (Hex)	S/UNI-QJET Register Location (Hex)
Idle cell pattern H1	5A	5A	x84
Idle cell pattern H2	5B	5B	Not Available
Idle cell pattern H3	5C	5C	Not Available
Idle cell pattern H4	5D	5D	x84
Idle cell pattern H5	5E	5E	Not Available
Idle cell payload	5F	5F	x85

The TXCP block in the S/UNI-QJET is replaced by a new block called TXCP_50. The functional descriptions for TXCP and TXCP_50 blocks are given below, describing the differences and similarities between the TXCP block of the S/UNI-PDH and the TXCP_50 block of the S/UNI-QJET. Because there is not a one-to-one correspondence between registers in the TXCP and TXCP_50 blocks, Table 13 lists specific bit names instead. Some of the bits that were available in the TXCP block are not available in the TXCP_50 block. Some of the functional bits in the TXCP are included in several functional bits in the TXCP_50 block. Care should be taken to ensure correct usage of the TXCP_50 block.

PLPP TXCP BLOCK

The Transmit Cell Processor (TXCP) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells is not scrambled. Note that cell payload scrambling is optional in the PLPP, and is required by CCITT Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are scrambled for the DS3 physical layer interface.

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and CCITT Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP inserts idle/unassigned cells. The idle/unassigned cell header is fully programmable using five internal registers. Similarly, the 48 octet information field is programmed with an 8 bit repeating pattern using an internal register.

S/UNI-PDH TXCP BLOCK

The Transmit Cell Processor (TXCP) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells is not scrambled. Note that cell payload scrambling is optional in the S/UNI-PDH, and is required by ITU-T Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell

payloads are scrambled for the DS3 physical layer interface (however discussions are ongoing to make scrambling a requirement in the future).

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP inserts idle/unassigned cells. The idle/unassigned cell header is fully programmable using five internal registers. Similarly, the 48 octet information field is programmed with an 8 bit repeating pattern using an internal register.

Registers 5AH to 5FH of the S/UNI-PDH represent cell patterns for the first 5 octets of the ATM cell. These octets not available in the S/UNI-QJET.

S/UNI-QJET TXCP_50 BLOCK

The Transmit Cell Processor (TXCP_50) Block integrates circuitry to support ATM cell payload scrambling, header check sequence (HCS) generation, and idle/unassigned cell generation.

The TXCP_50 scrambles the cell payload field using the self synchronizing scrambler with polynomial $x^{43} + 1$. The header portion of the cells may optionally also be scrambled. Note that cell payload scrambling may be disabled in the S/UNI-QJET, though it is required by ITU-T Recommendation I.432. The ATM Forum DS3 UNI specification requires that cell payloads are scrambled for the DS3 physical layer interface. However, to ensure backwards compatibility with older equipment, the payload scrambling may be disabled.

The HCS is generated using the polynomial, $x^8 + x^2 + x + 1$. The coset polynomial $x^6 + x^4 + x^2 + 1$ is added (modulo 2) to the calculated HCS octet as required by the ATM Forum UNI specification, and ITU-T Recommendation I.432. The resultant octet optionally overwrites the HCS octet in the transmit cell. When the transmit FIFO is empty, the TXCP inserts idle/unassigned cells. The 48 octet information field is programmed with an 8 bit repeating pattern using an internal register. Direct access to the ATM Cell header is given through the GFC, PTI, and CLP bits in register 84H of the S/UNI-QJET. No access is given to VPI and VCI. The ATM cell format is shown in the preceding section.

DHCS causes inversion of the HCS octet in the S/UNI-QJET. This is diferent from the S/UNI-PDH, in which DHCS inverts only one bit of the HCS byte.

HCKI, HCKE, and FIXPAT bits are not available to the S/UNI-QJET, as they are not useful features.

TTB Block

This section compares the TTB blocks of the S/UNI-PDH and S/UNI-QJET. Because the TTB block is specific to E3 applications, the PLPP has no TTB block.

Table 14. TTB Block

Register Function	PLPP Register Offset (Hex)	S/UNI-PDH Register Offset (Hex)	S/UNI-QJET Register Offset (Hex)
Base address (Hex)	Not Applicable	6C	x90
Control	Not Applicable	00	00
Trail trace identifier status	Not Applicable	01	01
Indirect address	Not Applicable	02	02
Indirect data	Not Applicable	03	03
Expected payload type	Not Applicable	04	04
Payload type label	Not Applicable	05	05

S/UNI-PDH TTB BLOCK

This block is equivalent to the TTB block in the S/UNI-QJET. The LEN16 bit in the control register selects the length of the message to be 16 bytes or 64 bytes.

S/UNI-QJET TTB BLOCK

The LEN16 bit in the S/UNI-PDH's TTB block is not available to the S/UNI-QJET. This bit position is reserved and should be set to logic 0 for proper operation, as LEN16 is automatically configured for E3 application.

PRGD Block

Since the PRGD block is unique to the S/UNI-QJET, it will not be discussed here. Please refer to the S/UNI-QJET data book for proper operation of this block.

General Configuration Registers

Although they cannot be specifically described as a functional block, the general configuration registers for the PLPP, S/UNI-PDH, and S/UNI-QJET have some similarities as discussed below. Because the base - offset notation is not appropriate for this table, register addresses are provided in a register - bit notation instead.

Table 15. General Configuration Registers

Register Function	PLPP Register - Bit	S/UNI-PDH Register - Bit	S/UNI-QJET Register- Bit
PLB	00 - 1	00 - 1	x00 - 0
DLB	00 - 2	00 - 2	x00 - 1
CLB	00 - 0	00 - 0	Not available
FRMRBP	00 - 3	00 - 3	x02 - 6:7, x03 - 6:7
LOOPT	00 - 4	00 - 4	x00 - 3
FIFOBP	00 - 5	00 - 5	Not available
E3ENBL	Not applicable	00 - 6	x02 - 6:7, x03 - 6:7
LLB	Not available	00 - 7	x00 - 2
RFDLE	01 - 0	01 - 0	x51 - 7
XFDLE	01 - 1	01 - 1	x5B - 0:3
PMONE	01 - 2	01 - 2	x11 - 2
FRMRE	01 - 3	01 - 3	register x31, x3A, x46, x48
RBOCE	01 - 4	01 - 4	x98 - 0:2, xA1 - 5:7
RXCPE	01 - 5	01 - 5	x63 - 0;3
TXCPE	01 - 6	01 - 6	x83 - 5:7
SPLRE	01 - 7	01 - 7	x09 - 0:6
Int Status Register	02 - 0:4	02 - 0:7	x05 - 0:7
TPNINV	03 - 0	03 - 0	x02 - 0:1
TCLKINV	03 - 1	03 - 1	x02 - 2
TUNI	03 - 2	03 - 2	x02 -3
RPNINV	03 - 3	03 - 3	x03 - 0:1
RCLKINV	03 - 4	03 - 4	x03 -2
DLINVERT	03 - 5	03 - 5	x04 - 0
8KREF	Not available	03 - 6	x00 - 7
TICLK	Not available	03 - 7	x02 - 4
ID / master reset	04 - 7	04 - 0:7	x06 - 0:2, x06 - 4:7, x98 - 2

As with other registers, mnemonics and minor functionality may be different between PLPP, S/UNI-PDH, and S/UNI-QJET devices. Care should be taken to ensure correct operation of the general configuration registers.

PLPP CONFIGURATION REGISTERS

The bits used to configure the PLPP are given in table 15 above.

S/UNI-PDH CONFIGURATION REGISTERS

The bits used to configure the SUNI-PDH are given in table 15 above.

S/UNI-PDH CONFIGURATION REGISTERS

Cell loopback is not available in the S/UNI-QJET.

The FIFOBP bit is not available in the S/UNI-QJET, but equivalent functionality can be configured using the TXCP_50 and RXCP_50 blocks, although the interface is via the UTOPIA bus instead. The relevant configuration bits are CCDIS in register x61H, HCSB in register x80H, and DS27_53 in register x00H.

In addition to the reset bit provided in register x06H, a per-quadrant reset is available using bit 2 of register x9BH.

CONTACTING PMC-SIERRA

PMC-Sierra, Inc.
105 - 8555 Baxter Place
Burnaby, B
Canada V5A 4V7

Telephone: 604-415-6000
Facsimile: 604-415-6200

Product Information: info@pmc-sierra.bc.ca
Applications information: apps@pmc-sierra.bc.ca

World Wide Web Site: http://www.pmc-sierra.com

NOTES

PMC-961125 Issue date: November 1996.

Printed in Canada