PM7322

RCMP
FAQ

Issue 1: October 30, 1995

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INTRODUCTION

This application note can be used in conjunction with the RCMP Engineering Documentation to aid the understanding of the application of the RCMP. The following contains a brief overview of the RCMP, followed by a list of frequently asked questions, and finally a list of abbreviations.

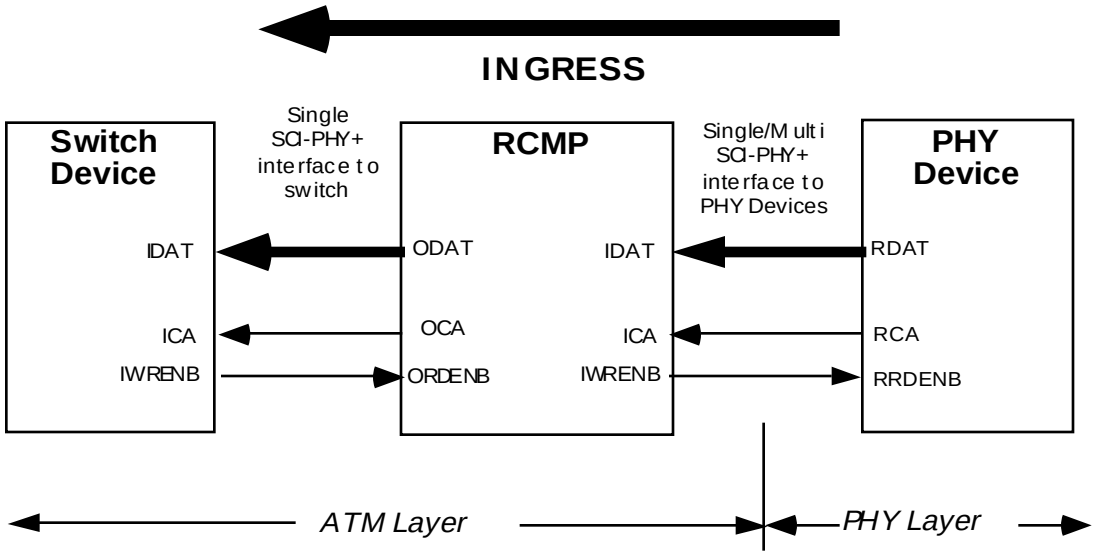
OVERVIEW

The RCMP performs ATM Layer functions: 1) Header translation and cell append for Routing, 2) Policing, 3) Cell counting and 4) OAM cell processing and routing, for 64K Virtual Channels (VC's). It provides SCI-PHY+[1] interface at both the physical and the switch sides. Multicasting is supported. The RCMP also provides cell insert/extract through the microprocessor interface and DMA access. The RCMP supports the ingress function primarily, but can be configured for use in the egress direction in single-PHY applications.

Main application areas for the RCMP are in the WAN and WAN access equipment: 1) Edge Switches, 2) Enterprise Switches, 3) Core Switches and 4) Access Muxes and Residential Broadband Switches.

The RCMP is fabricated in a 0.6 micron, 5v technology and housed in a 240-pin copper slugged plastic quad flat pack (PQFP) package.

Fig. 1 Typical Use of RCMP



[1]SCI-PHY stands for SATURN Compliant Interface for ATM PHY (Physical Layer) Devices. SCI-PHY+ includes extensions necessary for connecting to an ATM switch core.

FREQUENTLY ASKED QUESTIONS

Q: Does the RCMP perform actual routing of cells?

No, the RCMP performs header translation and appends appropriate bytes, all to be used by the switch core to physically route the cells.

Q: Are there any restrictions of the VPI/VCI address for cells to be processed by the RCMP?

There is no restriction on the VPI/VCI address range. There is complete address flexibility, which is a key advantage of the RCMP.

Q: How does the RCMP perform policing?

Two successive policing algorithms[2] are performed on each VC. In the case of Constant Bit Rate (CBR) connections, only one policing is needed for Peak Cell Rate (PCR) and Cell Delay Variation (CDV) conformance. In the case of Variable Bit Rate (VBR) connections, one policing is done for Peak Cell Rate (PCR) and Cell Delay Variation (CDV) conformance, and another policing is done for Sustained Cell Rate (SCR) and Burst Tolerance (BT) conformance.

Q: How does the RCMP handle AAL5 packets?

Since AAL5 packets can be very long (up to 1366 cells), if one cell within a packet is dropped because of non-conformance, then the entire packet has to be retransmitted, which would waste a lot of bandwidth. Thus, the RCMP can be configured such that all successive cells in an AAL5 packet can be dropped or tagged[3] on a per-VC basis, if any cell is dropped or tagged.

Q: What are the priorities of the different cells that are inserted by the RCMP?

RCMP-generated Performance monitoring cells have the highest insertion priority. This is followed by cells received in the input FIFO and cells from microprocessor. RCMP-generated Fault Management cells (such as AIS, RDI cells) have the lowest priority.

[2]The RCMP uses an approximation to the Virtual Scheduling Algorithm (or called the continuous-state leaky bucket) as specified in ITU-T Recommendation I.371 and ATM Forum UNI 3.0.
[3]Dropping means the cell is eliminated. Tagging means setting the Cell Loss Priority bit in the ATM cell header such that the cell becomes low-priority.

Q: What kind of cell structure does the RCMP handle?

The RCMP supports the SCI-PHY+ interface cell formats:

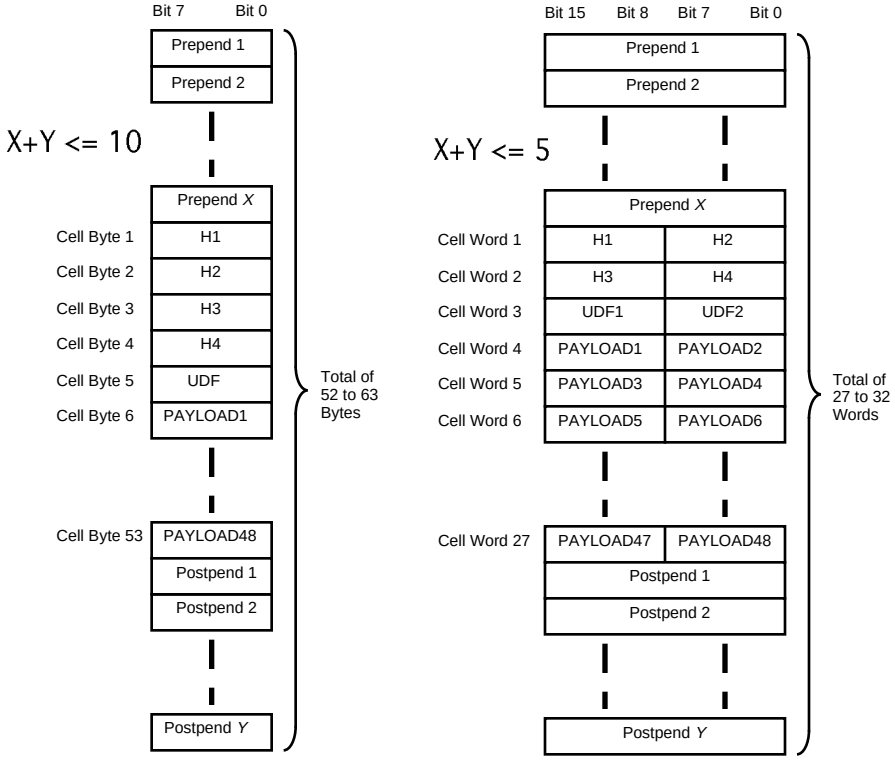
The ATM cell size can range from 52 to 63 octets (8-bit format), or 27 to 32 words (16-bit format). The 53 octet ATM cell can be appended as follows:

8-bit mode: Up to 10 octects before and/or after the ATM cell

16-bit mode: Up to 5 words before and/or after the ATM cell, plus the UDF2 octet (total of 11 octets)

Refer to Fig.1 for the ATM cell structure.

Fig.1 ATM cell format



Note: In 8-bit mode, the UDF (User-defined) octet takes the place of the HEC, since HEC is not used in the ATM layer. This UDF octet can be omitted, making the ATM cell 52 octets long. In 16-bit mode, UDF1 takes the place of HEC; both UDF1 and UDF2 are user-defined octets.

Q: Can the RCMP be used in the egress direction?

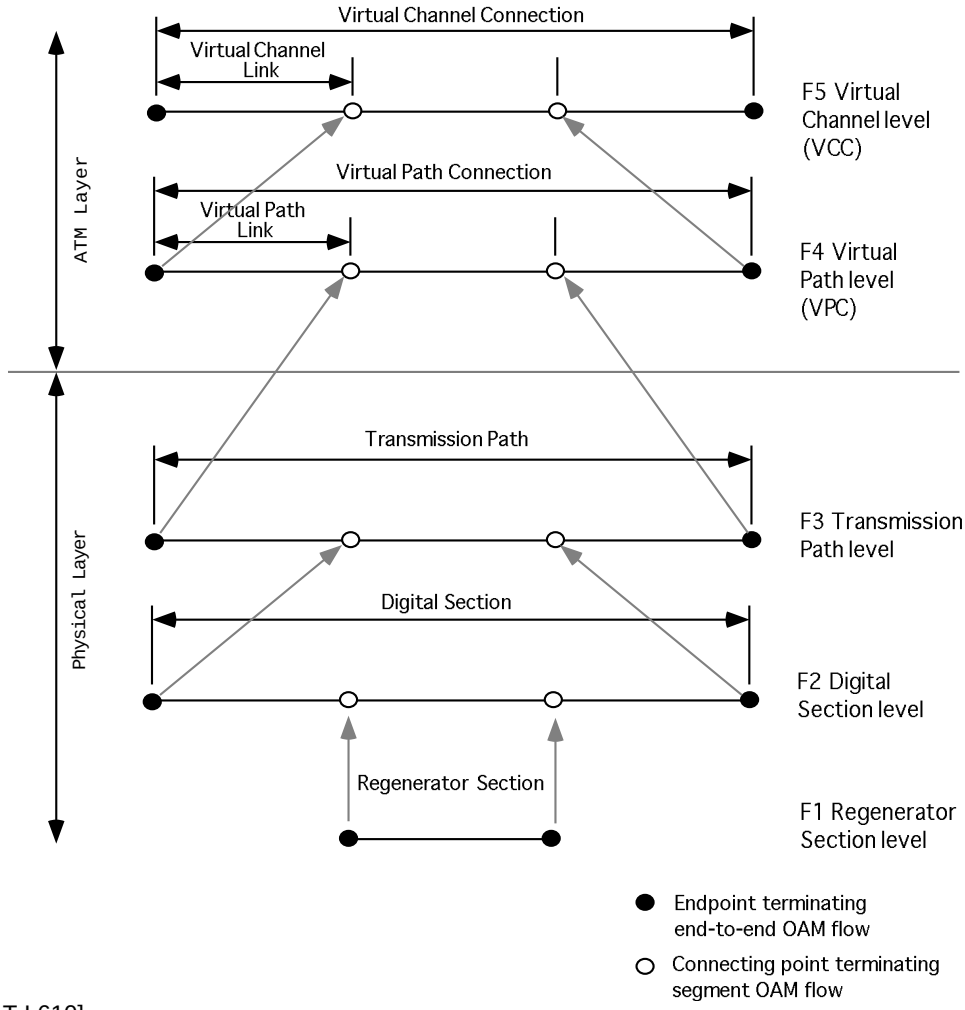
Yes, the RCMP can be configured for use in the Egress direction to provide header translation and OAM processing in a single-PHY application. The output of the RCMP can be connected directly to a PHY slave. The input of the RCMP, being a PHY master,

will need some glue logic (which includes a FIFO) to interface with a switch ASIC that is also a PHY master.

Q: What kind of OAM cells does the RCMP process?

The RCMP processes F4 (Virtual Path) and F5 (Virtual Channel) level OAM cells. Refer to Fig. 2 for a definition of F4 and F5 levels in a network. There are 3 main types of OAM cells processed: 1) Performance Monitoring cells for error counting , 2) Fault Management cells for fault notification and isolation and 3) Resource Management cells for bandwidth allocation in ABR services.

Fig. 2 OAM cell flow in network



[Source: ITU-T I.610]

Q: How can Resource Management (RM) cells be processed quicker?

In Available Bit Rate (ABR) connections, a closed-loop control system is used to control the bandwidth available for user, and RM cells carry the traffic and congestion information from the network nodes to the transmission source, which will adjust the bandwidth usage accordingly. It is therefore advantageous to speed up the processing of RM cells coming in the ingress direction, such that they can return to the source quicker in the egress direction. Instead of letting the RM cells go through the switch core to get to the egress direction, the RCMP puts a special tag on these RM cells so that they can be extracted by an external processing device and routed to the egress direction immediately. This special tag is added by overwriting an arbitrary header or appended byte.

Q: How is multicast accomplished in the RCMP?

The RCMP can perfrom logical multicasting[4]. A single received cell can result in an arbitrary number of cells (or branches) at the output, each with its own unique VPI/VCI value and appended bytes, but with the same cell payload. Each branch has it own VC Table entry[5]. Rate policing, cell counting and OAM is then performed independently for each branch. Note that multicasting affects the overall cell throughput, since the multicasting action is completed before any in new input cells are processed.

Q: What SRAM's can be used with the RCMP?

The RCMP requires external SRAM's to provide storage of the VC table for each VC supported. The VC Table is a database that indicates how cells are processed and stores the result of the processing and monitoring functions.

Each VC requires 16 word x 40 bits of memory. Together with 5 bits of parity, one needs a 45 bit data bus. Considering the common SRAM sizes available in the market, one solution is to use 2 64Kx18 chips for the 36 bits of data, and 2 32Kx9 chips for the remaining 9 bits. This will provide memory for 4K VC's. Another requirement is fast access time. With a maximum speed of 50MHz operation (ie. 20ns period), and a worst case setup time of 4ns at the RCMP, the SRAM should have access times of less than 15ns to provide enough margin.

Q: What kind of glue logic is required for the time-critical SRAM interface?

The most time-critical interface operation is the SRAM address decoding. The RCMP has a worst case prop delay of 12ns, and a typical setup time for a synchronous SRAM is 2ns. A 20ns clock period (max. frequency of 50MHz) means there is only 6ns for address decoding.

[4]Logical multicast means broadcasting copies of a VC to the same physical port. This is in contrast with spacial multicast where there are multiple physical ports for the VC copies to go to.
[5]Each VC has a table stored in external memory. This table contains all the information required for cell, processing such as header translation and policing functions.

The Cypress PAL20 16-L8, with a prop delay of 4.5ns, or the Phillips PLQ20L8 with 5ns prop delay should suffice.

Q: Can the 3v SRAM be used with the RCMP (5v)?

1. From 5v to 3v: Many 3v memories have 5v-tolerant inputs. For memories that do not, one can use a level translator such as the National LVX3L383 or LVX3L384, which has a delay of only 250ps. Or, one can use a simple voltage divider, as long as the DC current is not too high (< 12mA).

2. From 3v to 5v: one can interface the 3v output directly to the 5v, since the RCMP has TTL level inputs.

A good reference is the National Semiconductor databook: "Crossvolt Low Voltage Logic Series", page 4-3 to 4-9

Q: Using a 3v SRAM with the RCMP (5v), what if the 3v power supply is turned on first?

We do not recommend having the 5v power to RCMP off while I/O's are being driven, because this could result in large amount of current through the fully turned-on protection diodes in the RCMP I/O pads. However, if this cannot be avoided, the following solutions can be considered:

1) The best solution is to make sure that the SRAM will not be driving data out when it is powered-up. The SRAM will only be driving data out in a *read* operation. To perform a *read*, three signals are required to be in the following states: Chip-select Bar (CSB) asserted, Output Enable Bar (OEB) asserted, and Write Enable Bar (WEB) de-asserted. In the case where the RCMP is powered-down, these signals will be low: thus, CSB and OEB will be asserted, but WEB will also be asserted, which indicates a WRITE operation and therefore, the SRAM should not be driving the data lines (in this case they are tristated).

To add a bit of safety margin, it would be better to put a pull-up on the OEB signal.

2) The second best solution is to put a diode from the 3v to the 5v, such that the 5v supply will not be more than a diode drop lower than the 3v supply. First, a Schottky diode would be preferable, since it has a voltage drop of less than 0.7v (the lower the better, since it will reduce the voltage applied to the protection diodes) Second, the current running through this diode should not be high. If there is no clock supplied to the RCMP, it should consume very negligible power. Even with a clock (50MHz) running, with the RCMP in reset, the only power-consuming circuit will the the clock net inside. The resulting power is estimated to be much less than 100mW. With a diode drop of say, 0.5v, there is less than 200mA current through the diode.

ABBREVIATIONS

ABR	Available Bit Rate service
AIS	Alarm Indication Signal
BT	Burst Tolerance
CBR	Constant Bit Rate service
CDV	Cell Delay Variation
OAM	Operations, Administrative and Maintenance
PCR	Peak Cell Rate
PM	Performance Monitoring
RDI	Remote Defect Indication
RM	Resource Management
SCR	Sustained Cell Rate
VBR	Variable Bit Rate service
VCC	Virtual Channel Connection
VPC	Virtual Path Connection

NOTES

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