

PM5945

SONET ATM PHYSICAL INTERFACE (SAPI) APPLICATION BOARD ERRATA

Issue 1: October 25, 1995

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NEW ISSUE OF THE SAPI REFERENCE DESIGN ERRATA

This document is the errata notice for Issue 3 of the SONET ATM PHYSICAL INTERFACE (SAPI) APPLICATION BOARD reference design document (PMC-940106P3).

ISSUE 1 ERRATA (OCTOBER 25, 1995)**1. SCHEMATIC CHANGES****1.1 The active low JTAG test reset pin (TRSTB, pin 82) should be tied to RSTB for proper operation.**

The TRSTB signal provides an asynchronous S/UNI test access port reset via the IEEE P1149.1 test access port. If no reset is applied, the JTAG test circuitry can power up in a state which results in the microprocessor data bus being driven continuously low. This disables any and all accesses to the S/UNI-155 device until the JTAG test circuitry is reset through the TRSTB pin. To avoid this situation, the TRSTB should be tied to the RSTB pin, so that a power-up reset will also clear the JTAG test circuitry.

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