PM5355

S/UNI-622™

S/UNI-622™ ATM Reference Design with Multimode Optics

Preliminary Information

Issue 3: October 11, 1996

Table of Contents

OVERVIEW

The S/UNI-622 implements the SONET/SDH overhead processing and ATM convergence layer functionality required in an ATM system. This device integrates duplex operation by appropriate termination (or origination) of the SONET overhead and the extraction (or mapping) of the ATM payload in the receive (or transmit) path. In the receive direction, the SONET section (SOH), line (LOH) and path (POH) overhead are terminated and the ATM cells are extracted from the SONET payload. These extracted cells are made available to the external AAL processor via the SCI-PHY interface on the DROP side. In the transmit direction, the ATM cells received through the SCI-PHY interface are mapped into the SONET payload prior to the addition of the section (SOH), line (LOH) and path (POH) overhead. Once the SONET signal is assembled, it is transmitted out in a byte serial manner.

To build the core functionality of an ATM switching system (or an ATM router or an ATM terminal) the S/UNI-622 must be interfaced appropriately to the optical line and the SCI-PHY interface. In the receive direction the process required is to convert the optical data to electrical format, recover the clock and transform the serial data into a bytewise parallel form before connection to the S/UNI-622. The S/UNI-622 then handles the termination of the SONET line and the extraction of the ATM payload. In the transmit direction, the reverse process of converting the byte serial ATM mapped SONET data (from the S/UNI-622) to serial before conversion to the optical format is required. Logically, this is a simple function. However, because of the high speed signals involved in this design, the layout task must be effectively designed to minimize reflections due to transmission line effects at the 622MHz and 77MHz interfaces. This includes controlling the characterization of the transmission lines, keeping line distances short and incorporating extra circuitry dedicated for termination.

In this reference design the O/E conversion and the E/O conversion is carried out by the Hewlett Packard HFBR-5207 Multimode Fiber Transceiver. In the receive direction the HP HFBR-5207 converts the optical data to electrical PECL. This device also contains an integrated clock recovery circuit. The extracted clock and data is connected to a Vitesse VSC8110 which does the serial to parallel conversion before interfacing to the S/UNI-622. Note that the PECL serial receive data is level-shifted to interface properly with the Vitesse ECL input, which expects input signals between 0 to +2v. In the transmit direction, the S/UNI-622's bytewise data is taken by the Vitesse VSC8110 and converted to a serial stream at the 622Mhz rate. The HP HFBR-5207 takes the 622MHz serial data stream and converts it to optical format at the same frequency. Note that the serial transmit data from the Vitesse VSC8110 is level-shifted to PECL levels to interface properly with the HP optics. As already mentioned above, the layout between the HP HFBR-5207, and the VSC8110 is critical and should be controlled to minimize transmission line distances. Also, appropriate termination (with the characteristic impedance) at the end of the line is required to eliminate transmission line effects.

At the system side, the DROP and ADD interfaces to the S/UNI-622 allow the reception and transmission of ATM cells. The DROP side passes the extracted cells to the ATM/AAL layer processor device via the receive SCI-PHY interface. The ADD side receives the assembled ATM cells from the ATM/AAL processor via the transmit SCI-PHY interface. Both the DROP and ADD interfaces are configurable to be either 8 bit wide or 16 bit wide.

The microprocessor interface allows access to the S/UNI-622 internal registers. These are used to configure the S/UNI-622 into its various operating modes as well as to monitor the performance and status of its internal functions. When operating in the STM12c/STM-4 mode the internal configuration registers will default (on power up) to a state where microprocessor access is not required. In this mode, it is possible to do without a microprocessor interface and therefore avoid some expense. However, it should be noted that this will also limit the observability of internal status and general performance information that is normally available through the reading of internal registers.

This reference design implementation is shown in the block diagram below.

BLOCK DIAGRAM

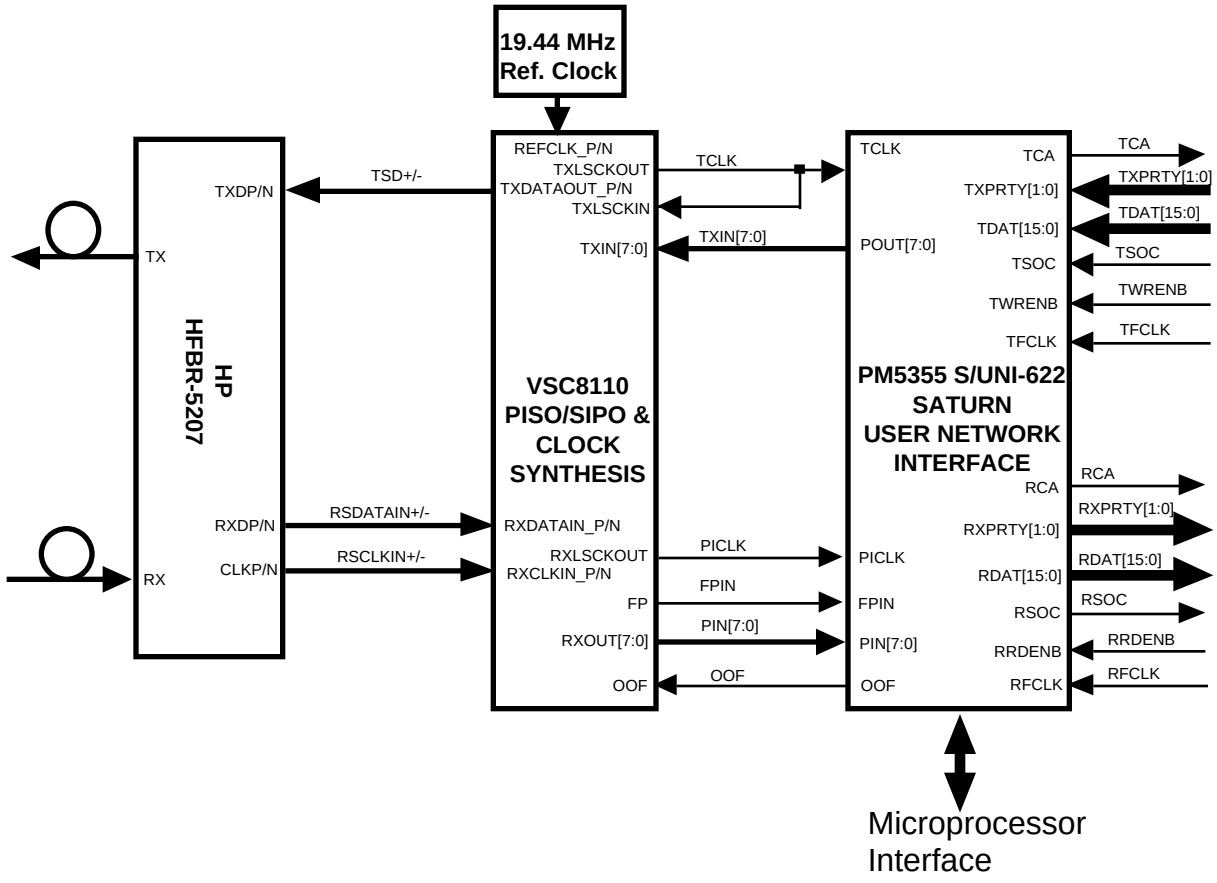


Figure 1. Block Diagram of 622 SONET/ATM Core.

IMPLEMENTATION DESCRIPTION

Sheet 1: Power Supply Protection & Regulation, SCI-PHY Expansion Board Connectors.

FUNCTION

The function of this sheet is to provide a regulated VMM (+2V) output for the Vitesse VSC8110, and to provide the SCI-PHY and microprocessor interface to the S/UNI-622.

IMPLEMENTATION

Power Supply Protection & Regulation

All capacitors shown are for power supply decoupling. The voltage regulator (LM317) supplies the +2V as controlled by resistors R10 and R29. The Vitesse VSC8110 utilizes power from the VMM output for its serial 622 serial input/output interface with the HP optics.

SCI-PHY Expansion Board Connectors

The AMP103911-8 and the AMP103911-2 together make up a 120 pin connector for interfacing to an external SCI_PHY motherboard, microprocessor and power supply module. This interface will be connected to the SCI-PHY motherboard and the microprocessor motherboard via an intermediate translation board that will map these pins to the target motherboard. This intermediate board will supply GND (0.0V) and VDD (+5.0V) power on the various connector inputs.

For microprocessor interfacing the address is received on the A[7:0] inputs and the data is transported on the D[7:0] pins. The read, write, address latch enable and chip select signals are received on the RDB, WRB, ALE and CSB inputs. All signals ending in "B" are active low. For the micro access timing, refer to the S/UNI-622 PMC-Sierra data book.

The remaining pins in these connectors, with the exception of the power supply pins, are dedicated to the SCI-PHY interface. The transmit cell available signal is received on the TCA input. The receive cell available signal is received on the RCA input. The receive data parity signals are received on the RXPRTY[1:0] inputs. The receive start of cell indication is indicated on the RSOC input. The receive cell data in transferred on the RDAT[16:0] inputs from the S/UNI-622 to the SCI-PHY device. The transmit cell data is transferred from the SCI-PHY device to the S/UNI-622 on the TDAT[16:0] outputs. The writing of the data into the S/UNI-622 is timed synchronous to the TFCLK output. The transmit start of cell indication is signaled to the S/UNI-622 on the TSOC output. The transmit data parity signals are conveyed on the TXPRTY[1:0] outputs. The cell data write enable is validated with the WRENB output. The data

read from the S/UNI-622 is synchronously controlled by the RFCLK clock output and the RRDENB output

The remaining pins on this 120 pin connector are dedicated to the power supply inputs from an external power supply module. The VDD (+5.0V) will be supplied on 8 connector inputs and the GND (0.0V) will be supplied on 34 connector inputs.

The power supply decoupling and rumble capacitor is also shown on this sheet. These components must be placed close to the connector inputs and the rumble capacitor must be 10µF polarized.

Sheet 2: S/UNI-622 Interconnect.

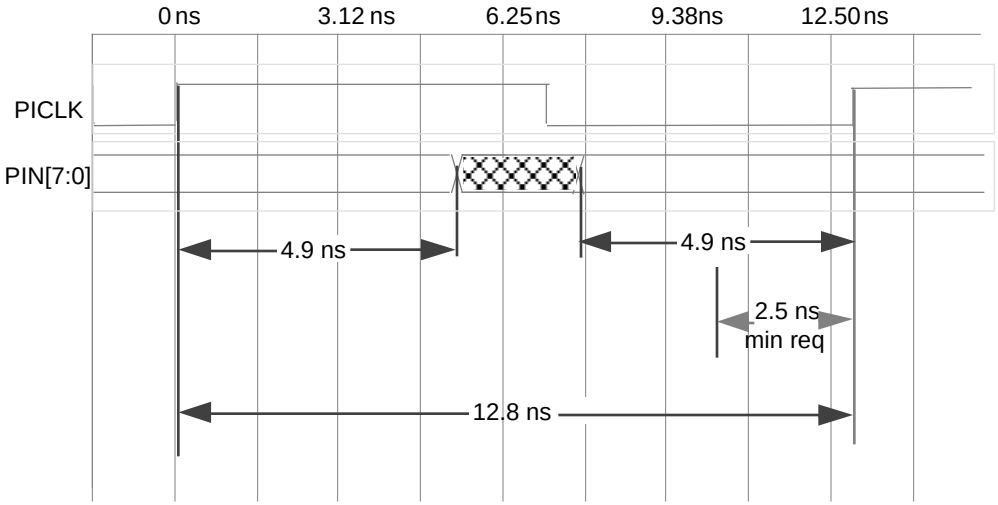
FUNCTION

The function of this sheet is to provide interconnect between the S/UNI-622, the VSC8110 (serial to parallel converter and parallel to serial converter), the SCI-PHY interface, and the microprocessor interface. Other functionality contained in this sheet provides retiming of the POUT[7:0] output, pullup/pulldown of the unused inputs and an LED display of some alarm indications.

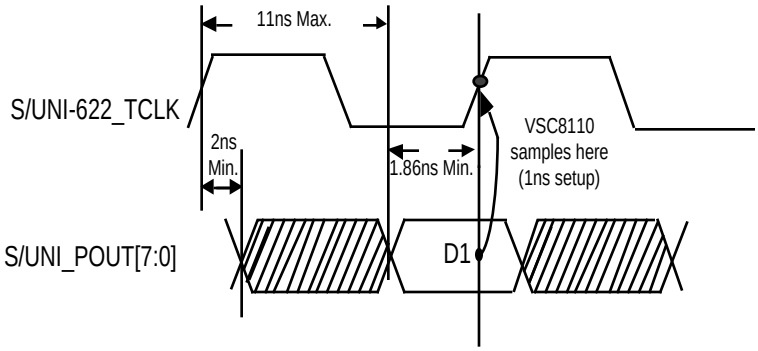
IMPLEMENTATION

The connections to the S/UNI-622 are depicted in the block diagram shown in figure1. The five main interfaces are the byte serial receive interface, the byte serial transmit interface, the SCI-PHY transmit interface, the SCI-PHY receive interface and the microprocessor interface. All unused inputs are connected to pulldown or pullup resistors via 1K resistor packs.

The byte serial receive interface consists of the PICLK, FPIN, FPOS and PIN[7:0] inputs. The PICLK input is a 77MHz signal derived by the VSC8110 by dividing the recovered clock by 8. This clock is used by the S/UNI-622 to sample the FPIN and PIN[7:0] inputs. The PICLK is terminated at the S/UNI-622 with the resistor network consisting of R18 and R13. FPOS is pulled high via a 1K resistor to enable FPIN to mark the third byte of the A2 byte of the SONET frame. The diagram below shows the marginal setup time that exists between the VSC8110 outputs and the S/UNI-622 PICLK and PIN[7:0] inputs. This identical timing exists with the FPIN input as well as the PIN[7:0]. Since there is only a 0.2ns timing margin on the setup time (data valid to the rising edge of clock) on the FPIN and PIN[7:0] inputs, precautions must be taken to avoid skew between these inputs. In fact, a slight delay (in the order of 1-5ns) in the data path would be advantageous and a slight delay (greater than 0.2ns) in the clock path would be intolerable. Hold time is not a concern on this interface since only 3ns are required and there are 11.9ns available.



The byte serial transmit interface consists of the TCLK and TFP inputs and the FPOUT and POUT[7:0] outputs. The TCLK input is a 77MHz signal derived by the VSC8110 by dividing the synthesized TXCK 622MHz clock by 8. The TFP input is tied low via a pull down resistor and the output data is arbitrarily aligned after powerup reset. TCLK is used by the S/UNI-622 to retime its FPOUT and POUT[7:0] outputs and is terminated at the S/UNI-622 with the resistor network consisting of R27 and R23. The VSC8110 has a setup time of 1.0ns on its TXIN[7:0] inputs. Combined with the propagation delay through the S/UNI-622 gives 12.0ns. Since this is less than one clock cycle, the transfer of data into the VSC8110 is guaranteed. The following timing diagram shows this more clearly. The S/UNI_POUT[7:0] waveform shows the relationship between the data out of the S/UNI-622 and its transmit clock, S/UNI-622_TCLK. This same clock is used to clock the data into the VSC8110.



The SCI-PHY transmit interface is implemented by the TFCLK, TSOC, TXPRTY[1:0], TWRENB and TDAT[15:0] inputs and the TCA output. These connections connect directly to the SCI-PHY interface connector on sheet 1.

The SCI-PHY receive interface is implemented by the RRDENB, RFCLK inputs and the RSOC, RXPRTY[1:0], RDAT[15:0] and RCA outputs. These connections also connect directly to the SCI-PHY interface connector on sheet 1.

The outputs POP0 to POP5 are used by the VSC8110 to determine the mode of operation. These outputs can be set to any value by writing to the internal S/UNI-622 registers associated with this port.

The microprocessor interface is implemented by the D[7:0] (bidirectional), A[7:0], ALE, CSB, WRB and RDB inputs. These connections connect directly to the microprocessor interface connector on sheet 1.

The 74HCT245 and the LED display circuitry interfaces to eight alarm signals generated by the S/UNI-622. Various other outputs of the S/UNI-622 are connected to observation points for easy probing during debug; these are provided by the TPn test points.

All capacitors are for power supply decoupling local to the S/UNI-622, and 74HCT245.

Sheet 3: Vitesse VSC8110 Interconnect

FUNCTION

The function of this sheet is to provide serial to parallel conversion (of the data received from the optics) and parallel to serial conversion (of the data transmitted to the optics). Clock synthesis is also implemented in this schematic.

IMPLEMENTATION

All data and clock traces are characterized with a 50Ω characteristic impedance (terminated accordingly at the end of the line) and should be kept short to reduce transmission line effects.

The VSC8110 transforms the bit serial receive data on its RXDATAIN_P and RXDATAIN_N inputs into a bytewise parallel form on the RXOUT[7:0] outputs. It is vital that the layout of the interface between the HP HFBR-5207 optics outputs and the VSC8110 inputs introduce no clock skew between the VSC8110 RXCLKIN_P and the RXDATAIN_P signals. This is achievable if layout and termination precautions are taken as mentioned in the overview. Note that AC-coupling capacitors are used to interface the PECL level clock and data signals from the HP HFBR-5207 to the 0V to +2V levels required by the VSC8110. The DC bias into the VSC8110 is set to 0.7V by the resistor network (147ohm to VMM (+2V) and 76 ohm to ground).

In the opposite direction there is no required clock and data relationship, since the HP HFBR-5207 only requires the transmit data. However, the same layout precautions should be taken so that there is no skew between the VSC8110 differential data pair outputs TXDATAOUT_N and TXDATAOUT_P. Note that AC-coupling capacitors are

used to interface the 0V to +2V level data signals from the VSC8110 to the PECL levels required by the HP HFBR-5207. The pull-down resistors, R17 and R32, at the VSC8110 TXDATAOUT_P and TXDATAOUT_N outputs have a value of 50 ohms, as opposed to 270ohms as recommended by Vitesse. This is done to increase the signal swing from 300mV to 500mV, which will be sufficient for the HP HFBR-5207 inputs.

The VSC8110 also generates a byte rate clock and a frame pulse on the FPIN and PICLK outputs. In the transmit direction, the POUT[7:0] byte serial data is converted into a bit serial output stream on the TSD+/- outputs. The VSC8110 also synthesizes a 77MHz TCLK and the 622MHz TXCK outputs using a 19.44MHz reference on its REFCLK_P/REFCLK_N PECL clock input.

The remaining passive circuitry implements transmission line termination and pullup pulldown and power supply decoupling functions.

Sheet 4: Optics Interface.

FUNCTION

The function of this sheet is to provide the optical interface in the receive and transmit directions. In the receive direction clock and data recovery is also implemented.

IMPLEMENTATION

The HP HFBR-5207 receives the optical signal and outputs the electrical recovered data on its RXDP and RXDN outputs, and the recovered clock on its CLKP and CLKN outputs.

In applications where the recovered clock frequency is not allowed to drift upon loss of input optical signal, the HP HFBR-5207 can generate a local clock output by multiplying an external 19.44MHz reference clock (connected to the REF_CLK input) to 622MHz. This feature is controlled by the active-low lock to reference input (LCK_REFB). This input is driven by the Signal Detect (SD) output from the HP HFBR-5207. That is, if the receiver section detects loss of optical signal, SD will be asserted, and this will cause the HP HFBR-5207 to lock to the reference clock.

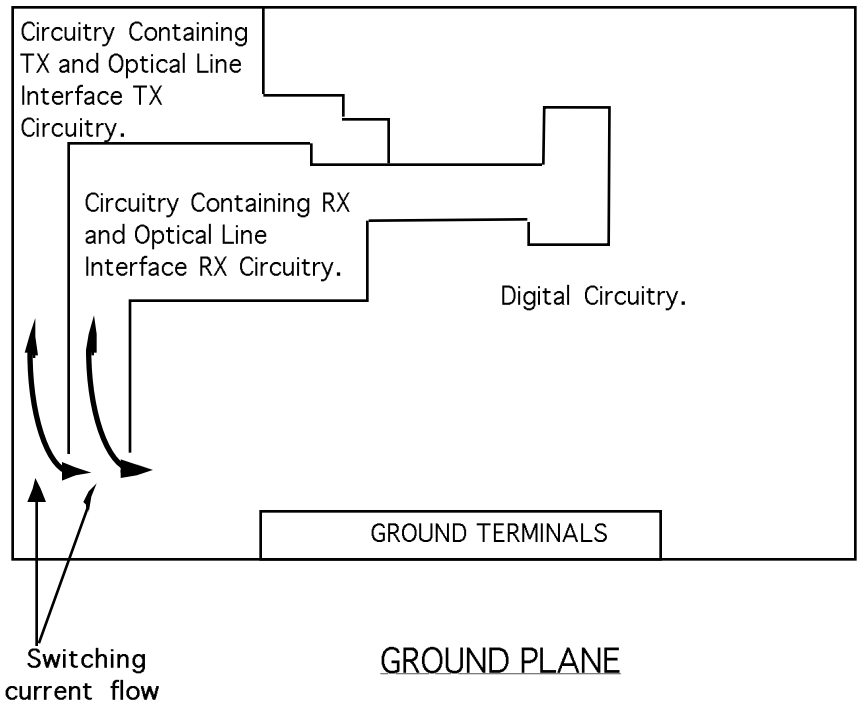
The passive components around the receiver section of the HP HFBR-5207 are for decoupling the power supply, providing emitter pulldown and termination of the 50Ω transmission line. The termination resistors should be placed at the end of the transmission line and the power supply decoupling capacitors should be placed as close as possible to the HP HFBR-5207.

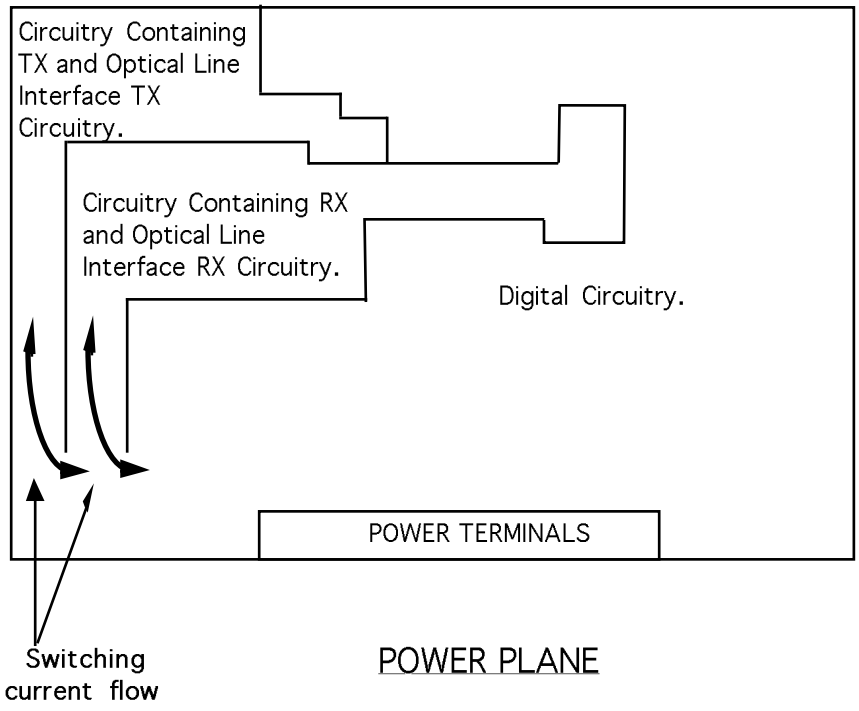
The HP HFBR-5207 transmits the optical signal to the line. This device takes the serial electrical data on the TSD+/- inputs and converts the signal to an optical format. The passive components around the HP HFBR-5207 are for decoupling the power supply and termination of the 50Ω transmission line. The DC bias of the TXDP and TXDN inputs are set to 3.7V by a resistor network (191ohms to +5V and 68.1ohms to

ground). The decoupling capacitors should be placed as close as possible to the HP HFBR-5207.

LAYOUT DESCRIPTION

In general the layout must be designed to minimize the noise coupling between the different interfaces on this board. Besides the usual capacitive decoupling methodology, further isolation can be provided by dedicating power and ground planes to distinguishable sections of circuitry. Such divisions can be made by grouping transmit and receive circuitry into two separate groups and further into analog and digital groups. By isolating in this way, the general noise level on the whole board can be kept minimal. An example of such a scheme is illustrated in the two diagrams below.



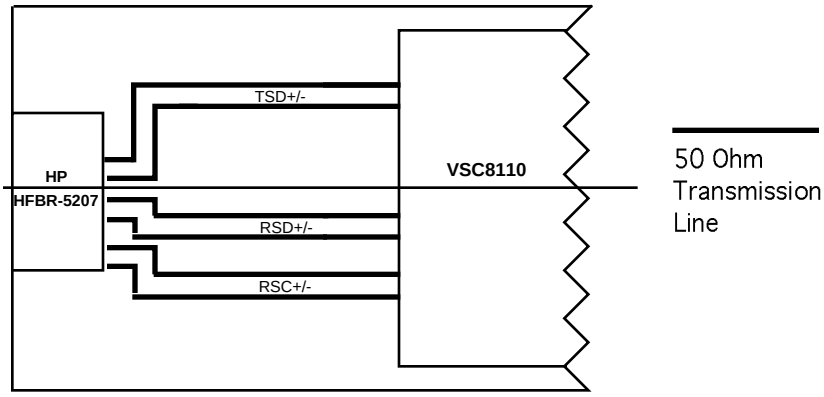


The actual layout can be seen in the layout schematic provided in this document. Throughout this design, high speed signal termination and noise reduction techniques outlined in the following text have been considered.

High Speed Signal Termination

Trace Impedance Control

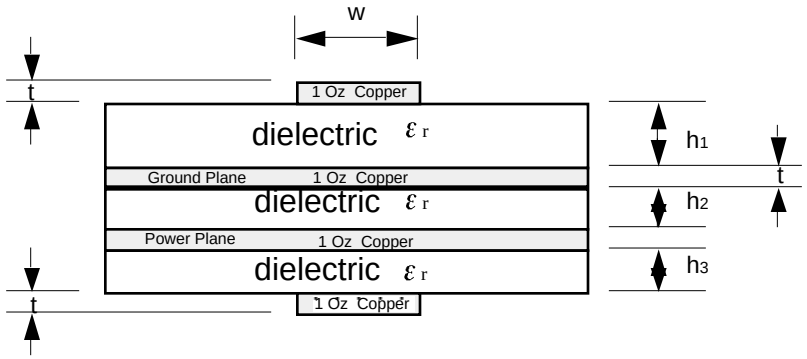
To reduce signal degradation due to reflection and radiation, the impedance of all high frequency signals should be treated as transmission lines and terminated with a matching impedance at the destination. In this design, all high speed signal traces use 50 Ohm transmission lines.



All high frequency traces are modeled as microstrip transmission lines. The calculation of the trace width is calculated using the following formula.

$$Z_o = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \times \ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

and based on the following layer setup:



where

ε_r = relative dielectric constant, nominally 5.0 for G-10 fibre-glass epoxy

t = thickness of the copper, fixed according to the weight of copper selected. For 1 oz copper, the thickness is 1.4 mil. This thickness can be ignored if w is great enough.

h1, h2, h3 = thickness of dielectric.

w = width of copper

The parameters h1, h2, and h3 can be specified. For example, if a 20 mil (including the copper thickness on both sides of the board) two layer core is selected, dielectric material that have the same relative dielectric constant can be added to both sides of the core to construct a 4 layer board.

Since all the controlled impedance traces are on the component side, only h1 is relevant in calculating the trace width. The calculation for the reference design is shown in the table below:

Note: The relative dielectric constant is specified to be between 4.8 and 5.4.

Parameter	Data			
ε_r	4.8	5.4	4.8	5.4
h (mil)	62	62	62	62
t (mil)	1.4	1.4	1.4	1.4
Zo (Ohm)	50	50	100	100
W (mil)	108.9	101.6	24.7	21.3

The value of the parameter h1 is chosen to be 62 mil. Since h1 is directly proportional to the width of the traces, a small h1 will result in the 100 Ohm traces being too thin to be accurately fabricated. Wider traces can be more precisely manufactured, but they take up too much board space. Therefore, the thickness of the board should be chosen so that the traces take up as little board space as possible yet still leaving enough margin to allow accurate fabrication. In the layout enclosed, the width of the 100 Ohm traces is 24 mil and that of the 50 Ohm traces is 104 mil.

Routing

High speed signal routing is based on design considerations as well as manufacturability. Several suggestions are listed below:

1. Turns and corners should be rounded to curves to avoid discontinuity in the signal path.

2. Allow at least 10 mil clearance among vias, traces, and pads to prevent shorts and reduce crosstalk. If possible, allow 20 mil or more clearance around vias as manufacturers may have minimum clearance requirements. For the traces that runs between pads of the 100 pin edge connector, clearance of 6 mil and trace width of 8 mil can be used. However, the number and lengths of such traces should be kept to a minimum.

3. The differential signal pairs should be of equal length so that both signals arrive at the inputs at the same time. They should also run parallel and close to one another for as long as possible so that noise will couple onto both lines and become common mode noise which is ignored by the differential inputs.

4. All power and ground traces should be made as wide as possible, up to 24 mil to provide low impedance paths for the supply current as well as to allow quick noise dissipation.

Termination

"Termination" applies to terminating a signal propagating down a transmission line to the characteristic impedance of line. If the line is not terminated to it's characteristic impedance, there will be reflections back down the line. The amount of reflection at the load (receiver) is given by the load reflection coefficient:

$$rL = (R_T - Zo)/(R_T + Zo)$$

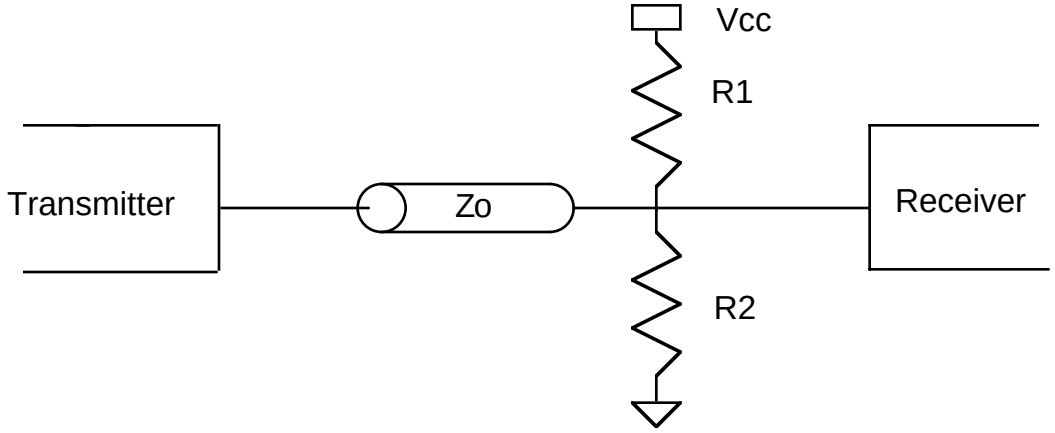
where R_T is the load impedance and **Zo** is the characteristic impedance of the line. The amount of reflection at the source (transmitter) is given by the source reflection coefficient:

$$rS = (R_S - Zo)/(R_S + Zo)$$

where R_S is the source impedance and **Zo** is the characteristic impedance of the line. The reflected signal propagates back and forth until the "ringing" dies out.

There are 4 basic types of terminations used for PECL (or ECL). They are open line termination, series termination, parallel termination, and Thévenin parallel termination. Since PECL (or ECL) signals only drive high, external biasing is needed to pull the PECL signal low. This biasing has to be incorporated into the termination scheme.

In the design, the Thévenin termination method has been used. The terminated lines are terminated to the characteristic impedance and sets the terminating (V_T) voltage. The Thévenin equivalent parallel termination is shown below:



The resistors R1 and R2 in parallel must equal Zo and the voltage at the input must pull the output of the transmitting gate to VBB Volts. Working out the equations for PECL +5 Volt supply for Vcc gives:

$$R2 = 2.5 * Zo$$

$$R1 = R2*2/3$$

Note that the above examples show only one of the differential inputs. With the Thévenin termination care must be taken so that the Vcc and grounds of the differential signals are taken in close proximity of each other or the noise on Vcc and ground will not be in common with each other.

Power and Ground Plane Noise Decoupling

Bypass capacitors can supply transient current and help filter out power and ground noise. They are placed as close to the pins as possible. Minimum of one 0.1 uF bypass capacitor per device is used. Wherever possible, one 0.1 uF bypass capacitor is placed at each power pin of each IC. For decoupling at the supply inputs, large electrolytic bypass capacitors (100 uF) are placed near the 5 volt power supply inputs.

It is also necessary to isolate power and ground planes supplying analog circuitry from the digital circuitry. The digital CMOS circuits have high immunity to external noise (approximately 0.3 * Vcc) whereas a small amount of external noise coupled into the analog circuits can be devastating since the analog circuits operate on low voltage swings (600 mVolts for the PECL inputs) compared to the large (5 Volt) voltage swings of the CMOS inputs. The CMOS circuits can also generate a lot of switching noise, especially when a large number of circuits are running synchronously all timed to the same system clock.

If the analog power and grounds are not isolated from each other it is unlikely that the board will be able to meet the 0.01 U.I. rms. jitter specified by Bellcore. Therefore, it is necessary to isolate the digital from the analog, otherwise the analog performance can be degraded to a point of non-conformance.

It is also necessary to isolate the transmit analog circuitry from the receive analog circuitry. Any noise on the receive analog power and ground or on the receive inputs will degrade jitter tolerance and add jitter to the recovered clock. It is also important to keep the analog optical transceiver receive path in common with the receive portion of the VSC8110, especially the grounds.

On the transmit side the, 622 MHz clock is synthesized from a 19.44 MHz reference clock. Any added noise on the power or ground inputs impacts the resulting synthesized 622 MHz clock. This added noise will result in an increased intrinsic jitter at the transmitter. The power and ground of the transmit portion of the HP HFBR-5207 optical transceiver should be in common with the analog transmit power and ground of the VSC8110 to reduce ground plane imbalance.

Since only one ground layer and one power layer is normally available, the transmit, receive, and digital power and grounds can be isolated by channels cut into the respective planes. The power and grounds should be brought from a quiet part of the board, usually where the power and grounds enter the board. Ferrite beads can also be used on the receive and transmit analog powers to prevent digital noise from

entering analog circuits of the 19.44 MHz oscillator, VSC8110 and the optical transceiver.

Ferrite beads are mainly used on power rails to pass DC current but to attenuate the higher frequency noise that is created by other sources. The impedance of Ferrite beads increases with frequency. At DC the ferrite bead is like a short but at higher frequency the impedance of a ferrite bead can increase to over 100 ohms (depending on the bead and frequency). Ferrite beads attenuate high frequency noise from the power supply from getting into a circuit, but they also stop high frequency noise from leaving the circuit. It is important, therefore, to use proper bypass decoupling when using ferrite beads.

Ferrite beads should be avoided on CMOS I/O power pins as the high current switching of the CMOS circuits causes a $\Delta I/\Delta t$ noise to be introduced into the power rail. Ferrite beads should also be avoided on the ground bus as this inhibits the return currents.

To reduce digital circuit switching noise, it is important to decouple every digital power pin of all devices so that the switching currents can be satisfied and thereby reduce the amount of noise introduced into the power plane.

APPENDIX1: JITTER TEST RESULTS

This appendix includes results obtained from jitter measurements performed on the S/UNI-622 reference design board using various optical modules. *These results are for reference only, and were obtained in the absence of appropriate standards at the time of execution. Compliance to future standards should be checked using these results.*

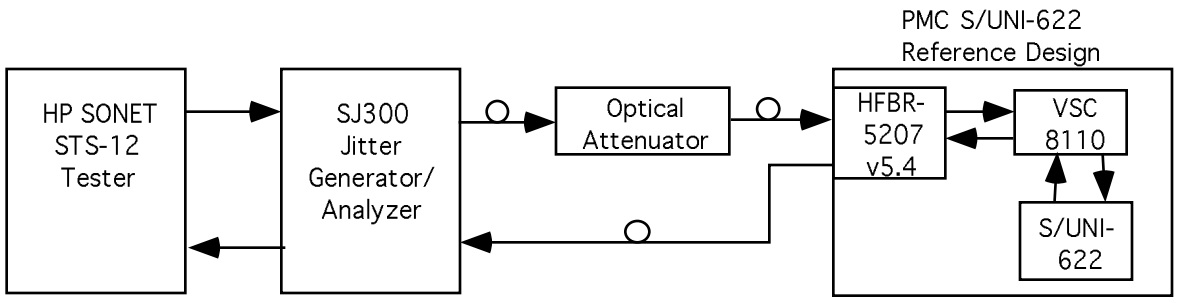
1. HP HFBR-2507 version 5.4

Jitter Tolerance

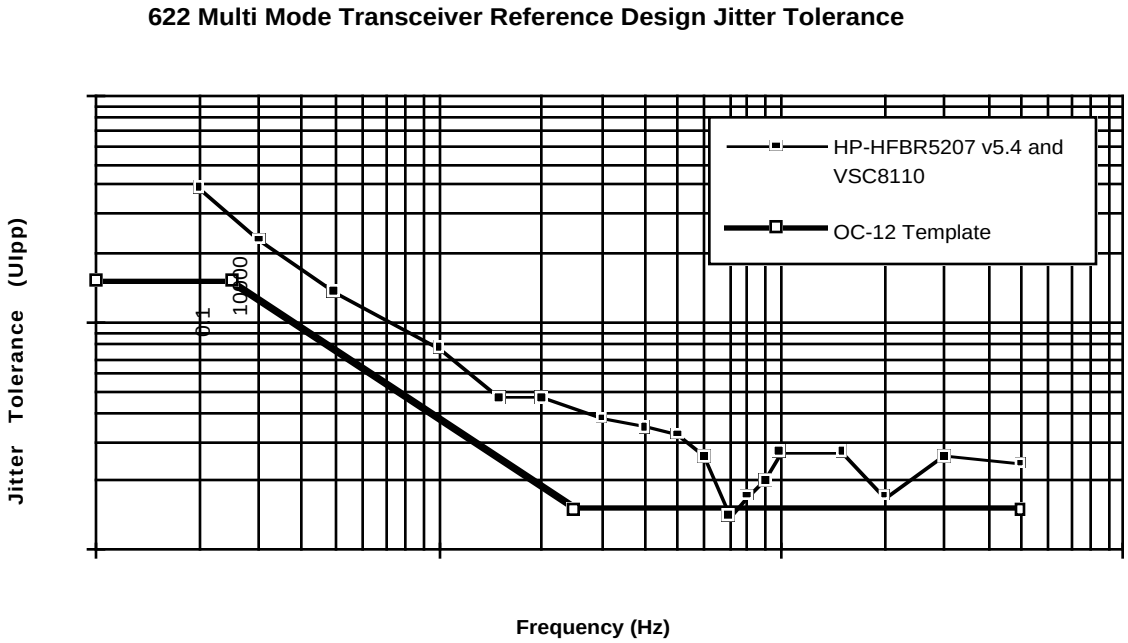
Measured using the S/UNI-622 reference design board, with the following components:
HP HFBR-2507 622 multimode optics with CRU, version 5.4
Vitesse VSC8110 SIPO
S/UNI-622 to monitor the bit error rate

Method:
- HP STS-12 SONET Tester used to generate and receive STS-12 electrical serial signal, with PRBS-23 data in one of the STS-3c's (HP does not have STS-12c mode).
- This goes into the SJ300 Jitter Analyzer, which converts the signal into optical form and adds the jitter for tolerance testing.
- Optical attenuator provides the necessary attenuation. Attenuation was added till the Section BIP error rate was about $1x10^{-10}$ (monitored at the tester by looking at FEBE's sent back by the S/UNI-622 to the Tester). Then the attenuation was reduced by 1 dB for the actual jitter tolerance test.

Setup:



Results:



Attenuation = 17.4 dB
Actual optical power at optical receiver = -28.2 dB

Conclusion: Jitter tolerance failed at 700kHz, 0.14UI.

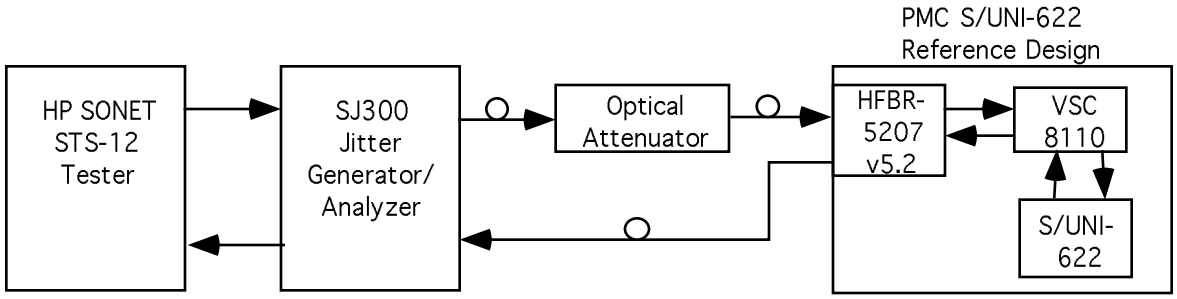
2. HP HFBR-5207 version 5.2

Jitter Tolerance

Measured using the S/UNI-622 reference design board, with the following components:
HP HFBR-5207 622 multimode optics with CRU, version 5.2
Vitesse VSC8110 SIPO
S/UNI-622 to monitor the bit error rate

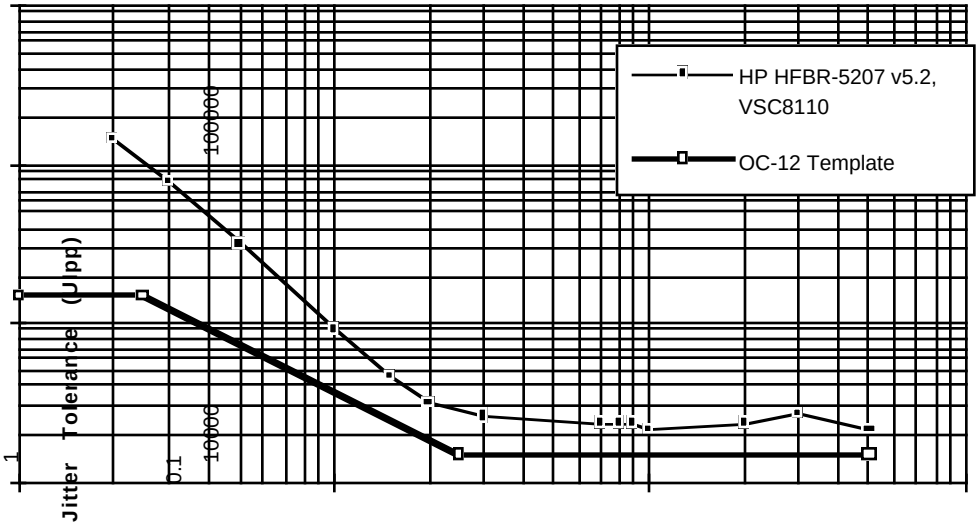
Method:
Same as with HP HFBR-5207 version 5.4.

Setup:



Results:

622 Multimode Reference Design Jitter Tolerance



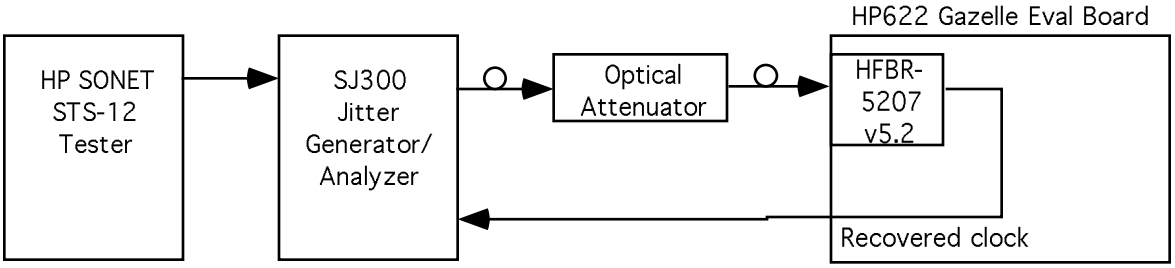
Attenuation = 18.7 dB
Actual optical power at optical receiver = -27.7 dB

Conclusion: Jitter tolerance passed with at least 0.06UI margin.

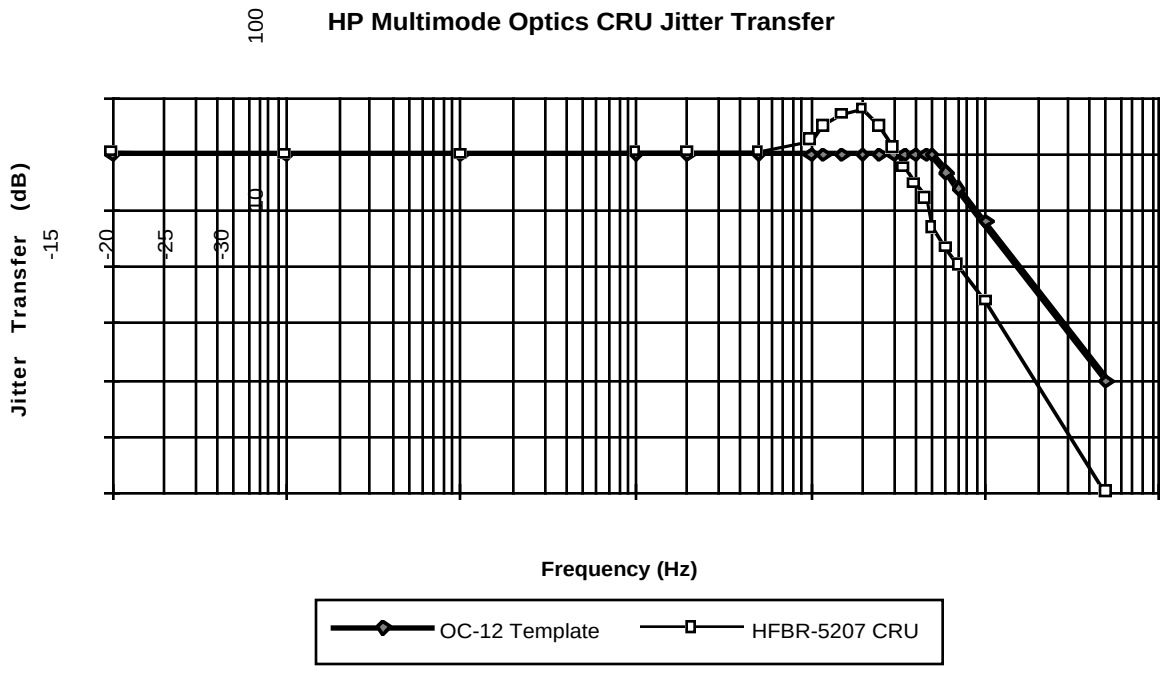
Jitter Transfer of CRU

Method:
- HP STS-12 SONET Tester used to generate and receive STS-12 electrical serial signal, with PRBS-23 data in one of the STS-3c's (HP does not have STS-12c mode).
- This goes into the SJ300 Jitter Analyzer, which converts the signal into optical form and adds the jitter for transfer testing.
- Optical attenuator used to set the same attenuation as in jitter tolerance test (17.7dB).
- The recovered clock from the optics is fed back into the SJ300

Setup:



Results:



Conclusion: Jitter Transfer failed. Peaking of about 4dB at 110kHz observed.

Jitter Generation of VSC8110 CSU

Method:
- Optical signal from HFBR-5207 measured directly by SJ300
- 2 different oscillator frequencies used to feed VSC8110 CSU
- RMS jitter measured with 12kHz high pass filter
- Peak-to-peak jitter measured with 10Hz high pass filter

Results:

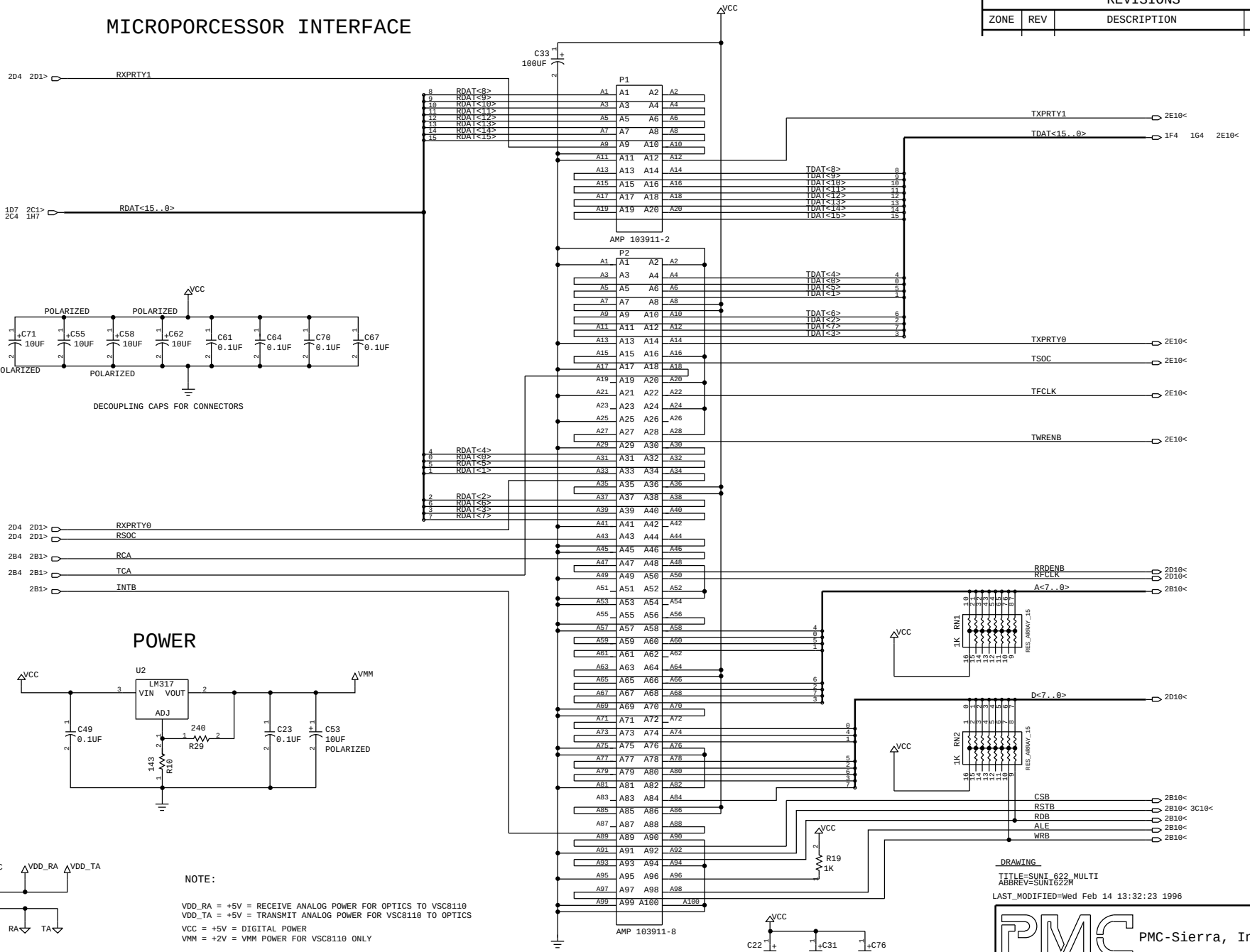
VDD (Volts)	Ref. Frequency (MHz)	RMS Jitter (UI)	Peak-to-Peak JItter (UI)
4.7	19.44	0.009	0.14
5.0		0.009	0.14
5.3		0.008	0.13
4.7	51.84	0.008	0.12
5.0		0.008	0.12
5.3		0.009	0.11

Conclusions: According to Bellcore GR-253, Dec 94, the maximum RMS jitter generated should be 0.01UI, and the maximum peak-to-peak jitter generated should be 0.10UI. The measured RMS jitter passed but the measured peak-to-peak jitter failed.

APPENDIX2: SCHEMATICS

MICROPORCESSOR INTERFACE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DECOUPLING CAPS FOR CONNECTORS

POWER

NOTE:

VDD_RA = +5V = RECEIVE ANALOG POWER FOR OPTICS TO VSC8110
VDD_TA = +5V = TRANSMIT ANALOG POWER FOR VSC8110 TO OPTICS

VCC = +5V = DIGITAL POWER
VMM = +2V = VMM POWER FOR VSC8110 ONLY

GND_RA = 0V = RECEIVE ANALOG GROUND FOR OPTICS TO VSC8110
GND_TA = 0V = TRANSMIT ANALOG GROUND FOR VSC8110 TO OPTICS
GND = 0V = DIGITAL GROUND

DRAWING

TITLE=SUNI_622_MULTI
ABBREV=SUNI622M

LAST_MODIFIED=Wed Feb 14 13:32:23 1996

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-950860	ISSUE: ISSUE 2
TITLE: PM5955-3: S/UNI_622 ATM REF DESIGN WITH MULTIMODE OPTICS	DATE: FEB 14, 1996
ENGINEER: P. CHOHAN	PAGE:1 OF 4

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

S/UNI 622

R18 & R13 PLACE CLOSE TO U13 S/UNI 622 PIN

PLACE AT FAR END

DECOUPLING CAPS FOR SUNI-622 +5V & 74HC541

NOTE: RN7, RN8 RN9 ARE SHORT CIRCUIT ON PCB

NOTE: FOR LAYOUT PURPOSE ONLY

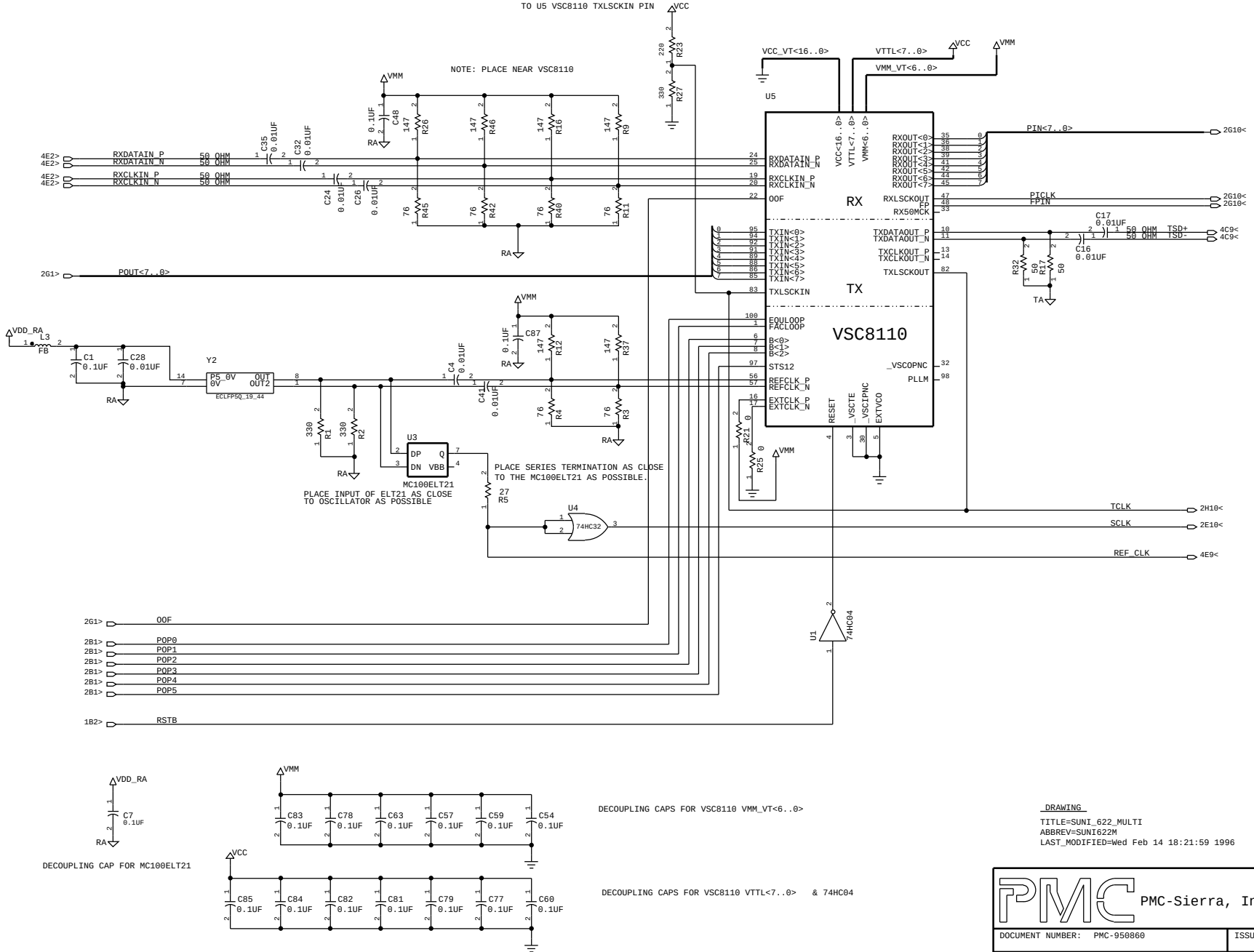
DRAWING
TITLE=SUNI 622 MULTI
ABSREV=SUNI622M
LAST_MODIFIED=Wed Feb 14 13:33:01 1996

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-950860	ISSUE: ISSUE 2
TITLE: PM5955-3: S/UNI_622 ATM REE DESIGN WITH MULTIMODE OPTICS	DATE: FEB 14, 1996
ENGINEER: P. CHOHAN	PAGE:2 OF 4

MUX/DMUX

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



DRAWING

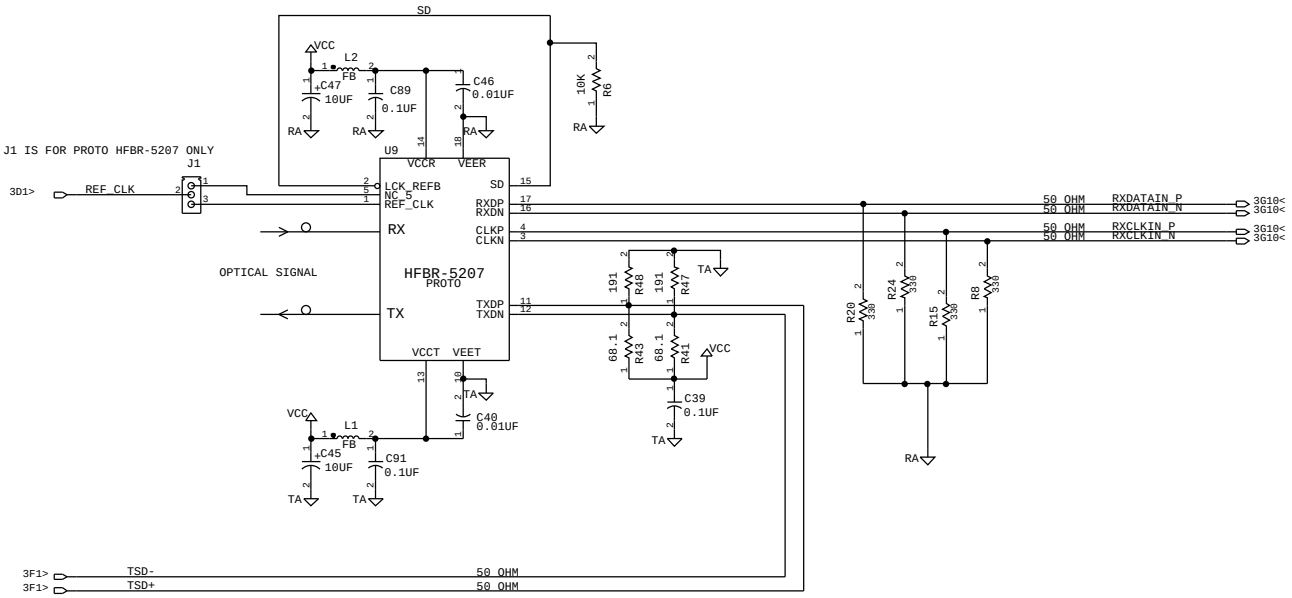
TITLE=SUNI_622_MULTI
ABBREV=SUNI622M
LAST_MODIFIED=Wed Feb 14 18:21:59 1996

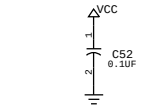
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-950860	ISSUE: ISSUE 2
TITLE: PM5955-3: S/UNI_622 ATM REF DESIGN WITH MULTIMODE OPTICS	DATE: FEB 14, 1996
ENGINEER: P. CHOHAN	PAGE:3 OF 4

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

OPTICAL INTERFACE





DECOUPLING CAPS FOR 74HC32

DRAWING

TITLE=SUNI_622_MULTI
ABBREV=SUNI622M
LAST_MODIFIED=Wed Feb 14 18:20:17 1996

PMC-Sierra, Inc.

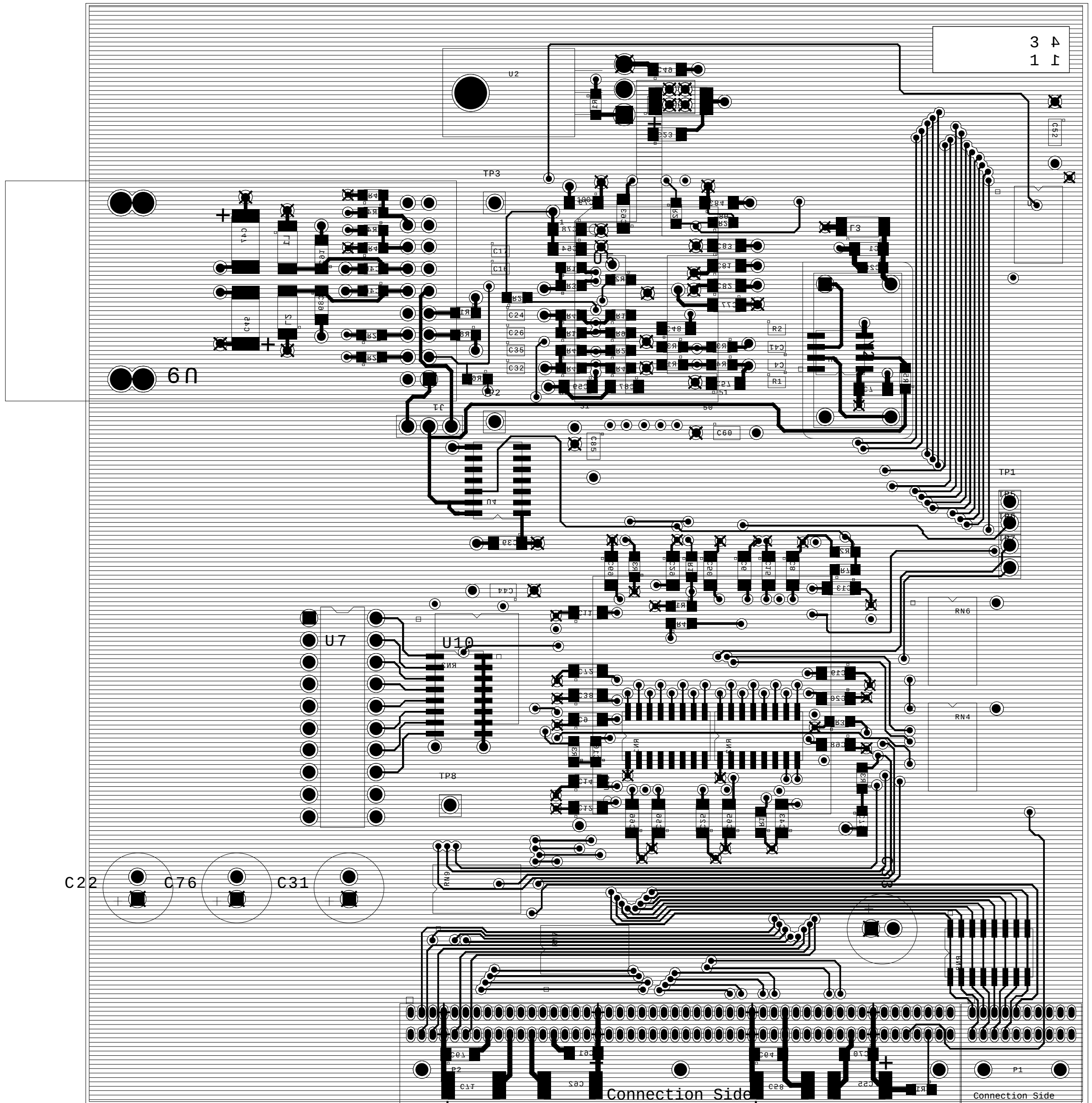
DOCUMENT NUMBER: PMC-950860	ISSUE: ISSUE 2
TITLE: PM5955-3: S/UNI_622 ATM REF DESIGN WITH MULTIMODE OPTICS	DATE: FEB 14, 1996
ENGINEER: P. CHOHAN	PAGE: 4 OF 4

BOTTOM_LAYER

PMC-SIERRA S/UNI-622 ATM RD WITH MULTIMODE OPTICS REV.2.0 1995

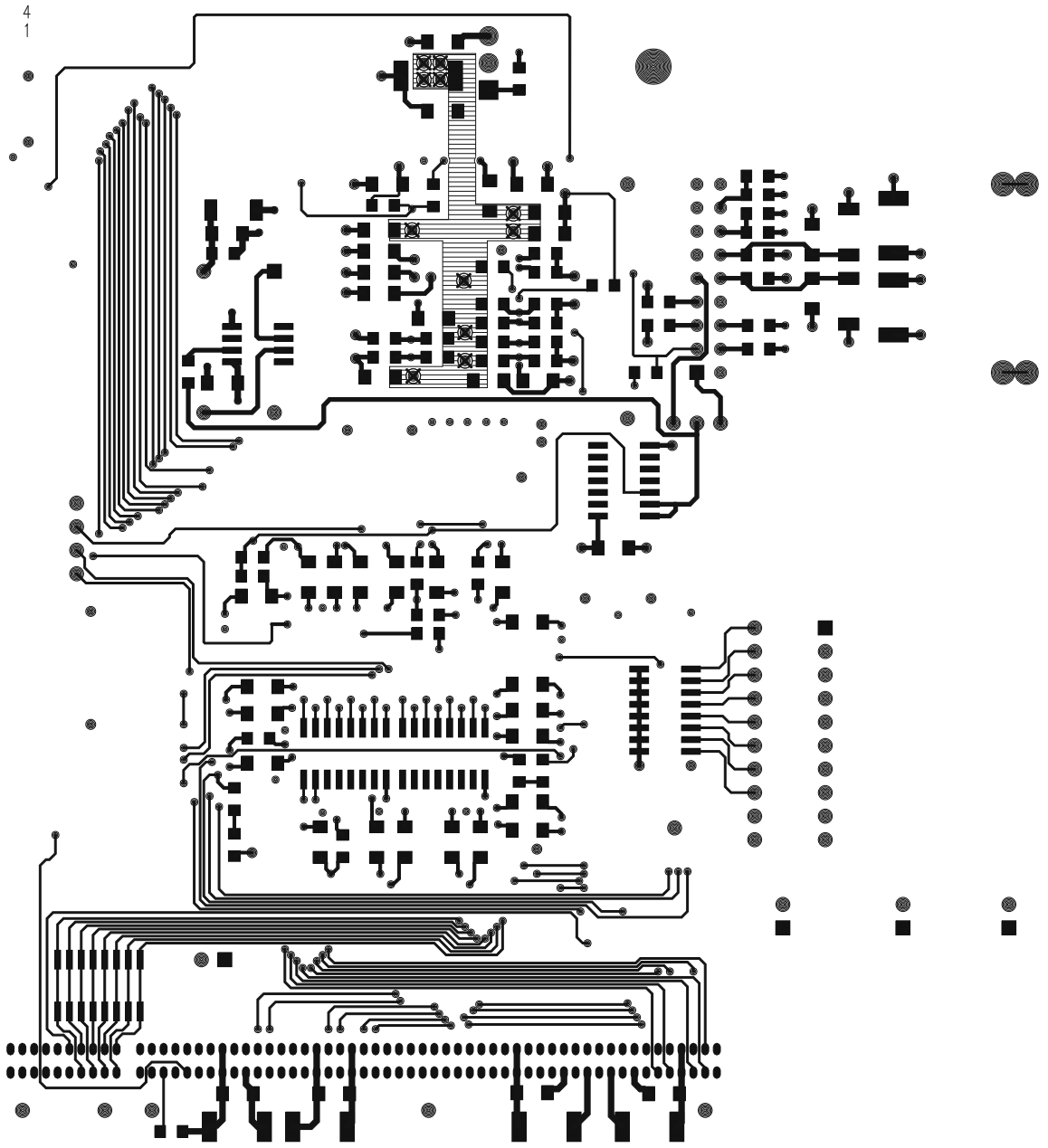
RES_DES TOP VCC_PLANE

RES_DES BOTTOM
BOTTOM_LAYER

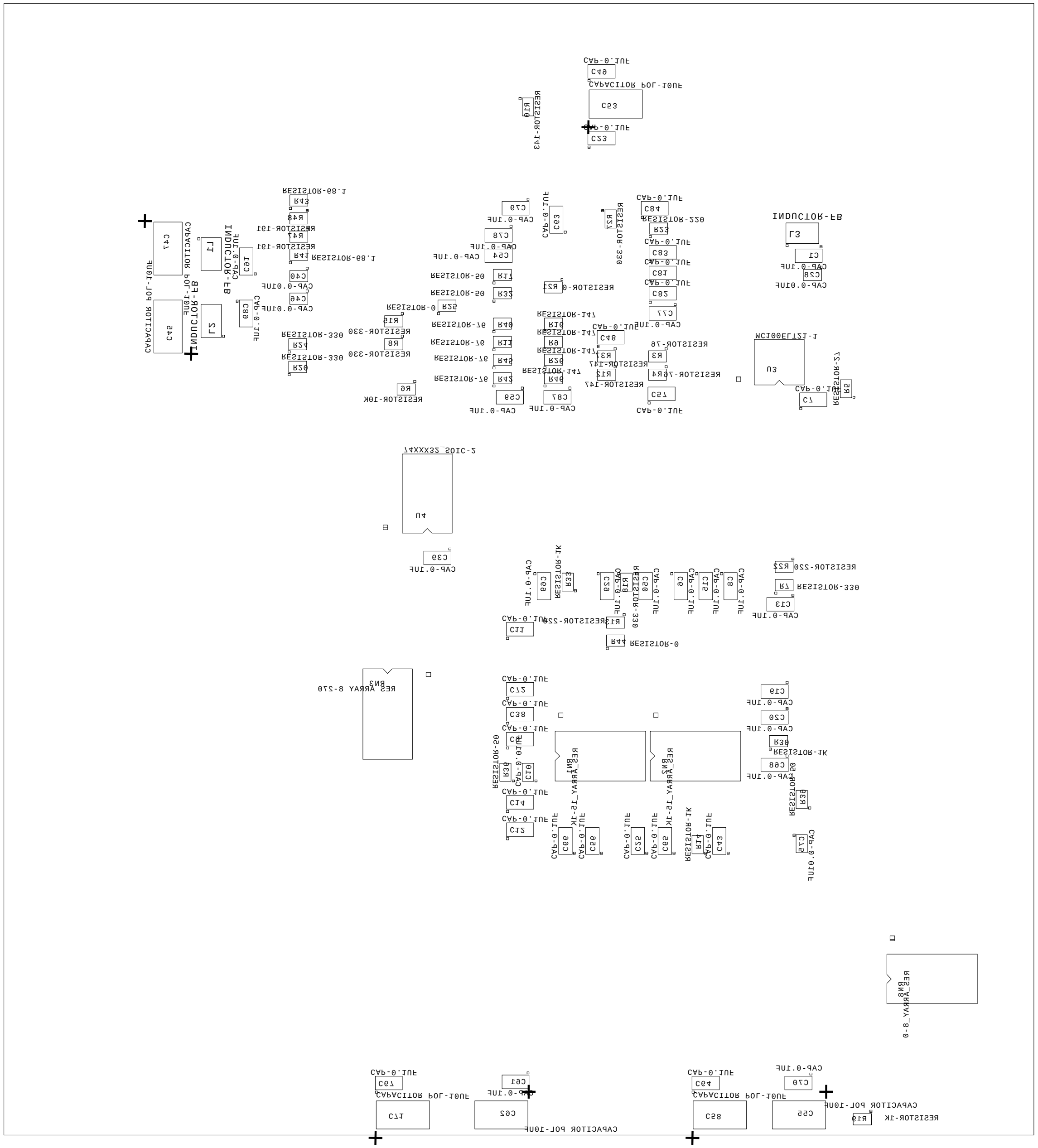


PMC-SIERRA S/UNI-622 ATM RD WITH MULTIMODE OPTICS REV 2.0 1995

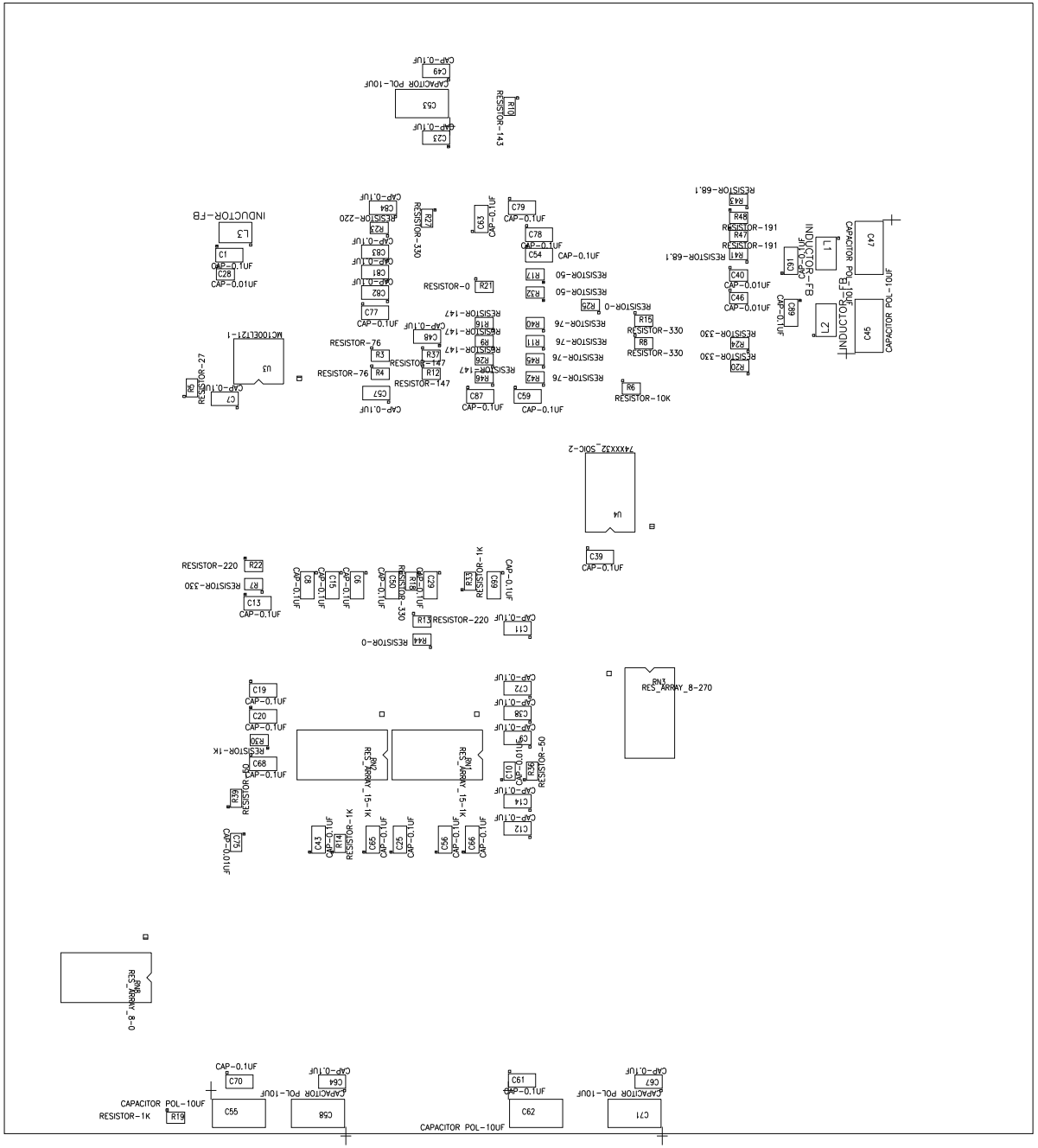
BOTTOM_LAYER



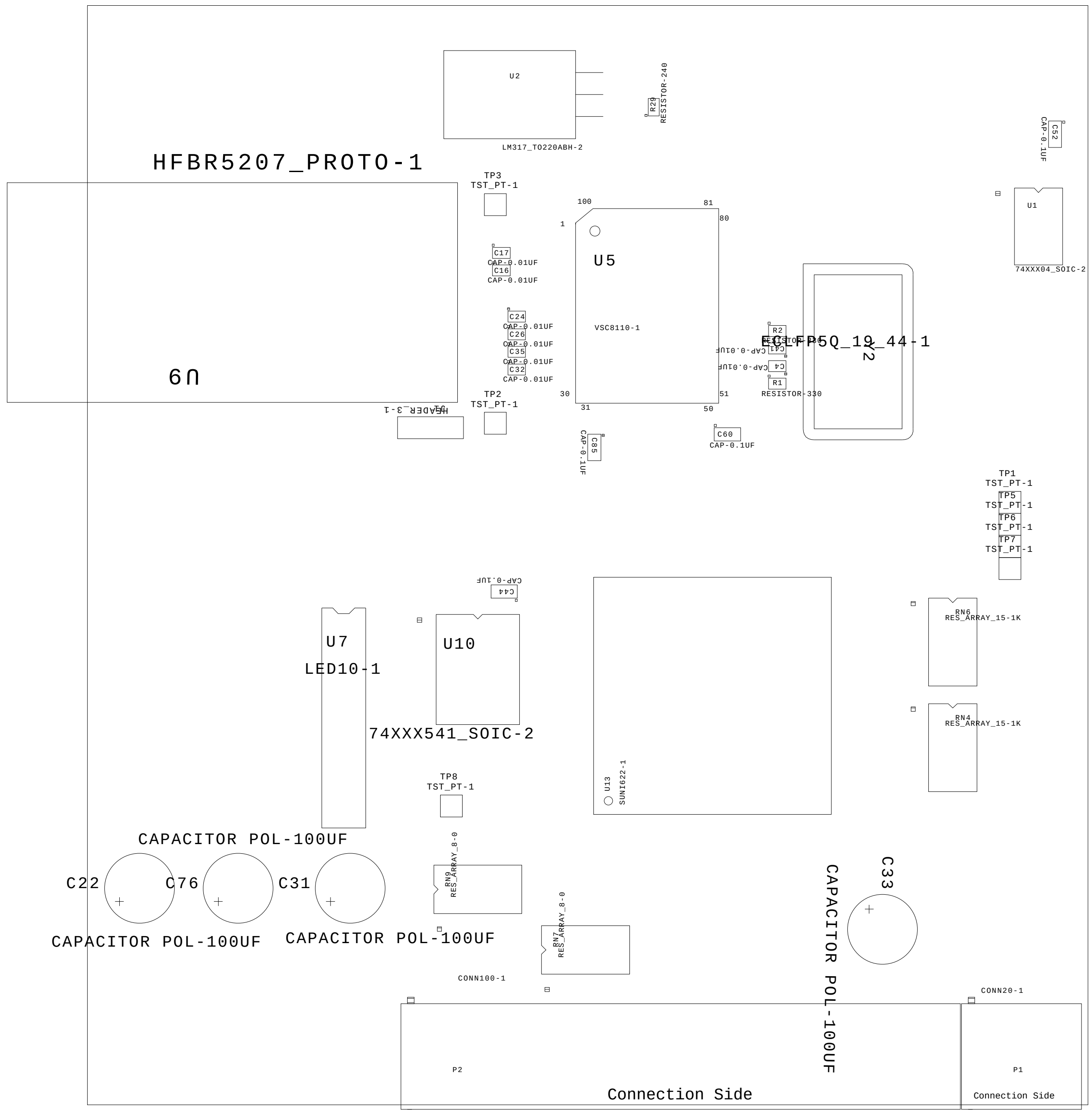
RES_DES BOTTOM



PMC-SIERRA S/UNI-622 ATM RD WITH MULTIMODE OPTICS REV.2.0 1995

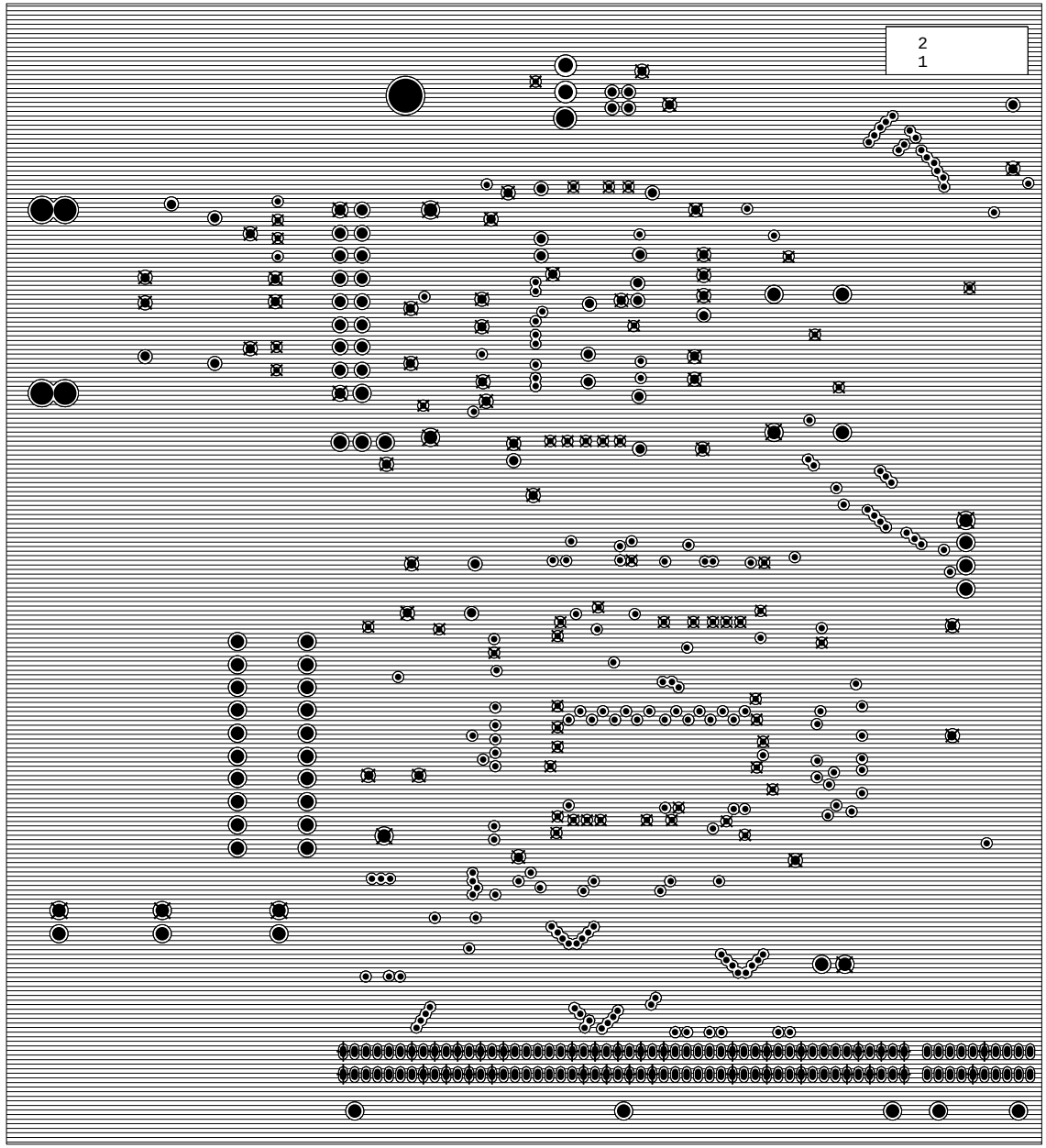


RES_DES TOP

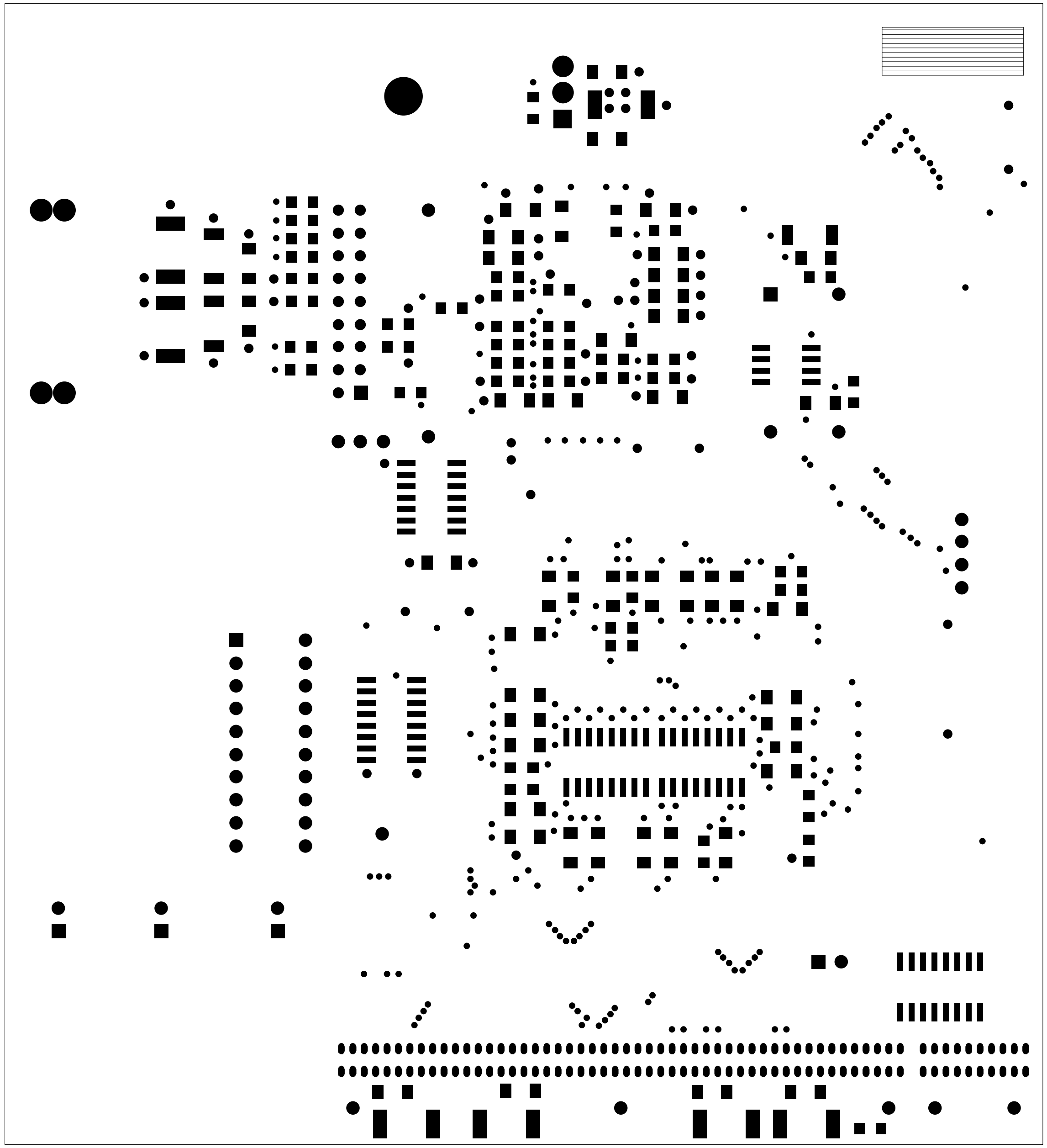


PMC-SIERRA S/UNI-622 ATM RD WITH MULTIMODE OPTICS REV.2.0 1995

GND_PLANE

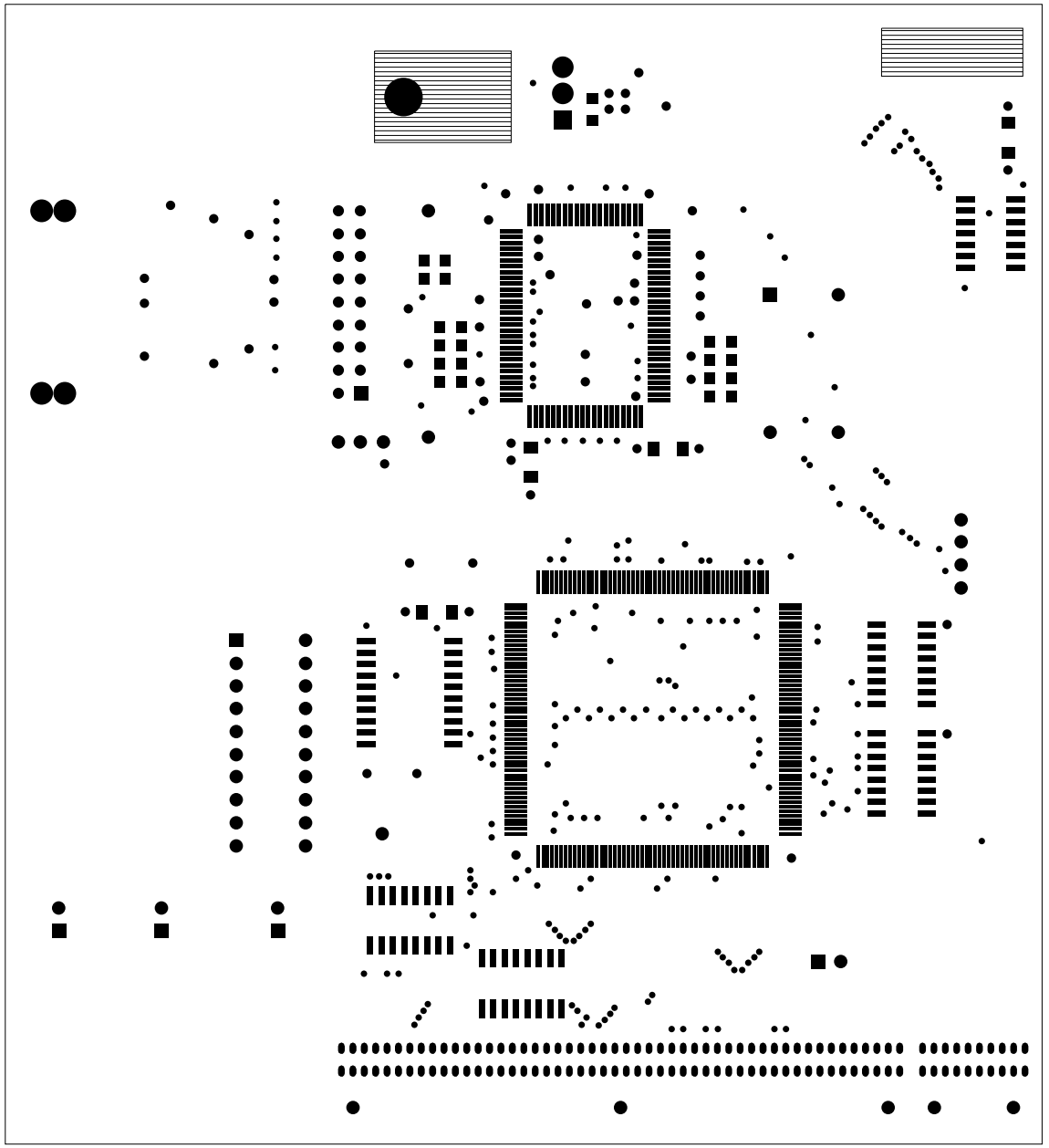


SOLDER_MASK BOTTOM



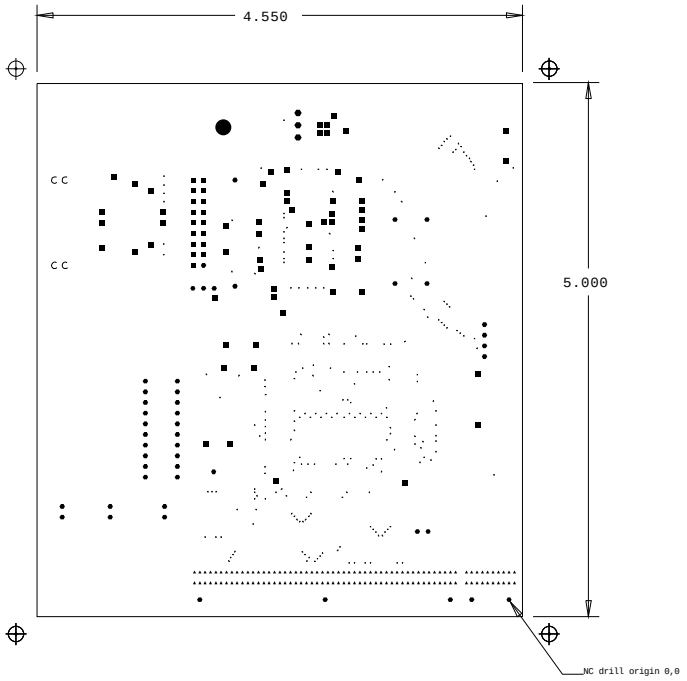
PMC-SIERRA S/UNI-622 ATM RD WITH MULTIMODE OPTICS REV.2.0 1995

SOLDER_MASK TOP



PMC-SIERRA S/UNI_622 ATM RD WITH MULTIMODE OPTICS REV.2.0 1995

REVISIONS					
REV	DESCRIPTION	DATE YY	MM	DD	APPROVED
1.0	NCDRILL_FIGURE	96	01	16	
1.0	MECHANICAL DRAWING	96	01	16	



PMC-SIERRA S/UNI-622 ATM REFERENCE DESIGN WITH
MULTIMODE OPTICS REV.2.0 1995

Board Material Details

	Material	Layer Type	Etch Name	Film type	Thickness	Dielectric Constant
#	COPPER	CONDUCTOR	TOP	POSITIVE	1.44 mil	------
	FR-4	DIELECTRIC	------	------	10 mil	4.2
	COPPER	CONDUCTOR	GND_PLANE	POSITIVE	2.88 mil	------
	FR-4	DIELECTRIC	------	------	33.4 mil	4.2
	COPPER	CONDUCTOR	VCC_PLANE	POSITIVE	2.88 mil	------
	FR-4	DIELECTRIC	------	------	10 mil	4.2
#	COPPER	CONDUCTOR	BOTTOM	POSITIVE	1.44 mil	------

Note: 50 ohm controlled impedence traces with trace width of 17 mil are on Top and Bottom layers.

ARTWORK FILM

TOP LAYER
GROUND PLANE
VCC PLANE
BOTTOM LAYER
SILKSCREEN TOP
SILKSCREEN BOTTOM
SOLDER MASK TOP
SOLDER MASK BOTTOM
MECH. DRAWING

Hole Chart

/ FIGURE / HOLESIZE / QTY /

.	15.000-P	237
.	22.000-P	120
■	25.000-P	62
■	32.000-P	17
●	36.000-P	48
●	55.000-P	3
C	79.000-P	4
●	150.000-P	1

Note: P = Plated
N = Non-Plated

Notes:

1. Copper thickness is 2 oz. on vcc_plane & gnd_plane, 1 oz. on all others layers.
2. Total thickness of board shall be 62 mil +/- 7 mil.
3. The outline dimension are specified on this drawing.
4. Material: See board material details above.
5. All holes shall have 1 mil mimimum copper wall thickness.
6. Dielectric constant: See board material details above.
7. Silk screen shall be screened in monoconductive white based ink.
8. Maximum warp and twist of finished PCB shall not exceed 0.010 in./in. per IPC-D-300.
9. All material comprising the PCB must be recongized by UL to the 94V-0 rating.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
2 PL DECIMALS +/- .03
3 PL DECIMALS +/- .005
ANGLES +
FRACTIONS +

		DATE YY	MM	DD
DRAWN	S. SIU	96	01	16
CHECKED				
ENGINEER				
APPROVED				

PMC-Sierra, Inc.

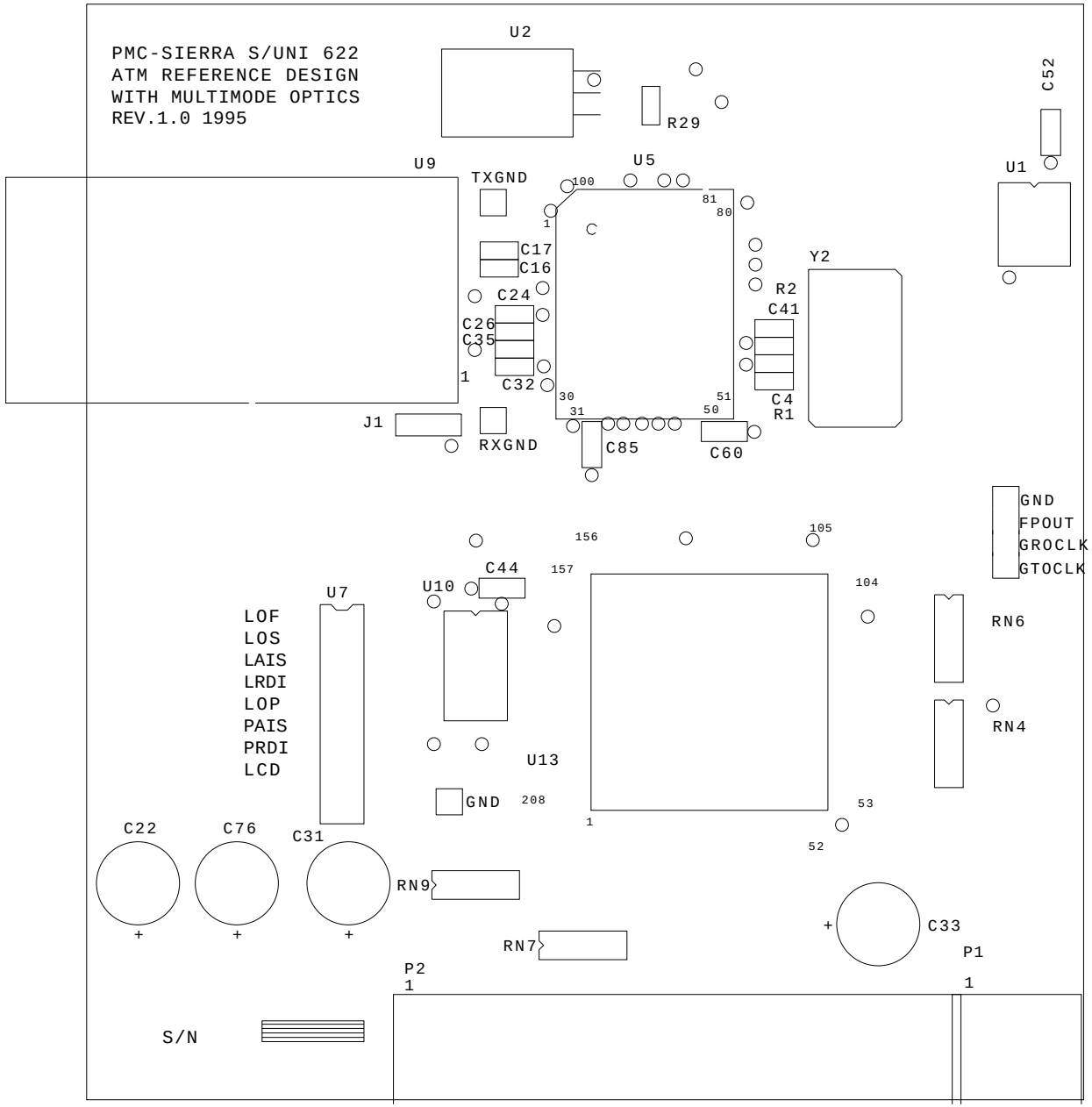
8501 Commerce Court, Burnaby B.C.
Canada, V5A 4A3
Tel: 604 668 7300 Fax: 604 668 7301

SIZE	FSCM NO	DWG NO
B		

SCALE	NTS	SHEET 1 OF 1

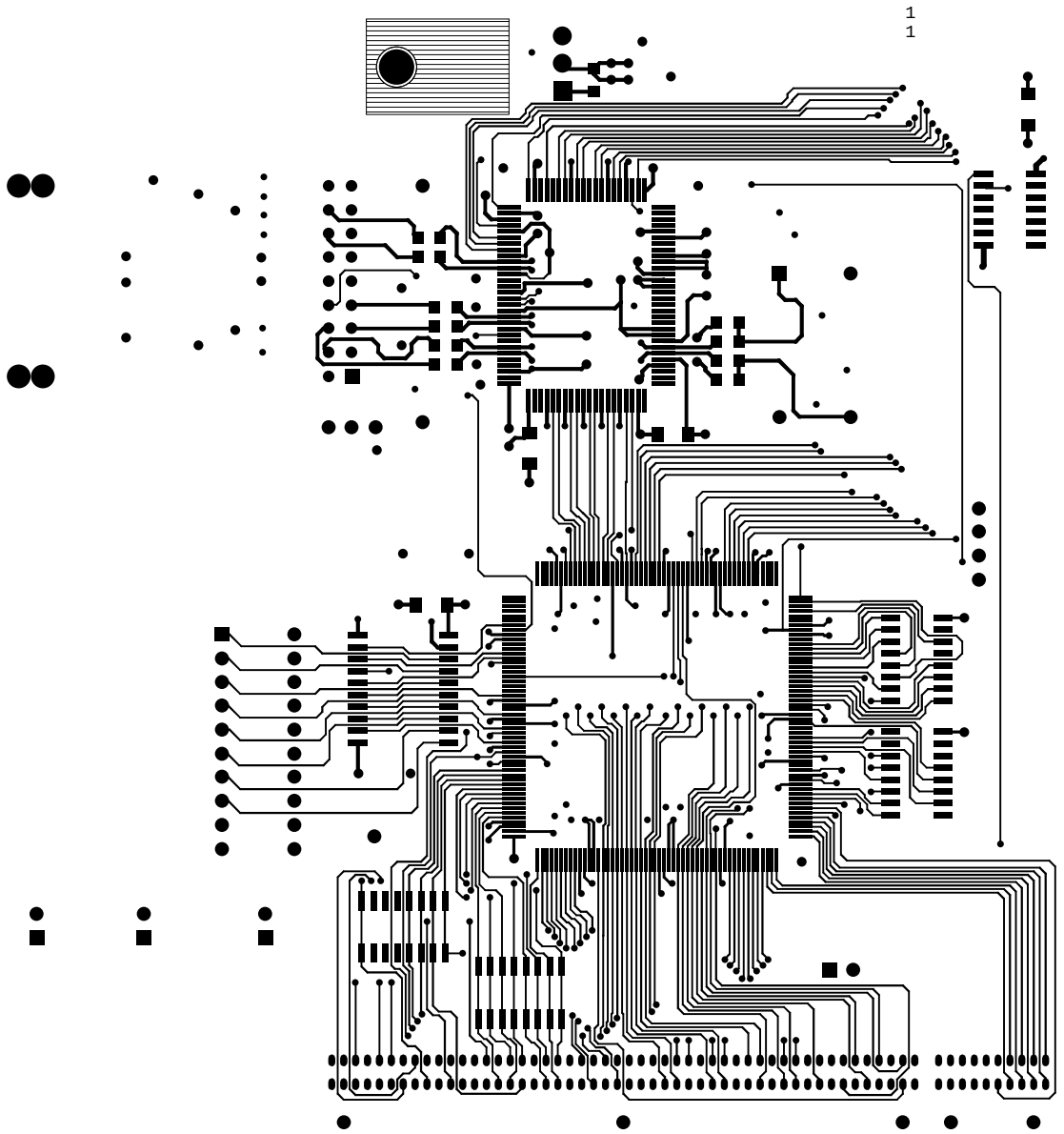
SILK_SCREEN BOTTOM
PMC-SIERRA S/UNI-622 ATM RD WITH MULTIMODE OPTICS REV.2.0 1995

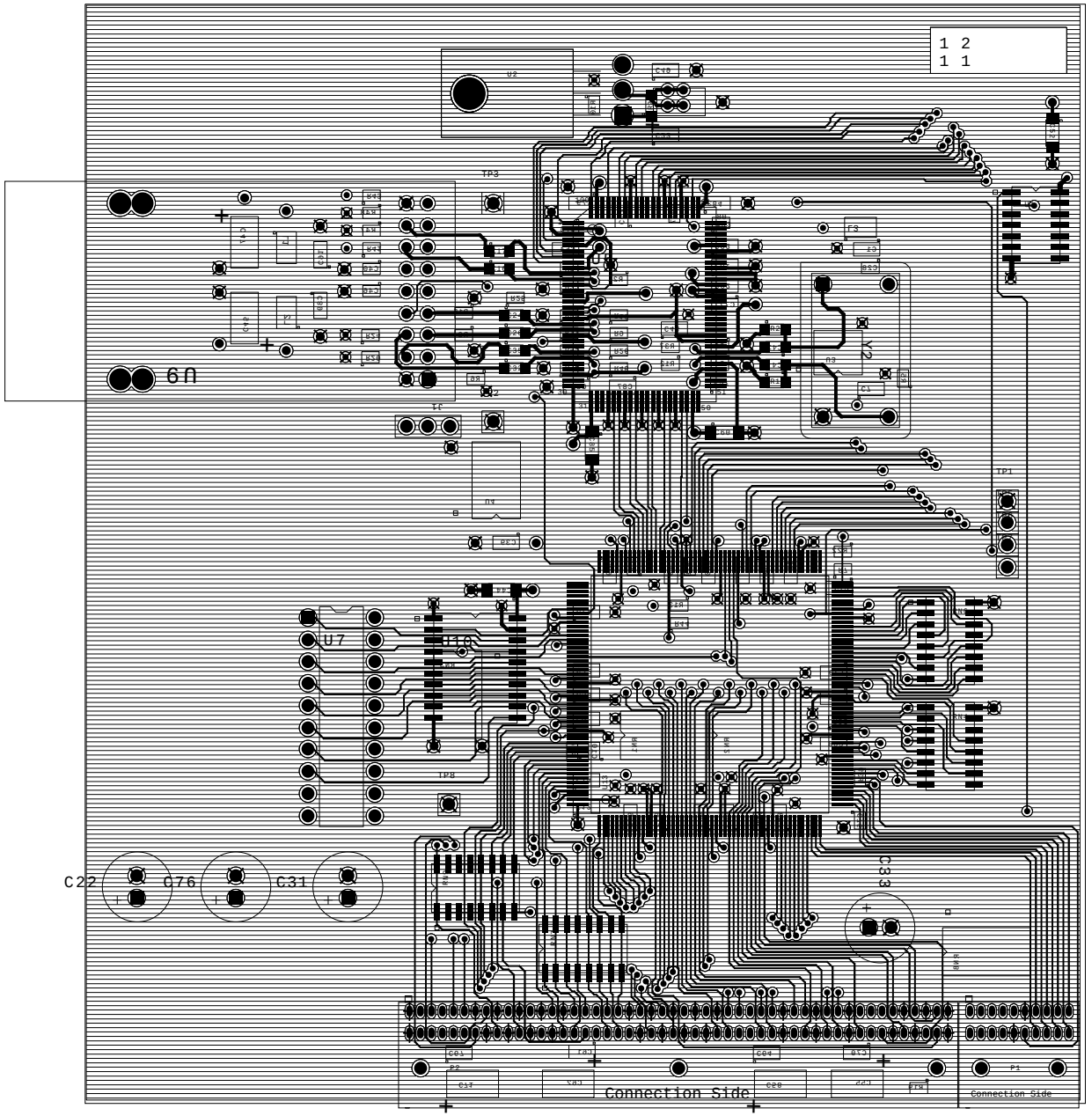
SILK_SCREEN TOP



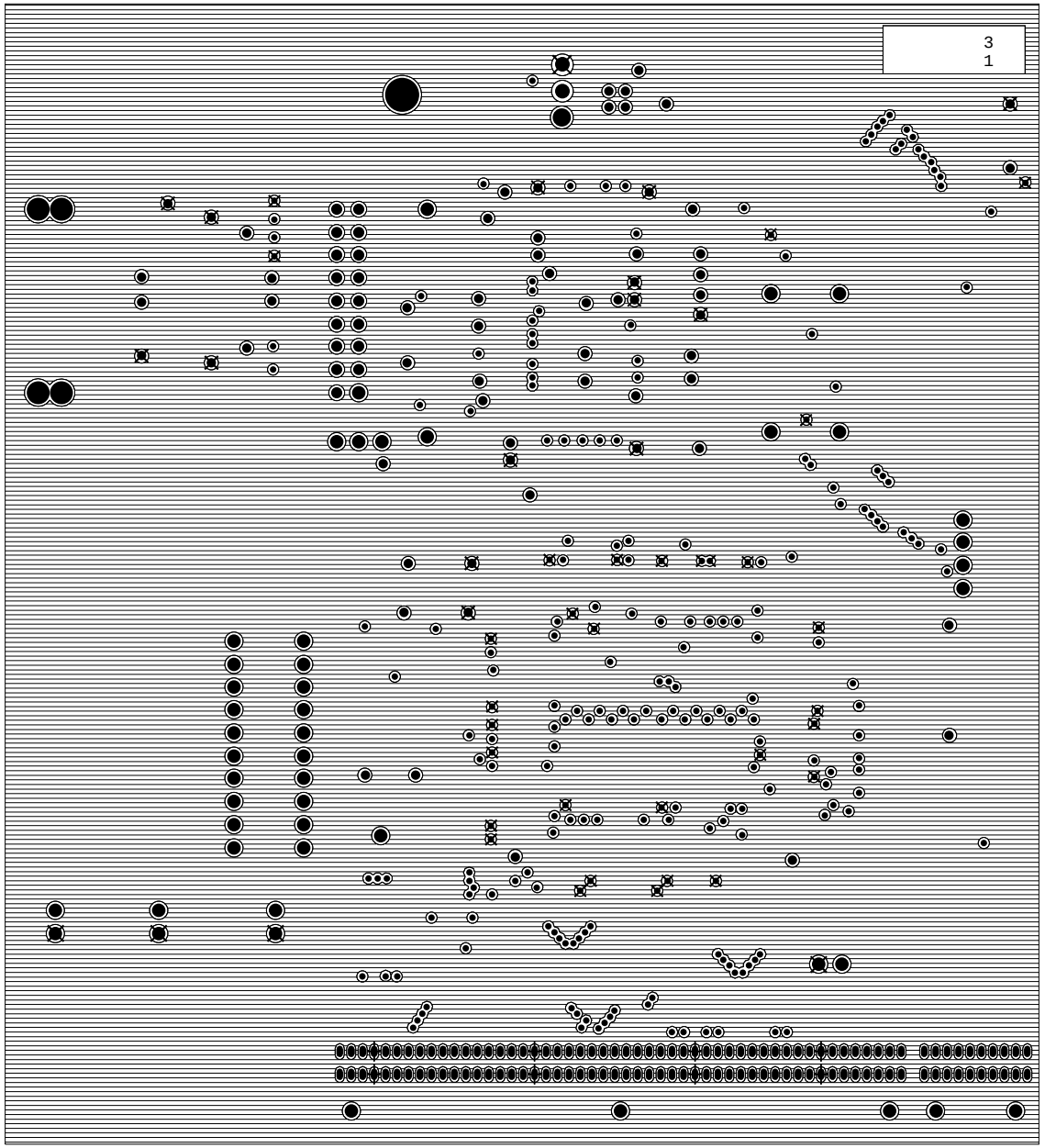
PMC-SIERRA S/UNI-622 ATM RD WITH MULTIMODE OPTICS REV.2.0 1995

TOP LAYER




1 2
1 1
U2
TP3
J2
J1
TP1
U7
TP8
C22
C76
C31
C33
Connection Side
Connection Side

VCC_PLANE



NOTES

Contact us for applications support:

FAX: (604) 415-6206

PHONE: (604) 415-6000

Email: apps@pmc-sierra.bc.ca

Website: http://www.pmc-sierra.com

PMC-950860(R3) Issue date: October 11, 1996.