PM7375
LASAR™

TECHNICAL OVERVIEW

Preliminary Information

Issue 1, June 26, 1995

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OVERVIEW

The PM7375 LASAR™ is a highly integrated semiconductor device that is ideally suited for ATM Network Interface Cards (NICs). The LASAR combines a Physical Layer Processor, ATM Layer and AAL-5 SAR Processor and a PCI DMA Controller on a single chip to simplify the design, programming and manufacturing of ATM adapters. The major functional blocks of the LASAR are illustrated in Figure 1.

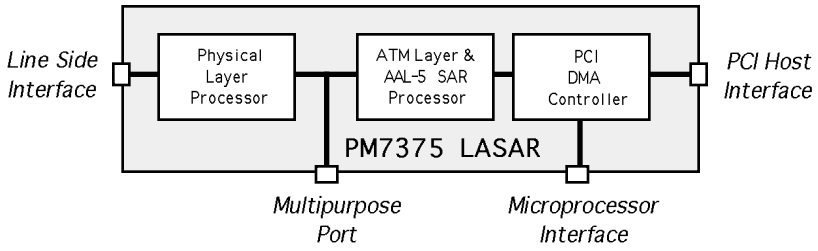

Figure 1. LASAR Major Functional Blocks.

The Physical Layer (PHY) Processor incorporates the industry standard PMC PM5346 S/UNI-LITE. It provides SONET and SDH interfaces at either STS-3c/STM-1 (155.52 Mbps) or STS-1 (51.84 Mbps) rates and supports control registers and signal pins that are compatible with those of S/UNI-LITE's. On the line side, the PHY Processor supports a direct interface to either optical or twisted pair cabling and provides on-chip clock recovery and clock synthesis units that are expected to be compliant with Bellcore TR-NWT-000253 Issue 2 and ITU-T G.958 jitter requirements.

The AAL-5 SAR Processor supports the simultaneous segmentation and reassembly of 128 open virtual circuits (VCs). The connection parameters for the 128 transmit and 128 receive VCs are maintained in an internal table to simplify the design of the NIC and to sustain a high data throughput rate. For traffic shaping, the LASAR implements a leaky bucket peak cell rate (PCR) enforcement using eight programmable rate queues arranged as a set of four high priority queues and a set of four low priority queues. The PCR can be specified on a per VC basis by associating a transmit VC with one of the eight rate queues and by selecting whether to use 100%, 50%, or 25% of the peak rate provided by the queue. The LASAR also supports the enforcement of sustainable cell rate (SCR) using a token generation mechanism. The ATM Forum is currently defining a new traffic management service called the Available Bit Rate (ABR). PMC-Sierra is participating in the standardization process and will update the LASAR's traffic shaper to support ABR when the standard is finalized.

The LASAR provides a 32 bit and 33 MHz Peripheral Component Interconnect (PCI) interface that is compliant with the PCI Local Bus Specifications Version 2.0. PCI is an open bus interface standard that is rapidly gaining widespread acceptance by the computer industry today. PCI's high bandwidth and low bus latency features enable packets to be segmented and reassembled in the host memory thereby eliminating the need for expensive local packet memory. The LASAR's PCI DMA Controller supports both bus-master and bus-slave modes. In bus-master mode, the PCI DMA Controller can access the host memory independent of the host processor. In bus-slave mode, the host processor can access LASAR's registers and communicate with the optional microprocessor via a mailbox mechanism provided by the PCI DMA Controller. The LASAR provides an efficient DMA controller to manage the transfer of packets between LASAR's SAR

engine and the host memory. The transmit and receive DMA channels are described in the Detailed Description section.

The LASAR conforms to ATM Forum User-Network Interface (UNI) Specification Version 3.1, Bellcore Standard TA-NWT-001113 and ITU-T Recommendations I.432 and I.363. It is implemented in low power, 0.6 micron, +5 Volt CMOS technology. It has TTL and pseudo ECL (PECL) compatible inputs and outputs and is packaged in a 208 pin PQFP package.

APPLICATION EXAMPLES

The LASAR is not only a highly integrated device but also a flexible device that can be configured to suit many application needs. This section highlights how the LASAR can be used in an ATM adapter, in conjunction with an external physical layer processor, and in multimedia applications.

ATM Network Interface Card

An ATM NIC implements PHY, ATM, and AAL protocol layers such that an end system can communicate with an ATM switch. Figure 2 illustrates a generic ATM NIC architecture and identifies the functional blocks that must be implemented and integrated to form the basis of the User-Network Interface.

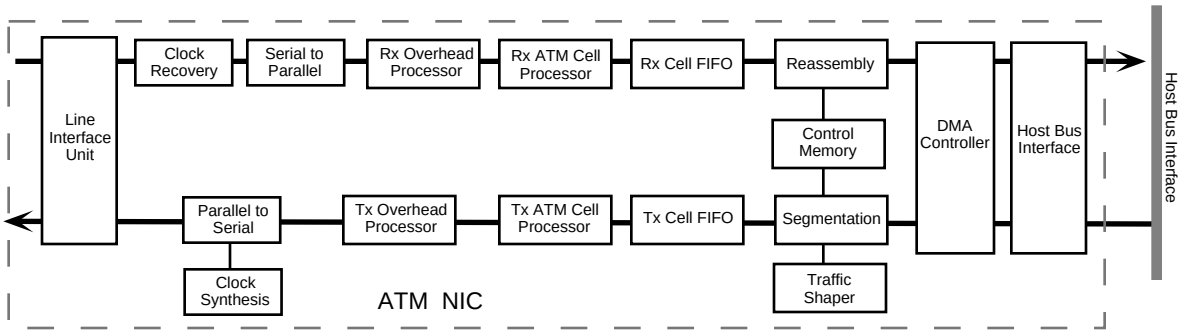

Figure 2. A generic ATM NIC architecture.

There are many ways to implement an ATM adapter including the use of discrete ICs, ASICs, microprocessors, and a mixture of these devices. However, multiple chip implementations are not only complicated to design but also costly to manufacture. In an era when the ATM adapter must compete head-on with other fast LAN technologies, one way to bring ATM to the desktop is to provide cost competitive NICs that use fewer parts.

The LASAR simplifies the design and manufacturing of ATM NICs by combining all the necessary functions on a single device. On the line side, the LASAR can connect directly to an OC-3 optical driver or to a UTP-5 line interface unit (LIU). On the system side, the LASAR can interface directly to a 32 bit 33 MHz PCI bus. Figure 3 illustrates the design of a SONET STS-1/3c[1] ATM NIC for the PCI bus.

[1]Unless specified otherwise, the term "SONET" is used to refer to both SONET and SDH and "STS-1/3c" is used to refer to STS-1 and STS-3C/STM-1 in the remainder of this document.

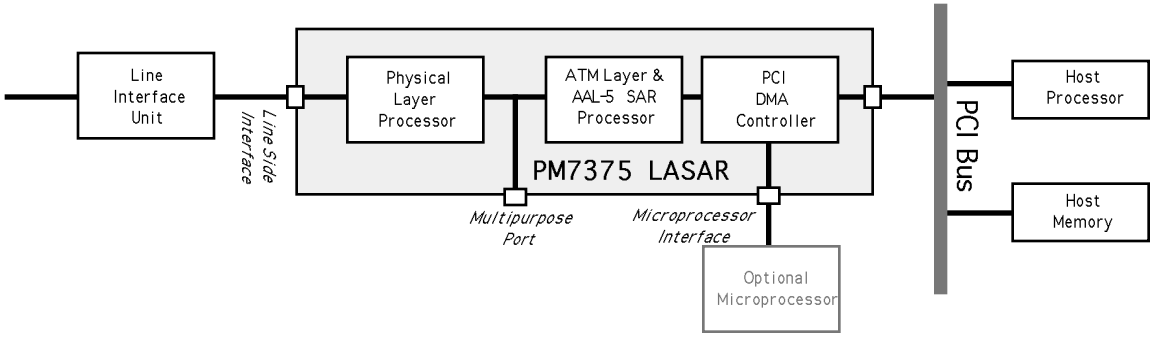

Figure 3: STS-3c/STS-1 ATM NIC example using the LASAR.

The initial configuration, ongoing control and monitoring of the LASAR can be performed by a PCI Host, an optional microprocessor, or the combination of both. The high bandwidth and low bus latency features offered by the PCI bus allow the segmentation and reassembly of packets in the host memory. In the transmit direction, the LASAR provides an 8 cell Service Data Unit (SDU) FIFO and in the receive direction a 96 cell SDU FIFO to allow for the bus latency. The transfer of packets between the LASAR and the host memory is facilitated by the PCI DMA Controller independent of the PCI Host.

Interface to External Physical Layer Processor

The LASAR's Multipurpose Port segments the ATM Layer & AAL-5 SAR Processor and PCI DMA Controller from the internal Physical Layer Processor. For applications that require the use of transmission technologies other than STS-1/3c, the Multipurpose Port can be configured as an 8 bit SCI-PHY ™ compliant interface to connect to an external physical layer processor.

Figure 4 provides an example where the LASAR is connected to the PM7345 S/UNI-PDH to provide a DS3/E3 User-Network Interface. The LASAR can access external devices when the Microprocessor Interface is configured for master mode operation. In this mode, the PCI Host configures, controls, and monitors the LASAR and the external devices attached to the Microprocessor Interface.

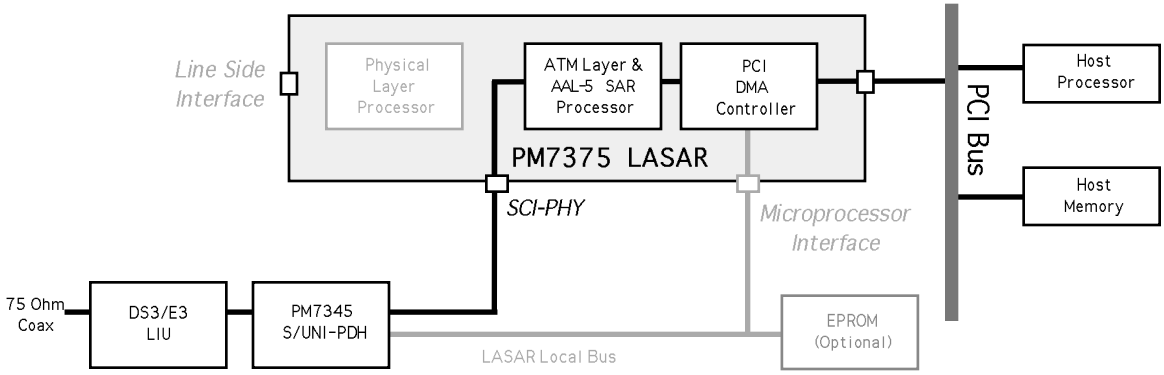

Figure 4: DS3/E3 ATM UNI Example.

While providing the ability to extend to external physical layer processors, the LASAR allows the designer to reuse the same device driver that interfaces to upper layer programs such as Signaling , LAN Emulation, and Network Management. By reusing the same device driver for multiple applications, a tremendous amount of development effort can be saved.

Multimedia Applications

The LASAR can be combined with an external AAL-1 SAR processor for certain video and multimedia applications. The external AAL-1 SAR processor can share the SONET framer with the internal AAL-5 SAR processor. The Multipurpose Port can be connected to an external FIFO to support the insertion and extraction of CBR cells that carry encoded video and audio signals as illustrated in Figure 5.

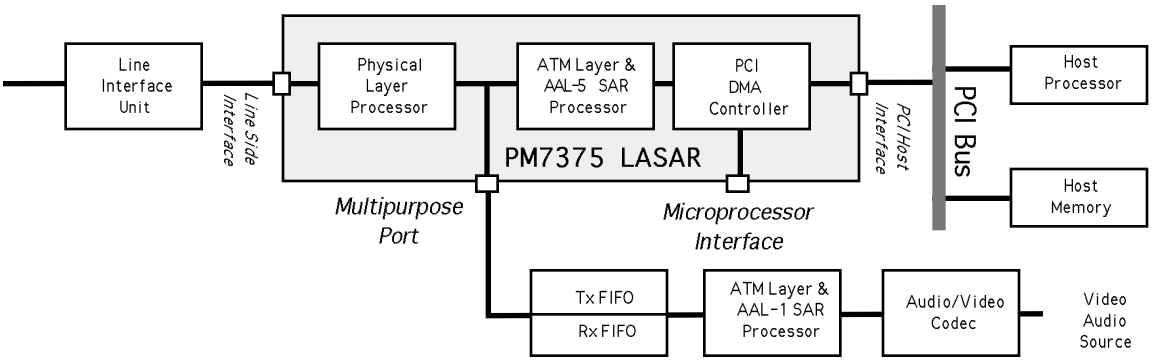

Figure 5: Multimedia Terminal Example.

In the receive direction, the LASAR supports cell copying and cell filtering operations. Cell copying is the action of directing cells from the Physical Layer Processor through the Multipurpose Port to the external FIFO. Cell filtering is the action of dropping cells destined for the PCI Host. The LASAR can be configured to detect and direct CBR cells to an FIFO where they can be processed by the AAL-1 SAR and the Audio/Video Codec.

In the transmit direction, the Multipurpose Port allows the insertion of CBR cells into an aggregate cell stream destined for the Physical Layer Processor. When the port indicates that a cell is ready to be transmitted, the LASAR inserts the cell into the aggregate cell stream at the earliest opportunity. The AAL-1 SAR Processor is responsible for implementing a traffic shaper for each CBR VC. The LASAR optionally applies an aggregate PCR traffic shaping mechanism on the aggregate cell stream using a peak cell rate counter. The aggregate PCR is user configurable from 32 Kbps to the full rate of 149 Mbps.

DETAILED DESCRIPTION

This section provides additional technical information on the Physical Layer Processor, ATM & Adaptation Layer Processor, and PCI DMA Controller.

Physical Layer Processor

The Physical Layer Processor implements the core of SONET STS-1/3c physical layer functions. The functional blocks are presented in Figure 6.

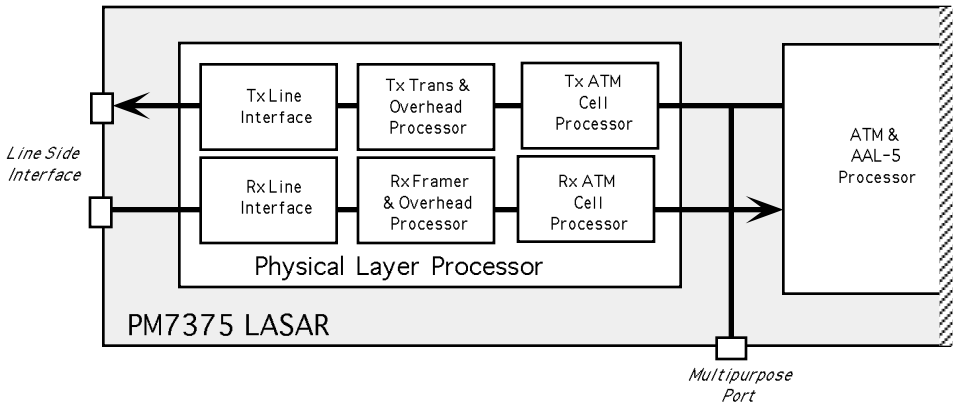

Figure 6. Physical Layer Processor Block Diagram.

Rx Line Interface

The Rx Line Interface block consists of a clock recovery unit (CRU) and a serial to parallel converter (SIPO). The CRU recovers the clock from the incoming bit serial data stream and is expected to be compliant with SONET jitter requirements. The SIPO converts the received bit serial SONET stream to a byte serial stream. The SIPO searches for the SONET framing pattern (A1, A2) in the incoming stream, and performs serial to parallel conversion on octet boundaries.

Rx Framer and Overhead Processor

The Rx Framer and Overhead Processor frames to an incoming SONET STS-1/3c stream and performs all the SONET section, line and path overhead processing. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line and path bit interleaved parity (B1, B2, B3), accumulating error counts at each level for performance monitoring purposes. Line and path far end block error indications (Z2, G1) are also accumulated. The LASAR interprets the received payload pointers (H1, H2) and extracts the synchronous payload envelope (SPE) which carries the received ATM cell payload.

Rx ATM Cell Processor

The Rx ATM Cell Processor receives the SPE from the Rx Framer and Overhead Processor. It performs ATM cell delineation, provides cell filtering based on idle/unassigned cell detection, cell filtering based on the Header Error Code (HEC) error detection and single bit correction, Generic Flow Control (GFC) field extraction, ATM layer alarm detection (OCD, LCD) and performs ATM cell payload descrambling. In addition, the number of received assigned cells is accumulated.

Tx ATM Cell Processor

In the transmit direction, the Transmit ATM Cell Processor inserts ATM cells into SONET SPEs. The GFC bits may optionally be inserted using a dedicated serial port. The HEC is automatically calculated and inserted. The cell payload is optionally scrambled. Generated transmit cells are automatically inserted into SONET STS-1/3c SPEs. In the absence of transmit cells, the LASAR automatically inserts idle/unassigned cells into the SPE.

Tx Transmit and Overhead Processor

The Tx Transmit and Overhead Processor generates the payload pointer (H1, H2) and inserts the SPE which carries the ATM cell payload. In addition, it formats SONET section, line, and path overhead appropriately. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and creates section, line and path bit interleaved parity (B1, B2, B3) as required to allow performance monitoring at the far end. Line and path far end block error indications (Z2, G1) are also inserted.

Tx Line Interface

The Tx Line Interface performs clock synthesis and performs parallel to serial conversion. The transmit clock may be synthesized from either a 19.44 MHz or a 6.48 MHz reference. The phase lock loop filter transfer function is optimized to enable the PLL to track the reference, yet attenuate high frequency jitter on the reference clock.

ATM & AAL-5 SAR Processor

The ATM & AAL-5 SAR Processor implements ATM Forum's ATM and AAL-5 protocol layers. It is a service user of the Physical Layer Processor and a service provider to the higher layer programs via the PCI DMA Controller The higher layer programs include Q.2931/Q.SAAL signaling, LAN Emulation, native ATM applications, and network management agents. The functional blocks of ATM & AAL-5 SAR Processor are illustrated in Figure 7.

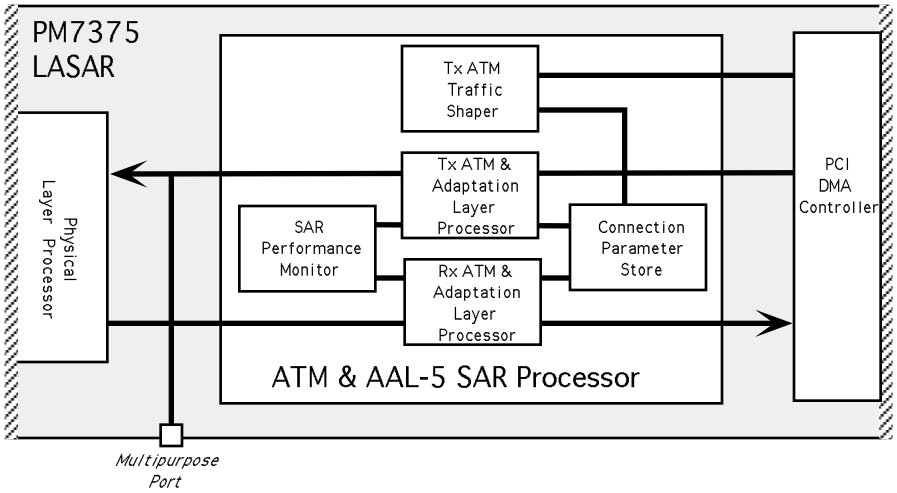

Figure 7. ATM & AAL-5 Layer Processor Block Diagram.

Rx ATM and Adaptation Layer Processor

The Rx ATM and Adaptation Layer Processor performs ATM Layer and AAL-5 reassembly functions. ATM Layer processing includes open VC verification, cell filtering, cell copying and CRC-10 verification. Cell filtering is the action of dropping cells intended for the PCI Host . Cell copying is the action of directing cells to the Multipurpose Port when it is configured in a cell source mode. Cell copying to the Multipurpose Port can be based on the VPI/VCI code and/or PTI codepoints "110" and "111" for F5 OAM cells.

The AAL processing includes the reassembly and verification of AAL-5 protocol data units (PDUs). The Rx ATM & Adaptation Layer Processor can optionally perform VC aging and non-activity termination. VC aging protects the LASAR from slow or dead connections that may be holding valuable receive buffer resources for an unacceptable duration. Non-activity termination allows for the automatic termination of a PDU under reassembly when the packet exceeds a user specified time-out period.

Tx ATM Traffic Shaper

The Tx ATM Traffic Shaper provides peak cell rate (PCR) enforcement using eight peak rate queues arranged as a group of four high priority queues and a group of four low priority queues. As part of the provisioning process, a VC must be associated with one of the eight rate queues. Once a VC is provisioned, packets supplied by the PCI DMA Controller are attached to the associated rate queue. High priority queues must be completely serviced before the low priority queues are serviced. If the high priority queues consume all the available link bandwidth, the low priority queues are allowed to starve. An indication is provided when any queue is experiencing a starvation condition.

The Tx ATM Traffic Shaper allows packet transmission at either the PCR or the sustainable cell rate (SCR). The SCR is specified as a fraction of the PCR (that is, SCR = PCR/n where n =1 to 8). The PCR transmission is defined on a per VC basis by associating a VC with one of the eight rate queues and by selecting whether to use 100%, 50%, or 25% of the PCR provided by the queue.

The SCR transmission is managed on a per VC basis through a token generation mechanism. The Tx ATM Traffic Shaper provides each VC with a token bucket and transmission is allowed only if the token bucket is not empty. Each transmitted cell consumes one token. When the VC is idle, the bucket is replenished at the SCR up to the capacity of the bucket. When the bucket is full, newly generated tokens are discarded. Cell transmission can be maintained at PCR when the bucket is not empty. When the bucket is empty, transmission continues at the SCR which is the rate of token generation.

Tx ATM & Adaptation Layer Processor

The Tx ATM & Adaptation Layer Processor performs ATM layer and AAL-5 segmentation functions. The AAL-5 processing is performed in conjunction with the PCI DMA Controller and the Tx Traffic Shaper. As the Tx Traffic Shaper schedules when cells from a packet under segmentation can be sent, the PCI DMA Controller retrieves the payload from the host memory and passes it to the Tx ATM & Adaptation Layer Processor which calculates the CRC-32 fields and forms the AAL-5 protocol data unit (PDU).

The ATM layer processing includes generating the GFC, VPI, VCI, PTI, CLP fields and optionally generating the CRC-10 field for each cell transmitted.

SAR Performance Monitor

The SAR Performance Monitor accumulates the following statistics:

- ATM Cell unprovisioned VPI/VCI errors
- ATM Cell CRC-10 errors
- Receive CPAAL5_PDU Invalid Common Part Indicator errors
- Receive CPAAL5_PDU Invalid SDU Length errors
- Receive CPAAL5_PDU CRC-32 errors
- Receive CPAAL5_PDU Oversize SDU errors
- Receive CPAAL5_PDU Abort errors
- Receive CPAAL5_PDU Count
- Receive CPAAL5_PDU Time-outs Count
- Receive buffer errors
- Transmit CPAAL5_PDU Oversize SDU errors
- Transmit CPAAL5_PDU Count

ATM cell counters are sized such that they can be polled once per second. Error counters are sized such that they can be polled once per second given that every PDU is in error and the average packet is size is 8 cells.

Connection Parameter Store

The Connection Parameter Store provides the internal VC parameter storage for both the 128 transmit and 128 receive VCs. The VC parameters are referenced by the Tx Traffic Shaper, Tx ATM & Adaptation Layer Processor, and Rx ATM & Adaptation Layer Processor. In addition, indirect access to the parameter memory space is also provided to the microprocessor.

PCI DMA Controller

The PCI DMA Controller (PCID) facilitates the communication between the PCI Host and the SAR engine as well as between the PCI Host and the microprocessor. Figure 8 illustrates the functional blocks of the PCID:

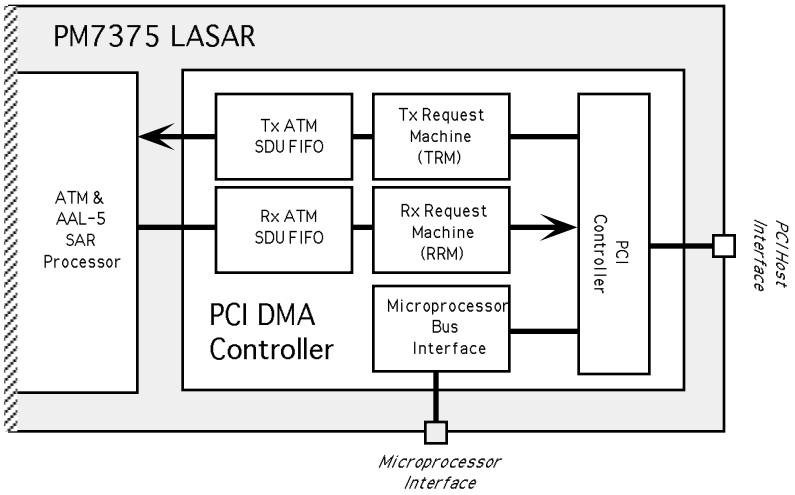

Figure 8. PCI DMA Controller Block Diagram

The PCI Controller provides a 32-bit 33 MHz PCI Local Bus interface that is compliant with Version 2.0 of the PCI Specifications. The PCI Controller supports both bus-master and bus-slave access modes. As a bus master, the PCI Controller uses burst DMA cycles to read or write data on the PCI bus independent of the PCI Host. As a bus slave, the PCI Controller allows the PCI Host to access the LASAR's internal registers, to communicate with the optional microprocessor, or to access external devices when the microprocessor is not present.

Two DMA channels are provided: A Transmit DMA Channel managed by the Tx Request Machine (TRM) and a Receive DMA Channel managed by the Rx Request Machine (RRM). To allow for the short but expected bus latency, up to 8 cells can be prefetched into the Tx ATM SDU FIFO in the transmit direction. A 96 cell Rx ATM SDU FIFO is provided between the Rx ATM & AAL Processor and the RRM to allow for a 270 µs PCI bus latency.

The microprocessor interface is provided for device configuration, ongoing control and monitoring by an external local microprocessor. For applications where local microprocessor control is not required and all device operations are performed by the PCI Host, the microprocessor interface allows the PCI Host to access the LASAR local bus. In the absence of the microprocessor, LASAR local bus can support up to two devices without using any external logic.

Transmit DMA Channel[2]

The Transmit DMA Channel transfers cell payloads of packet prepared by the PCI Host to the Tx ATM & Adaptation Layer Processor where they are combined with headers to form ATM cells. The Transmit DMA Channel is serviced at the source end by the PCI Host and at the destination end by the TRM.

The PCI Host uses a Transmit Descriptor (TD) to describe a packet or portion of a packet to TRM. The packet exchange mechanism uses three Descriptor Reference Queues as illustrated in Figure 9. The TD Free Queue contains TD References (TDRs) that points to unused TDs that the PCI Host can use to prepare packets in the host memory. The Ready Queues contain TDRs that points to TDs that describe packets in the host memory.

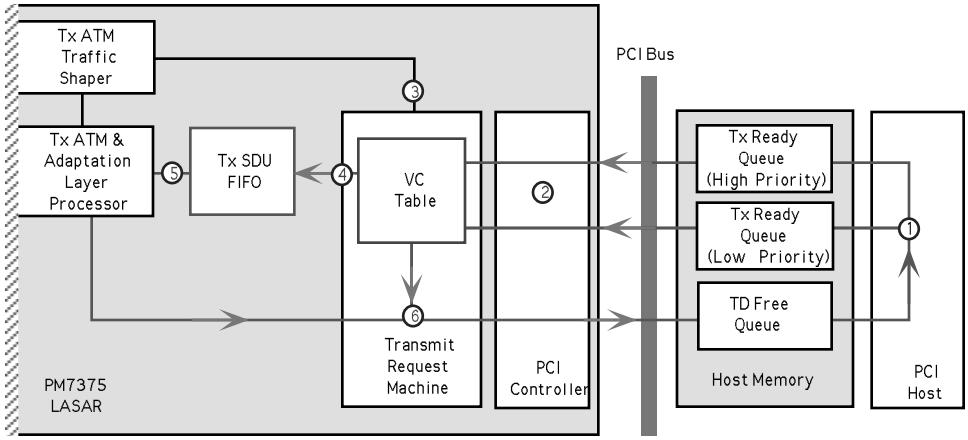

Figure 9. Transmit DMA Channel

The PCI Host is responsible for creating the data structures used in the DMA channel. All data structures and packet data reside in the host memory. After the VCs are provisioned, the operation of the Transmit DMA Channel is based on the process described below:

1 When the PCI Host is ready to send a packet, it retrieves free TDRs from the TD Free Queue to prepare a packet in the host memory. Once the VC attributes are initialized and the packet is prepared, the PCI Host places the TDRs into either the High Priority or Low Priority Tx Ready Queue.

2 The TRM checks the content of the Tx Ready Queues via the PCI Controller interface. The TRM services the High Priority Tx Ready Queue and only when it is empty does it service the Low Priority Tx Ready Queue. The TRM maintains an internal VC Table that keep track of prepared packets in the host memory on a per VC basis.

3 When the line bandwidth is available for a particular VC, the Tx Traffic Shaper places a request to the TRM to read cells from the host memory to the Tx ATM and Adaptation Layer Processor.

4 The TRM burst reads one cell at a time from the host memory into the Transmit SDU FIFO. Up to 8 cells can be buffered in the Tx SDU FIFO to allow for the bus latency.

5 The Tx ATM and Adaptation Layer Processor retrieves cells from the Transmit SDU FIFO and converts them into AAL-5 PDUs.

[2]The data structures used by the Transmit DMA Channel and the Receive DMA Channel are described in Appendix A of this document.

6 When a TDR used to describe the packet is processed, it is returned to the TD Free Queue to be reused. The TRM attaches the status of segmentation with the returning TDR to the PCI Host.

Receive DMA Channel

The Receive DMA Channel transfers packets received by the Rx ATM and Adaptation Layer Processor to the host memory. The receive DMA channel is serviced at the source end by the Receive Request Machine (RRM) and at the destination end by the PCI Host.

The RRM uses Receive Packet Descriptors (RPD), two Receive Packet Descriptor Reference Free queues, and a Receive Packet Descriptor Reference Ready queue on the packet reassembly path. The RRM uses Receive Management Descriptors (RMD), a Receive Management Descriptor Reference Free Queue and a Receive Management Descriptor Reference Ready Queue on the management cell path. All data structures, reassembled packets, and management cells reside in the host memory (Figure 10). The PCI Host is responsible for the initialization of the data structures used in the Receive DMA Channel.

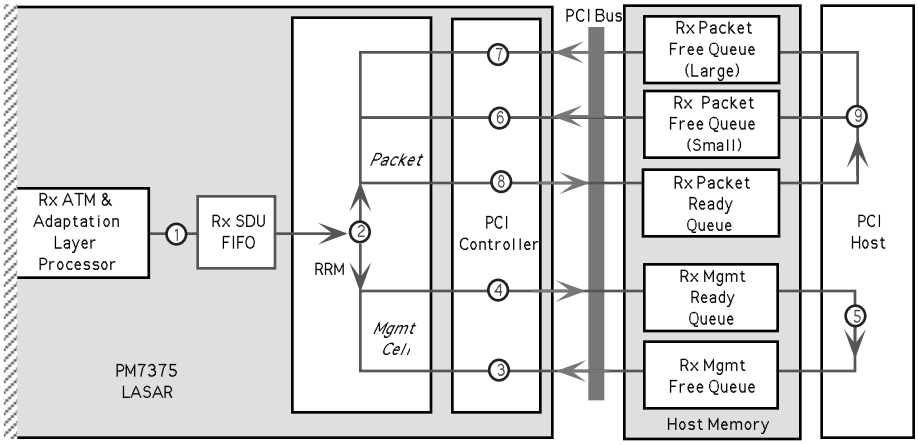

Figure 10. Receive DMA Channel

The operation of the Receive DMA Channel is described below:

1 The RRM receives cells associated with an open VC from the Rx ATM & Adaptation Layer Processor. Received cells are buffered in a 96 cell Receive SDU FIFO to allow for up to 270 µs of latency during bus request/grant cycles.

2 The RRM retrieves a cell from the SDU FIFO and determines whether it is a management cell or part of a packet under reassembly. Management cells and packet cells are processed separately.

Management Cell Processing

3 The RRM first retrieves a RMD Reference (RMDR) from the Rx Management Free Queue to describe a management cell in the host memory.

4 The RMDR points to a RMD which points to a buffer in the host memory where the management cell is burst written to. When the transfer of the management cell is completed, the RMDR is moved to the Rx Management Ready Queue and the PCI Host is alerted.

5 Once alerted, the PCI Host retrieves the RMDR from the Rx Management Ready Queue and follows the pointers to the management cell. When the management cell is processed, the PCI Host returns the RMDR back to the Rx Management Free Queue where it can be reused.

Packet Cell Processing

To ensure the optimal use of the host memory, the RRM uses two different buffer sizes to store packets in the host memory. The RRM always uses a small buffer to save the head of a packet. If the packet cannot fit completely inside the small buffer, the remainder of the packet is saved using one or more large buffers. The size of the small and large buffers are configurable at runtime and can be adjusted to suit different applications. The steps involved in the receive packet cell processing are described below:

6 When the start of a packet is detected, the RRM retrieves a RPDR from the Small Rx Packet Free Queue. The attributes of the packet, such as VPI/VCI, are copied to the RPD. The content of the packet is burst written to the small buffer referenced to by the RPD.

7 If a packet cannot fit completely inside a small buffer, the RRM retrieves a RPDR from the Large Rx Packet Free Queue.

8 The remainder of the packet is burst written to the large buffer referenced to by the RPD. The new RPD is joined to the tail of the previous RPD to form a linked list. This process is repeated until the entire packet is saved to the host memory.

9 The RRM alerts the PCI Host when the complete packet has been reassembled and all the RPDRs used to describe the packet are in the Rx Packet Ready Queue. The PCI Host retrieves the packet by traversing the RPD linked list and access the data in the buffers. Once processed, the PCI Host returns the first RPD to the Small Receive Packet Free Queue and all following RPDs to the Large Receive Packet Free Queue where they can be reused.

ADDITIONAL INFORMATION

PM7375 LASAR is supported by other documents including a data book, application notes, and a short form data sheet. Please contact PMC-Sierra for additional information:

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APPENDIX A: PCID DATA STRUCTURES

This section provides an overview of the data structures used in the DMA channels. The data structures include Descriptor, Descriptor Table, Descriptor Reference, and Descriptor Reference Queue. All the data structures reside in the host memory and must be allocated and initialized by the PCI Host.

Descriptor

The LASAR and the PCI Host use a 32 byte data structure, called Descriptor, to describe a packet or a portion of a packet in the host memory to each other. Different descriptors are used in the Transmit and Receive DMA Channels: In the transmit direction, the PCI Host uses a one or more Transmit Descriptors (TDs) to describe a packet to the TRM (Figure A1). In the receive direction, the RRM uses one or more Receive Packet Descriptors (RPDs) to describe a packet under reassembly and a Receive Management Descriptor (RMD) to describe an OAM cell to the PCI Host.

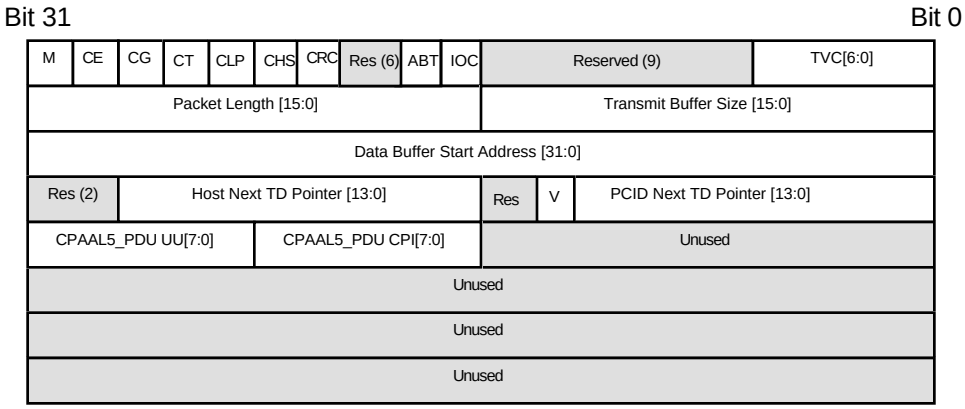

Figure A1: Transmit Descriptor

Each descriptor contains control fields, status fields, a pointer to a data buffer, and pointers to other descriptors. The latter feature allows descriptors to be connected in a chain to describe a packet that is scattered in multiple data buffers. The RMD does not support linking as the OAM cell can be stored in a single 48 byte buffer.

Descriptor Reference

Each descriptor can be addressed using a Descriptor Reference. A Descriptor Reference is an offset pointer to an entry in the descriptor table. Figure A2 illustrates how the physical address of a descriptor (RPD_ADDR) can be determined by summing the descriptor table base address (RPDTB) with the descriptor reference (RPDR).

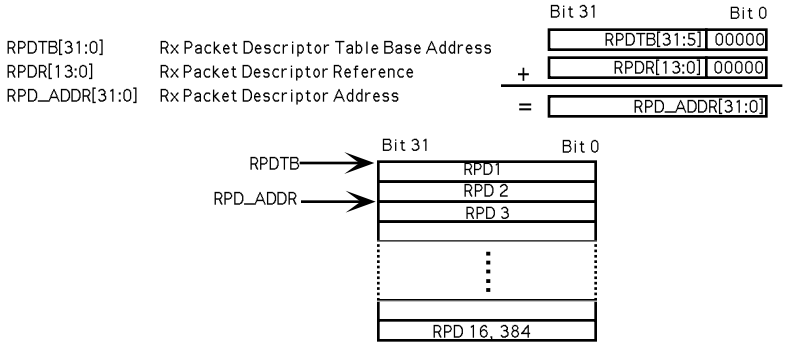

Figure A2: Receive Packet Descriptor Table Overview

Descriptor Table

Common descriptors reside in the same descriptor table. The TDs are located in the TD Table, the RPD in the RPD Table, and RMD in the RMD Table. All descriptor tables are located in the host memory and must be allocated by the PCI Host during initialization of the device. The size of each descriptor table is user configurable up to a maximum of 16,384 entries.

Descriptor Reference Queue

A Descriptor Reference Queue is a data structure used by the PCI Host and PCID to manage Descriptor References. Three Descriptor Reference Queues are used in the Transmit DMA Channel and five Descriptor Reference Queues are used in the Receive DMA Channel.

Each Descriptor Reference Queue uses four pointers: Start Address, End Address, Write Address and Read Address as illustrated in Figure A3. A new queue element is inserted at the Write Address. After the write operation the pointer is advanced to the next element in the queue. To read from the queue, the Read Address is first incremented and the next Descriptor Reference can then be retrieved from the Read Address. All pointers are specified in LASAR registers.

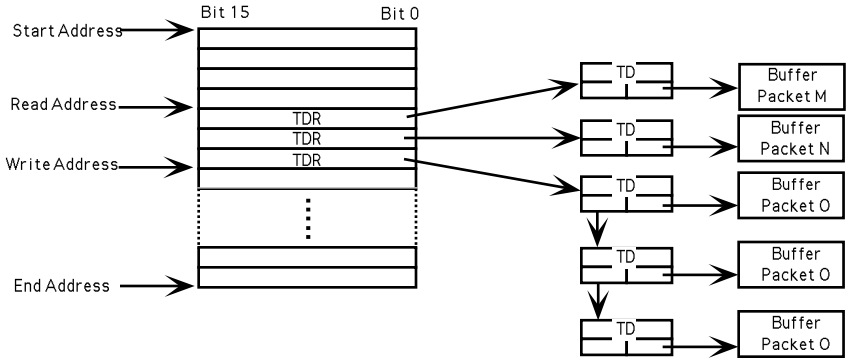

Figure A3: Transmit Descriptor Reference Queue Overview.

In the example in Figure A3, there are three TDRs pointing to three packets in the host memory. Each TDR references a TD which in turn points to a data buffer. Packets *M* and *N* each can fit in a single buffer and thus require only one TD. Packet *O* is scattered among three data buffers. Three TDs are connected in a chain to point to the three data buffers of packet *O.* The TRM and the PCI Host can traverse the list to access all the buffers of packet *O.*

GLOSSARY

AAL	ATM Adaptation Layer	An ATM protocol layer defined by ITU and adopted by the ATM Forum. The AAL defines a segmentation and reassembly protocol for mapping between data packet and the 48-octet ATM cell payload. Segmentation is process of breaking a data packet into ATM cell payloads. Reassembly is the process of putting together ATM cell payloads into a data packet.
ABR	Available Bit Rate	A traffic management service that is being defined by the ATM Forum. ABR allows for the dynamic sizing of cell rate according to the condition of the network.
ATM	Asynchronous Transfer Mode	A high speed connection-oriented multiplexing and switching method specified in international standards utilizing fix-length 53 bytes cells that can carry video, audio, and data signals.
CPAAL5_PDU	Common Part Convergence Sublayer AAL Type 5 Protocol Data Unit	A type of ATM Adaptation Layer specification as defined in ITU Recommendation I.363.
DMA	Direct Memory Access	A process that transfers data from memory to memory without CPU intervention.
GFC	Generic Flow Control	A field in the ATM cell that has local significance only and can be used to provide standardized local functions on the customer site.
HEC	Header Error Control	A field in the ATM cell that is used by the physical layer for detection/correction of bit errors in the cell header. It may also be used for cell delineation.
NIC	Network Interface Card	The attachment that connects a device to a network. An ATM NIC provides the UNI interface such that an end system can be connected to the ATM network. Also referred to as ATM adapter.
OC	Optical Carrier	The optical carrier level signal in SONET which results from an STS-n signal conversion.
PCI	Peripheral Component Interconnect	An open local bus standard for personal computers and workstations that provides a high-speed data path between the CPU and peripheral devices such as network card, video, and disk drive.
PCID	PCI DMA Controller	LASAR's functional block that provides 32 bit 33MHz PCI interface and a DMA controller that consists of a Transmit Request Machine (TRM) and a Receive Request Machine (RRM).
PCR	Peak Cell Rate	The highest cell rate specified in a VC. Cell transmission in that VC cannot exceed PCR, but can be less than PCR.
PHY	Physical Layer	The lowest ATM protocol layer. It is divided into two sublayers: the Physical Medium Dependent (PMD) sublayer and the Transmission Convergence (TC) sublayer. The PMD sublayer provides for the actual transmission of the bits in the ATM cells and the TC sublayer transforms the flow of cells into a steady flow of bits and bytes for the transmission over the physical medium.
RMD	Receive Management Descriptor	A 32 byte data structure used by the RRM and the PCI Host to describe a management cell in the host memory.

RMDR	Receive Management Descriptor Reference	An offset pointer to a RMD. The RMDR is also the carrier of the status of reassembly from RRM to the PCI Host.
RPD	Receive Packet Descriptor	A 32 byte data structure used by the RRM and the PCI Host to describe a packet or a portion of a packet in the host memory.
RPDR	Receive Packet Descriptor Reference	An offset pointer to a RPD. The RPDR is also the carrier of the status of reassembly from RRM to the PCI Host.
RRM	Receive Request Machine	The receive DMA controller portion of the PCID block of the LASAR.
SAR	Segmentation And Reassembly	See AAL.
SATURN™ Group	SONET/ATM User Network Development Group	A development group founded by PMC-Sierra and Sun Microsystems to facilitate the development of components for ATM LANS and WANs based on interoperability specifications published by the ATM Forum.
SCI-PHY™	SATURN Compliant Interface for ATM PHY Devices	A specification defined by the SATURN Group for the interconnect of physical layer ATM devices to ATM layer or ATM Adaptation Layer processor. SCI-PHY is a superset of the ATM Forum's Utopia specification for 8-bit cell based interchange.
SCR	Sustainable Cell Rate	The maximum average rate that a bursty traffic source can be sent.
SDH	Synchronous Digital Hierarchy	The European counterpart to SONET. SDH supports speeds ranging from 155 Mbits/sec and 2.5 GBits/sec.
SDU	Service Data Unit	Unit of information transferred across the OSI interface between service provider and service user.
SONET	Synchronous Optical NETwork	A fiber optic transmission system for high speed digital traffic. SONET supports line speeds ranging from 51 Mbits/sec to multiple gigabits per second.
SPE	Synchronous Payload Envelope	The SPE contains the information being transported by the SONET/SDH frame.
TD	Transmit Descriptor	The data structure used by the PCI Host and TRM to describe a packet or a portion of a packet in the host memory.
TDR	Transmit Descriptor Reference	An offset pointer to a TD. The TDR is also the carrier of the status of segmentation from TRM to PCI Host.
TRM	Transmit Request Machine	The transmit DMA controller portion of the PCID block of the LASAR.
UNI	User-Network Interface	The point where the user access the network.
UTP	Unshielded Twisted Pair	A cable medium with one or more pairs of twisted insulated copper conductors bound in a single plastic sheath.
VC	Virtual Circuit	A virtual connection established through the network from origination to destination, where cells are routed over the same path for the duration of the call. VCs appear to the end users as dedicated connections, but are actually network resources shared by multiple users.
VCI	Virtual Channel Identifier	A field within the ATM cell header which identifies the virtual channel of a VC.
VPI	Virtual Path Identifier	A field within the ATM cell header which identifies the virtual paths of a VC.

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