

FEATURES

- Monolithic SATURN®-compatible Asynchronous Transfer Mode (ATM) network interface.
- Implements the ATM transmission convergence (TC) sublayer for ATM according to ATM Forum specifications and ITU-T recommendations using the SONET/SDH 155.52 Mb/s format. Also implements ATM Forum specified “Mid-range PHY” rates of 51.52, 25.92 and 12.96 Mb/s.
- Includes on-chip clock recovery and clock synthesis at all rates. Clocking can be bypassed for use with external clock sources. Operates in master or slave (loop timed) timing modes.
- Provides TTL-compatible inputs and outputs. Provides differential pseudo-ECL-compatible serial line side inputs.
- Supports Fiber Optic, Unshielded Twisted Pair and Shielded interfaces.
- Processes all SONET/SDH UNI overhead.
- Provides access to section and line datalinks and all additional transport and path overhead to allow additional external processing for full SONET/SDH Network-Node Interface (NNI) compliance.
- Provides synchronous 8-bit or 16-bit SCI-PHY™ system side interface with 4-cell deep FIFO buffers in transmit and receive paths with parity support.
- Inserts and extracts ATM payloads using cell delineation.
- Provides a generic 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Software-compatible with the PM5345 S/UNI-155™, PM5346 S/UNI-155-LITE™ and the PM5355 S/UNI-622™.
- Provides a standard 5-signal P1149.1 JTAG test port for boundary scan board test purposes.
- Low power, +5 V CMOS technology.
- Packaged in a 208 pin (28mm x 28mm) PQFP with 0.5mm pin pitch.
- Industrial temperature range operation (-40°C to +85°C).
- Counts received cells written into the receive FIFO, received HCS errored cells that are discarded, and received HCS errored cells that are corrected and passed through the receive FIFO.

- Counts transmit cells read from the transmit FIFO.
- Inserts a register programmable path signal label (C2).
- Inserts path B3, path FEBE indications, line B2, line FEBE indications, and section B1 to allow performance monitoring at the far end.
- Optionally inserts the 16- or 64-byte section trace (J0) sequence and the 16 or 64 byte path trace (J1) sequence from internal register banks.
- Optionally inserts an externally generated section user channel (F1), order wire channels (E1, E2) and the DCC channels (D1-D3 and D4-D12) via serial interfaces.
- Optionally inserts path AIS, path RDI, line AIS, and line RDI.
- Optionally inserts register programmable APS (K1, K2) and synchronization status (Z1) bytes.

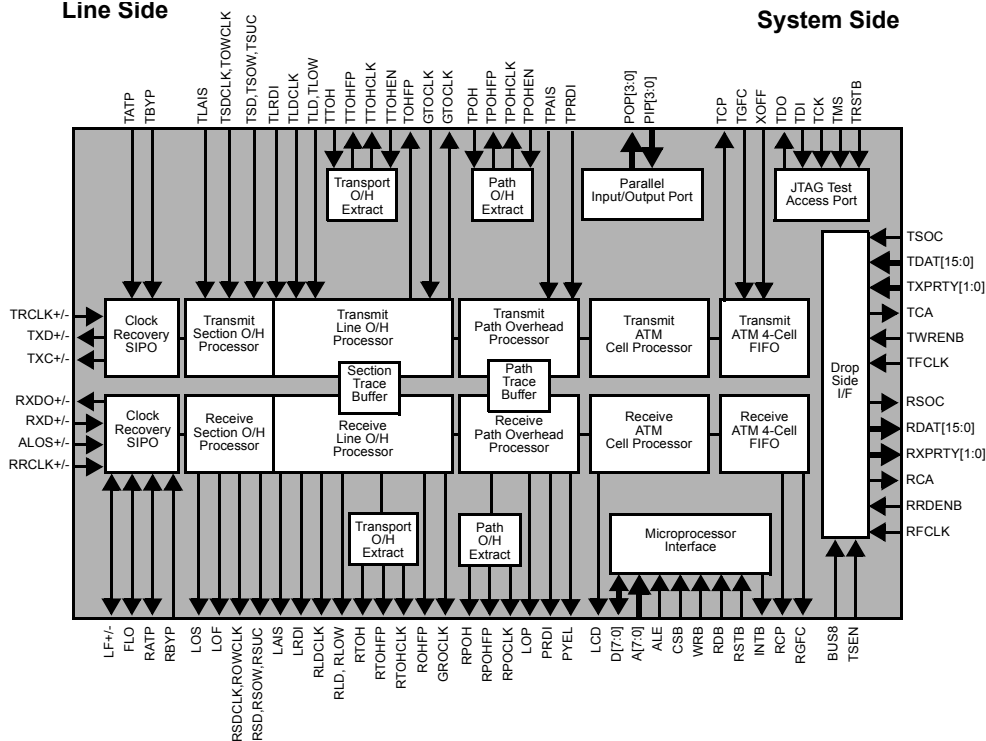
- Filters and captures the automatic protection switch channel (K1, K2) bytes in readable registers and detects APS byte failure.

- Extracts the 16- or 64-byte section trace (J0) sequence and the 16- or 64-byte path trace (J1) sequence into internal register banks.
- Extracts the DCC channels (D1-D3 and D4-D12) for optional external processing.
- Detects Loss Of Signal (LOS), Out Of Frame (OOF), Loss Of Frame (LOF), line Alarm Indication Signal (AIS), line Remote Defect Indication (RDI-L), Loss Of Pointer (LOP), path AIS, path RDI (RDI-P) and Loss Of Cell Delineation (LCD).
- Counts received section B1 errors, line B2 errors, line FEBEs, path B3 errors and path FEBEs for performance monitoring purposes.

- ATM Switching Systems
- ATM Access Systems
- LAN Switches, Hubs and Routers
- ATM Test Equipment
- SONET or SDH ATM Interfaces

Line Side

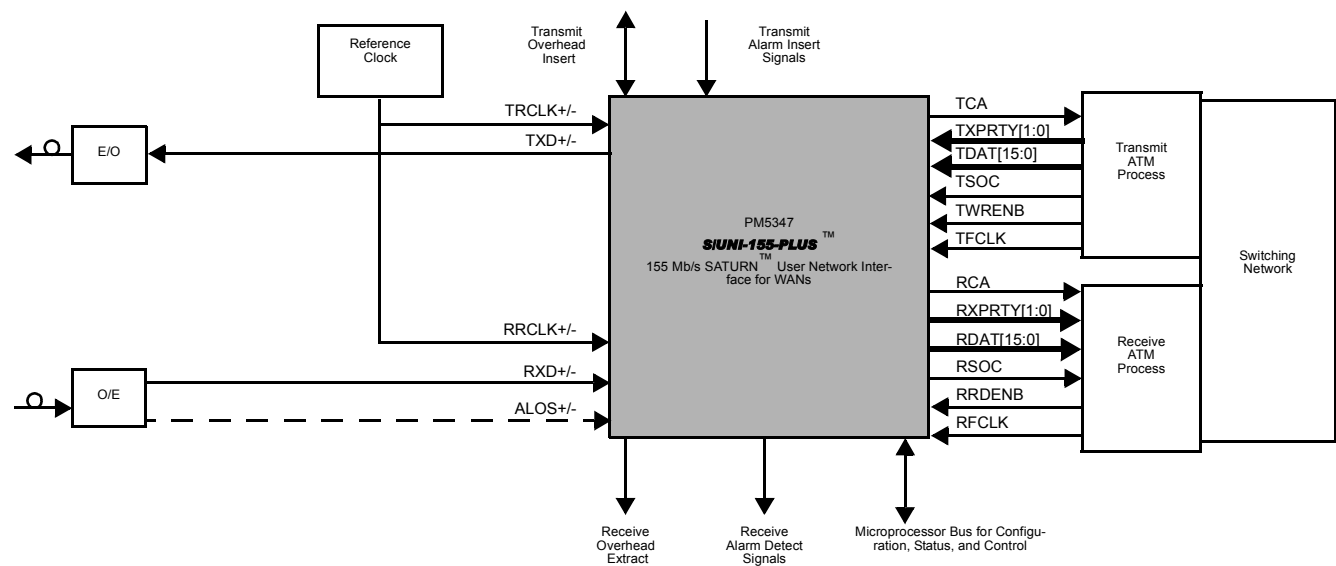
System Side



155 Mb/s SATURN User Network Interface for WANs

TYPICAL APPLICATION

155 Mb/s ATM SWITCH PORT INTERFACE



STS-3C/STM-1 OVERHEAD BYTE USAGE

A1						C1/J0	C1	C1	J1
B1						F1			B3
D1						D3			C2
H1	H1	H1	H2	H2	H2	H3	H3	H3	G1
B2	B2	B2	K1			K2			
D4			D5			D6			
D7			D8			D9			
D10			D11			D12			
Z1					M1	E2			Z5

Transport Overhead SOH

Path Overhead POH

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