Integrated Circuit Systems, Inc.

ICSSSTUA32S865A

28-Bit Registered Buffer for DDR2

Recommended Application:
- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS97U877
- Ideal for DDR2 400, 533 and 667

Product Features:
- 28-bit 1:2 registered buffer with parity check functionality
- Supports SSTL_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on CSR# and RESET# inputs
- Low voltage operation V_{DD} = 1.7V to 1.9V
- Available in 160 BGA package
- Green packages available

Pin Configuration
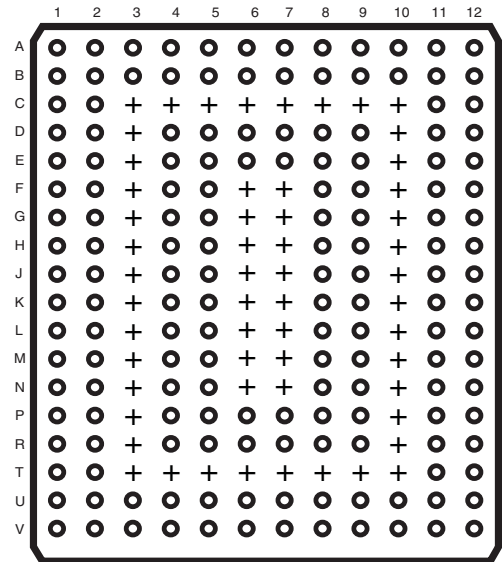
160 Ball BGA (Top View)

Functionality Truth Table

Inputs							Outputs		
RESET#	DCS0#	DCS1#	CSGate Enable	CK	CK#	Dn, DODTn, DCKEn	Qn	QCS#	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L
H	L	L	X	↑	↓	H	H	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	L
H	L	H	X	↑	↓	H	H	L	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L
H	H	L	X	↑	↓	H	H	H	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	L
H	H	H	L	↑	↓	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	L
H	H	H	H	↑	↓	H	Q_0	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L

Ball Assignments

	1	2	3	4	5	6	7	8	9	10	11	12
A	VREF	NC	PARIN	NC	NC	QCKE1A	QCKE0A	Q21A	Q19A	Q18A	Q17B	Q17A
B	D1	D2	NC	NC	NC	QCKE1B	QCKE0B	Q21B	Q19B	Q18B	QODT0B	QODT0A
C	D3	D4									QODT1B	QODT1A
D	D6	D5		VDDL	GND	NC	NC	GND	GND		Q20B	Q20A
E	D7	D8		VDDL	GND	VDDL	VDDR	GND	GND		Q16B	Q16A
F	D11	D9		VDDL	GND			VDDR	VDDR		Q1B	Q1A
G	D18	D12		VDDL	GND			VDDR	VDDR		Q2B	Q2A
H	CSGateEN	D15		VDDL	GND			GND	GND		Q5B	Q5A
J	CK	DCS0#		GND	GND			VDDR	VDDR		QCS0B#	QCS0A#
K	CK#	DCS1#		VDDL	VDDL			GND	GND		QCS1B#	QCS1A#
L	RESET#	D14		GND	GND			VDDR	VDDR		Q6B	Q6A
M	D0	D10		GND	GND			GND	GND		Q10B	Q10A
N	D17	D16		VDDL	VDDL			VDDR	VDDR		Q9B	Q9A
P	D19	D21		GND	VDDL	VDDL	VDDR	VDDR	GND		Q11B	Q11A
R	D13	D20		GND	VDDL	VDDL	GND	GND	GND		Q15B	Q15A
T	DODT1	DODT0									Q14B	Q14B
U	DCKE0	DCKE1	MCL	PTYERR#	MCH	Q3B	Q12B	Q7B	Q4B	Q13B	Q0B	Q8B
V	VREF	MCL	MCL	NC	MCH	Q3A	Q12A	Q7A	Q4A	Q13A	Q0A	Q8A

Note: An empty cell indicates no ball is populated at that gridpoint. NC denotes a no-connect (ball present but not connected to the die). MCL denotes a pin that Must be Connected LOW. MCH denotes a pin that Must be Connected HIGH.

General Description

This 28-bit 1:2 registered buffer with parity is designed for 1.7V to 1.9V V_{DD} operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8 V CMOS drivers that have been optimized to drive the DDR2 DIMM load. The **ICSSSTUA32S865A** operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going high, and CK# going low.

The device supports low-power standby operation. When the reset input (RESET#) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when RESET# is low all registers are reset, and all outputs except PTYERR# are forced low. The LVCMOS RESET# input must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied, RESET# must be held in the low state during power up.

In the DDR2 RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET# until the input receivers are fully enabled, the design of the **ICSSSTUA32S865A** must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both DCS0# and DCS1# inputs and will gate the Qn outputs from changing states when both DCS0# and DCS1# are high. If either DCS0# or DCS1# input is low, the Qn outputs will function normally. The RESET# input has priority over the DCS0# and DCS1# control and will force the Qn outputs low and the PTYERR# output high. If the DCS-control functionality is not desired, then the CSGateEnable input can be hardwired to ground, in which case, the setup-time requirement for DCS would be the same as for the other D data inputs.

The **ICSSSTUA32S865A** includes a parity checking function. The **ICSSSTUA32S865A** accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the D-inputs and indicates whether a parity error has occurred on its open-drain PTYERR# pin (active LOW).
Package options include 160-ball Thin Profile Fine Pitch BGA (TFBGA) (12 X 18 array, 9.0 X 13.0 mm body size, 0.65 mm pitch, MO-246, Issue A).

Inputs							Output
RESET#	DCS0#	DCS1#	CK	CK#	of inputs = H (D0-D21)	PARIN*	PTYERR#**
H	L	H	↑	↓	Even	L	H
H	L	H	↑	↓	Odd	L	L
H	L	H	↑	↓	Even	H	L
H	L	H	↑	↓	Odd	H	H
H	H	L	↑	↓	Even	L	H
H	H	L	↑	↓	Odd	L	L
H	H	L	↑	↓	Even	H	L
H	H	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$PTYERR\#_0$
H	X	X	L or H	L or H	X	X	$PTYERR\#_0$
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	H

* PARIN arrives one clock cycle after the data to which it applies.

** This transition assumes PTYERR# is high at the crossing of CK going high and CK# going low. If PTYERR# is low, it stays latched low for two clock cycles or until RESET# is driven low.
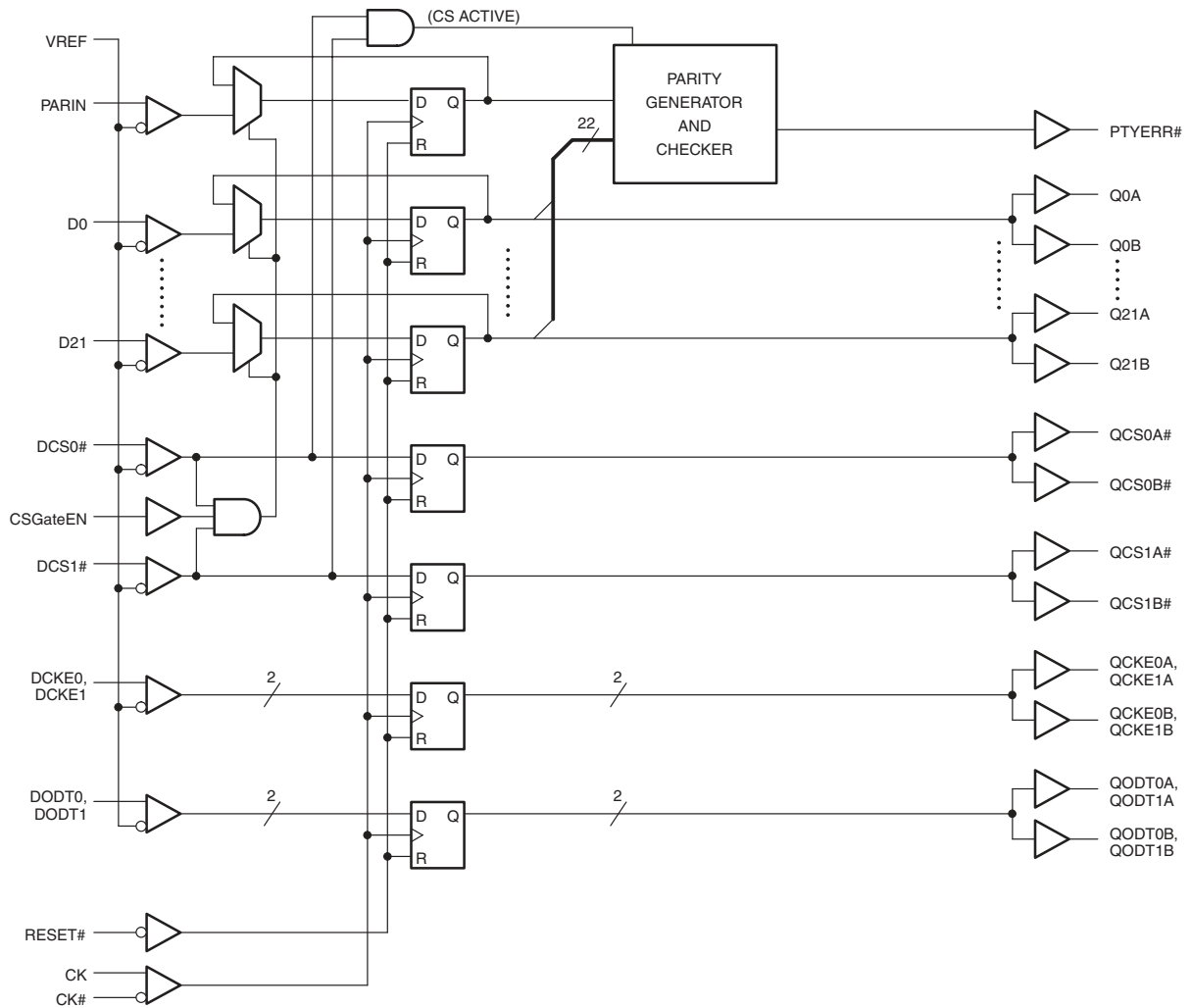
Ball Assignment

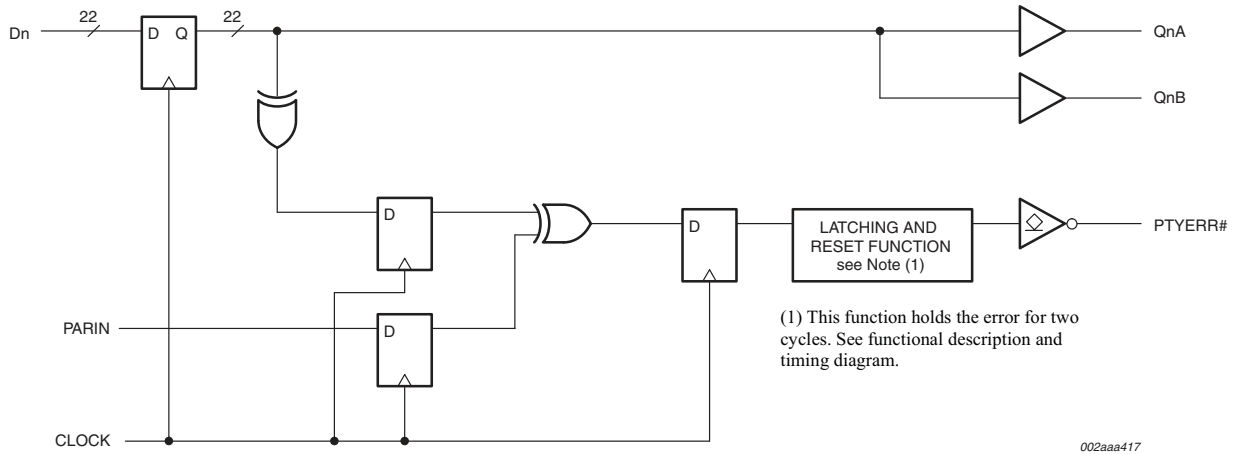| Signal Group	Signal Name	Type	Description
Ungated inputs	DCKE0, DCKE1, DODT0, DODT1	SSTL_18	DRAM function pins not associated with Chip Select.
Chip Select gated inputs	D0 ... D21	SSTL_18	DRAM inputs, re-driven only when Chip Select is LOW.
Chip Select inputs	DCS0#, DCS1#	SSTL_18	DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGateEN high) when at least one Chip Select input is LOW.
Re-driven outputs	Q0A...Q21A, Q0B ... Q21B, QCS#0-1A,B, QCKE0-1A,B, QODT0-1A,B	SSTL_18	Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock.
Parity input	PARIN	SSTL_18	Input parity is received on pin PARIN and should maintain odd parity across the D0...D21 inputs, at the rising edge of the clock.
Parity error output	PTYERR#	Open drain	When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. PTYERR# will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition).
Program inputs	CSGateEN	1.8 V LVCMOS	Chip Select Gate Enable. When HIGH, the D0..D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0...D21 inputs will be latched and redriven on every rising edge of the clock.
Clock inputs	CK, CK#	SSTL_18	Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CK).
Miscellaneous inputs	MCL, MCH		Must be connectedd to a logic LOW or HIGH.
	RESET#	1.8 V LVCMOS	Asynchronous reset input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. RESET# also resets the PTYERR# signal.
	VREF	0.9 V nominal	Input reference voltage for the SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.

Block Diagram

Parity Functionality Block Diagram

(1) This function holds the error for two cycles. See functional description and timing diagram.
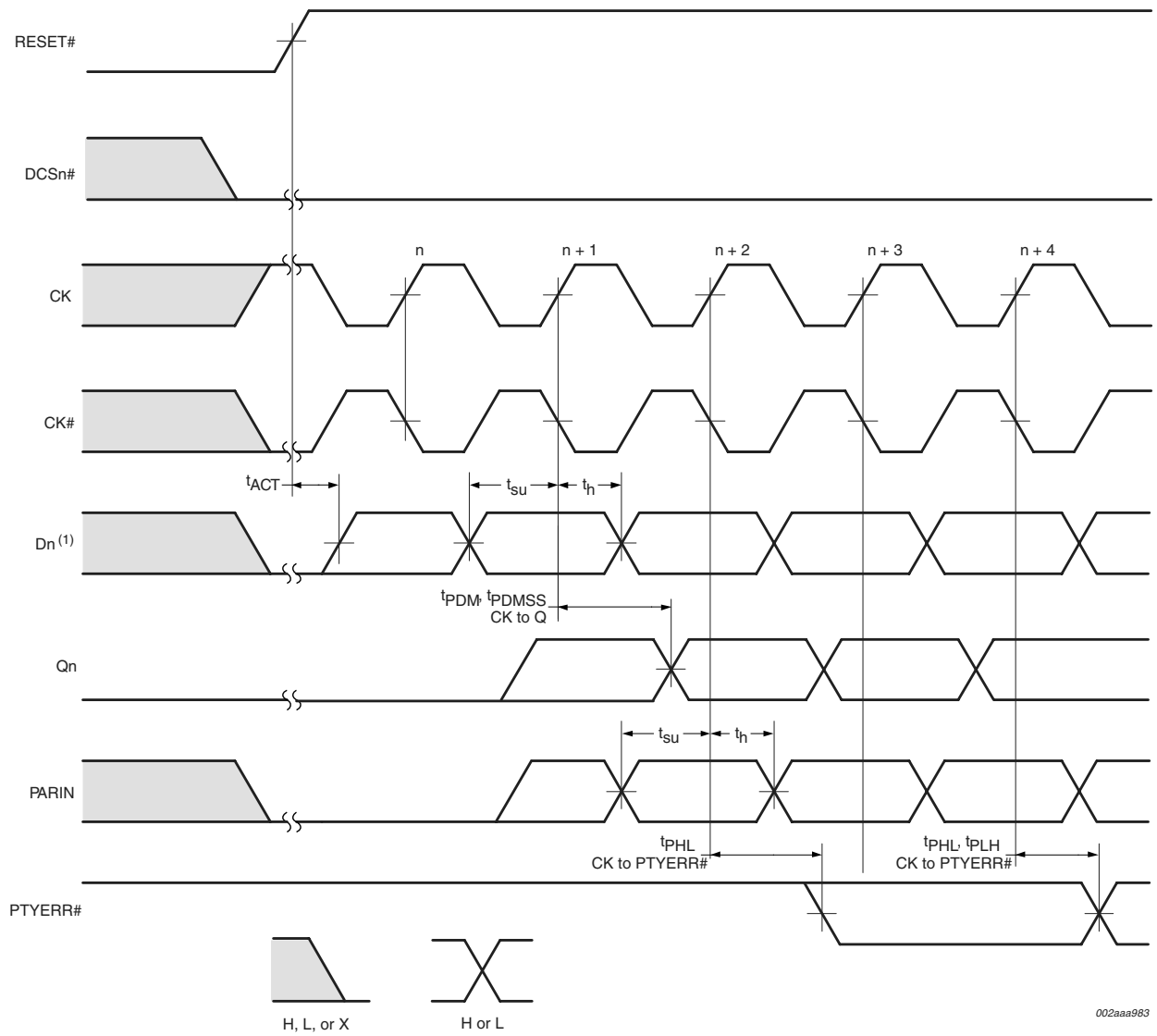
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Register Timing

Figure 4 — RESET# switches from L to H

(1) After RESET# is switched from LOW to HIGH, all data and PARIN input signals must be set and held LOW for minimum time of t_{ACT} (max.) to avoid false error.
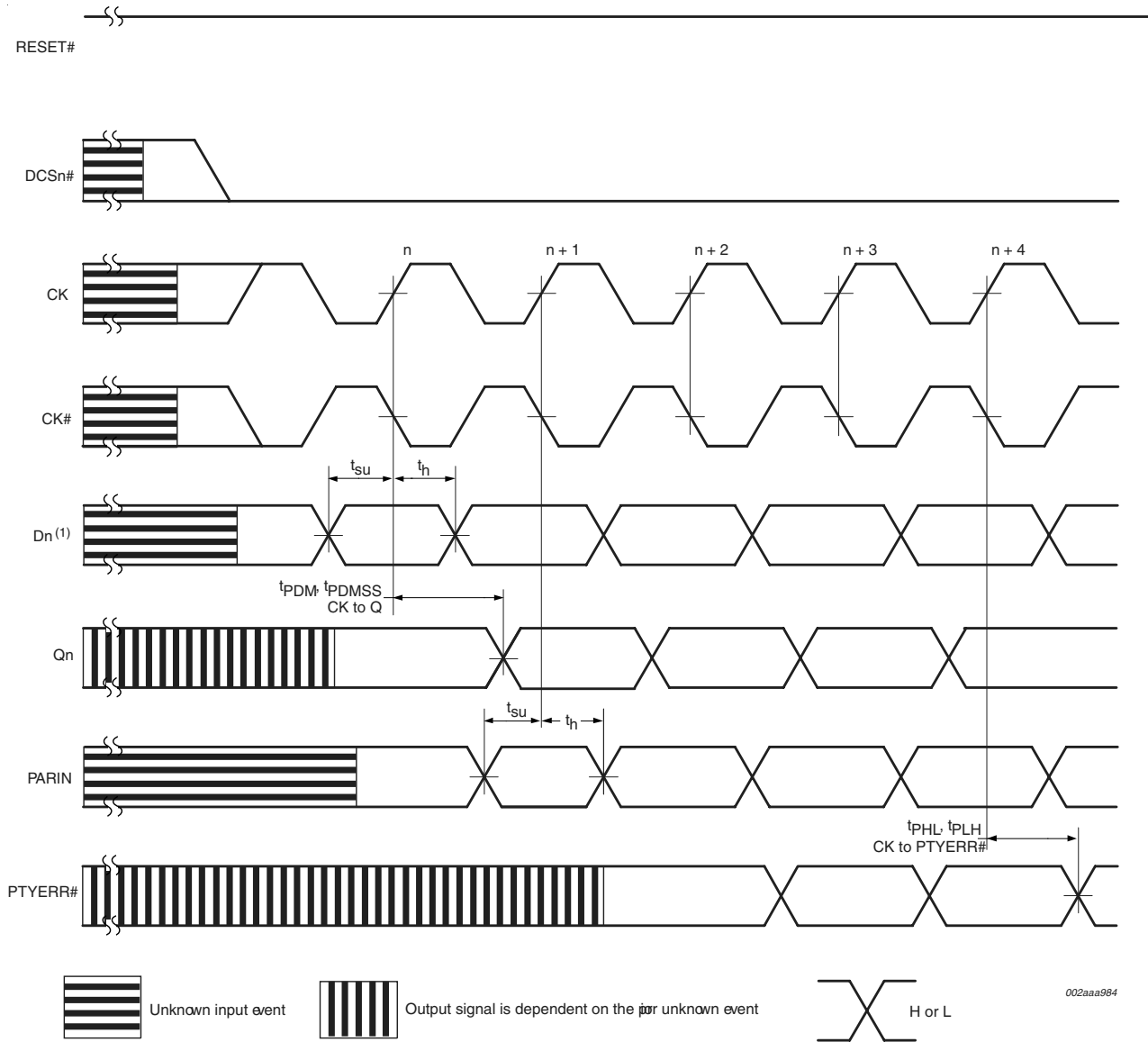
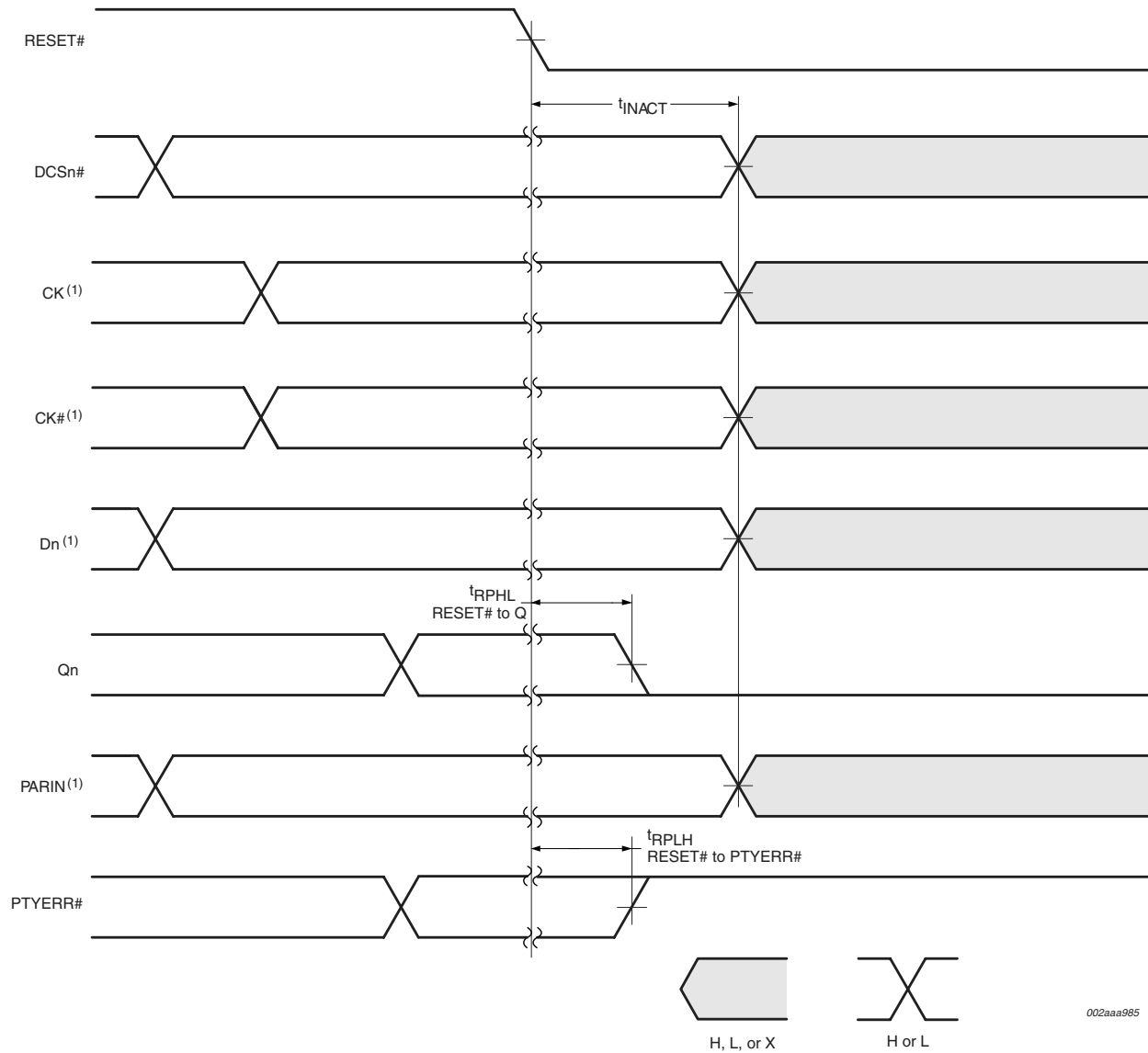## Register Timing

Figure 5 — RESET# being held HIGH

Register Timing

Figure 6 — RESET# switches from H to L

(1) After RESET# is switched from HIGH to LOW, all data and clock input signals must be set and held at valid logic levels (not floating) for a minimum time of t_{INACT} (max.).

Absolute Maximum Ratings

Storage Temperature . . . . $-65°C$ to $+150°C$
Supply Voltage . . . . -0.5 to 2.5V
Input Voltage[1] . . . . -0.5 to VDD + 2.5V
Output Voltage[1,2] . . . . -0.5 to VDDQ + 0.5
Input Clamp Current . . . . ±50 mA
Output Clamp Current . . . . ±50mA
Continuous Output Current . . . . ±50mA
VDDQ or GND Current/Pin . . . . ±100mA

Package Thermal Impedance[3] . . . . 36°C

Notes:
1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level $V_0 > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V_{DD}	I/O Supply Voltage		1.7	1.8	1.9	
V_{REF}	Reference Voltage		0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	
V_I	Input Voltage		0		V_{DDQ}	
$V_{IH (DC)}$	DC Input High Voltage	Data Inputs	V_{REF} + 0.125			
$V_{IH (AC)}$	AC Input High Voltage		V_{REF} + 0.250			
$V_{IL (DC)}$	DC Input Low Voltage				V_{REF} - 0.125	V
$V_{IL (DC)}$	AC Input Low Voltage				V_{REF} - 0.250	
V_{IH}	Input High Voltage Level	RESET#, C0, C1	0.65 x V_{DDQ}			
V_{IL}	Input Low Voltage Level				0.35 x V_{DDQ}	
V_{ICR}	Common mode Input Range	CLK, CLK#	0.675		1.125	
V_{ID}	Differential Input Voltage		0.600			
I_{OH}	High-Level Output Current				-8	mA
I_{OL}	Low-Level Output Current				8	
T_A	Operating Free-Air Temperature		0		70	°C

[1]Guaranteed by design, not 100% tested in production.

Note: Reset# and Cn inputs must be helf at valid logic levels (not floating) to ensure proper device operation.

The differential inputs must not be floating unless Reset# is low.

Electrical Characteristics - DC

T_A = 0 - 70°C; V_{DD} = 2.5 +/-0.2V, V_{DDQ}=2.5 +/-0.2V; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS	V_{DDQ}	MIN	TYP	MAX	UNITS
V_{OH}		I_{OH} = -6mA	1.7V	1.2			
V_{OL}		I_{OL} = 6mA	1.7V			0.5	
I_I	All Inputs	V_I = V_{DD} or GND	1.9V			±5	µA
I_{DD}	Standby (Static)	RESET# = GND	1.9V			200	µA
	Operating (Static)	V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, RESET# = V_{DD}				80	mA
I_{DDD}	Dynamic operating (clock only)	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK# switching 50% duty cycle.	I_O = 0		TBD		µ/clock MHz
	Dynamic Operating (per each data input)	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL\,(AC)}$, CLK and CLK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle	1.8V		TBD		µA/ clock MHz/data
C_i	Data Inputs	V_I = V_{REF} ±350mV		2.5		3.5	pF
	CLK and CLK#	V_{ICR} = 1.25V, $V_{I(PP)}$ = 360mV		2		3	
	RESET#	V_I = V_{DDQ} or GND			2.5		

Notes:

1 - Guaranteed by design, not 100% tested in production.

Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range (See figure 7)

PARAMETER	V_{DD} = 1.8V ± 0.1V		UNIT
	MIN	MAX	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ[1]		1	V/ns

1. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETERS		V_{DD} = 1.8V ±0.1V		UNITS
			MIN	MAX	
f_{clock}	Clock frequency			410	MHz
t_W	Pulse duration		1		ns
t_{ACT}	Differential inputs active time			10	ns
t_{INACT}	Differential inputs inactive time			15	ns
t_S	Setup time	Data before CLK↑, CLK#↓	0.5		ns
		DCS0, DSC1# before CK↑, CK#↓, CSR# high	0.7		
t_H	Hold time	DCS#, DODT, DCKE and Q after CK↑, CK#↓	0.50		ns
	Hold time	PAR_IN after CK↑, CK#↓	0.50		ns

Notes: 1 - Guaranteed by design, not 100% tested in production.

2 - For data signal input slew rate of 1V/ns.

3 - For data signal input slew rate of 0.5V/ns and < 1V/ns.

4 - CLK/CLK# signal input slew rate of 1V/ns.

Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

Symbol	Parameter	Measurement Conditions	MIN	MAX	Units
fmax	Max input clock frequency		410		MHz
t_{PDM}	Propagation delay, single bit switching	CK↑ to CK#↓ QN	1.25	1.9	ns
t_{LH}	Low to High propagation delay	CK↑ to CK#↓ to PTYERR#	1.2	3	ns
t_{HL}	High to low propagation delay	CK↑ to CK#↓ to PTYERR#	1	3	ns
t_{PDMSS}	Propagation delay simultaneous switching	CK↑ to CK#↓ QN		2	ns
t_{PHL}	High to low propagation delay	Reset# ↓ to QN↓		3	ns
t_{PLH}	Low to High propagation delay	Reset# ↓ to PTYERR#↑		3	ns

1. Guaranteed by design, not 100% tested in production.
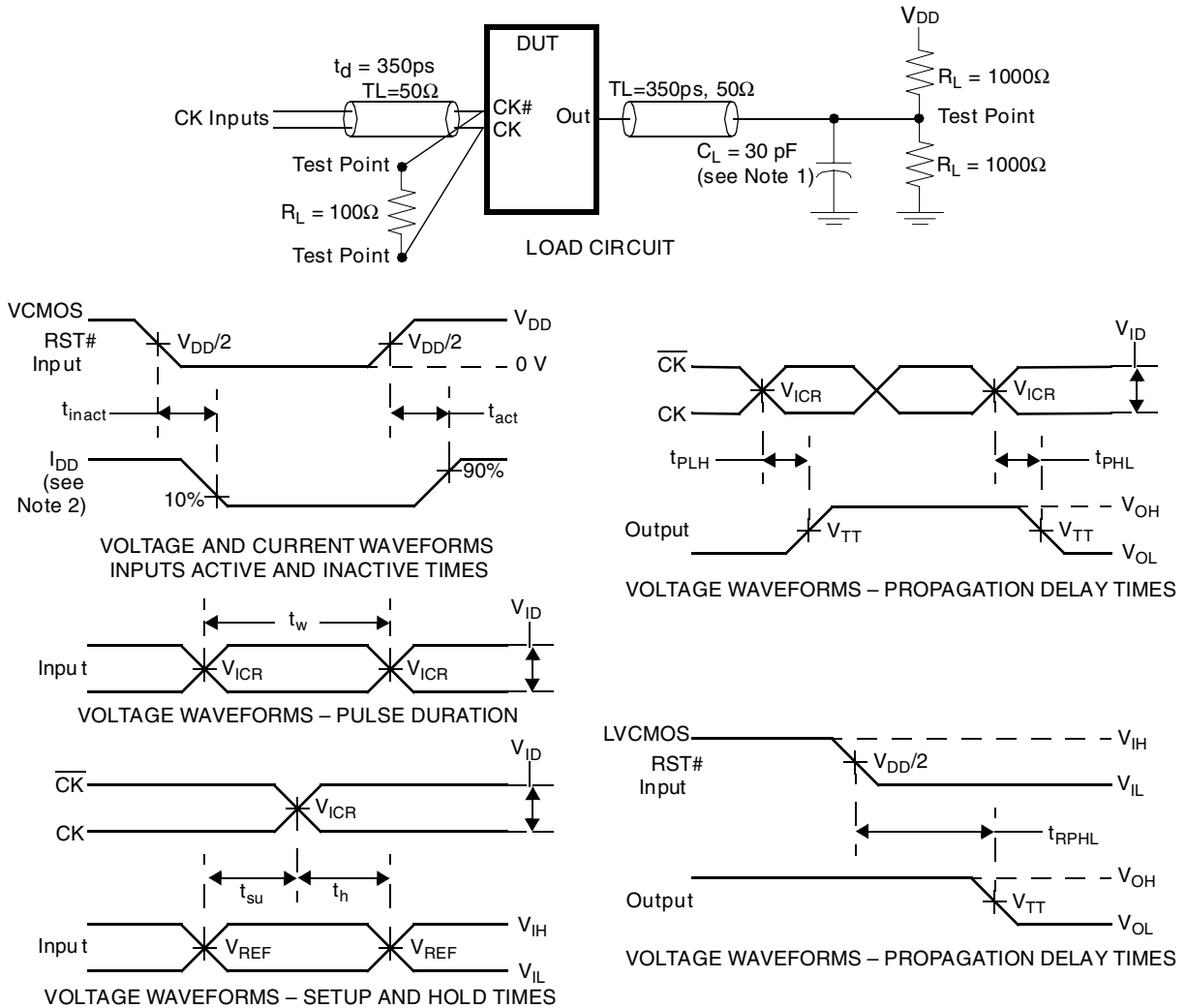
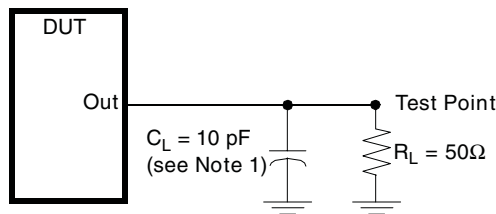Figure 6 — Parameter Measurement Information (V_{DD} = 1.8 V ± 0.1 V)

Notes: 1. C_L incluces probe and jig capacitance.

2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and Io = 0mA.

3. All input pulses are supplied by generators having the following charaecteristics: PRR ≤10 MHz, Zo=50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

4. The outputs are measured one at a time with one transition per measurement.

5. V_{REF} = V_{DD}/2

6. V_{IH} = V_{REF} + 250 mV (ac voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS input.

7. V_{IL} = V_{REF} - 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

8. V_{ID} = 600 mV

9. t_{PLH} and t_{PHL} are the same as t_{PDM}.
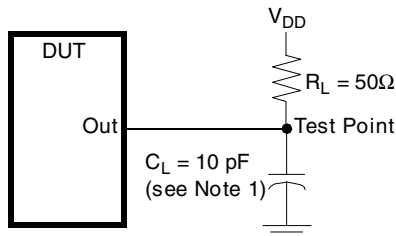
LOAD CIRCUIT – HIGH-TO-LOW SLEW-RATE MEASUREMENT
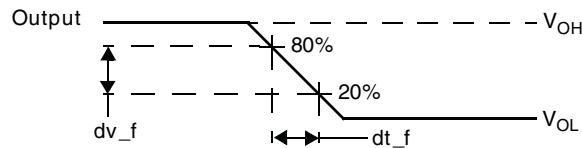
VOLTAGE WAVEFORMS – HIGH-TO-LOW SLEW-RATE MEASUREMENT

LOAD CIRCUIT – LOW-TO-HIGH SLEW-RATE MEASUREMENT
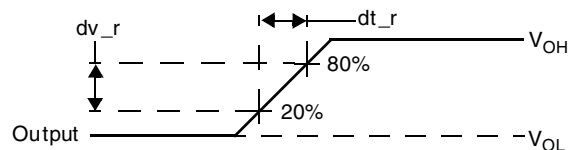
VOLTAGE WAVEFORMS – LOW-TO-HIGH SLEW-RATE MEASUREMENT

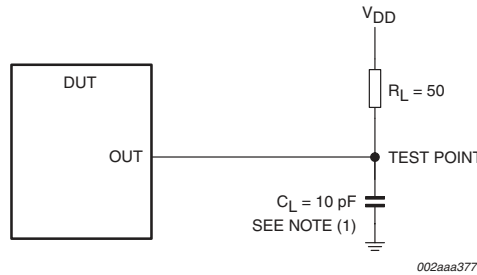Figure 7 — Output Slew-Rate Measurement Information (V_{DD} = 1.8 V ± 0.1 V)

Notes: 1. C_L includes probe and jig capacitance.
 2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10MHz, Z_O = 50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).

Output slew rate measurement information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR $\leq$ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

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(1) C_L includes probe and jig capacitance.
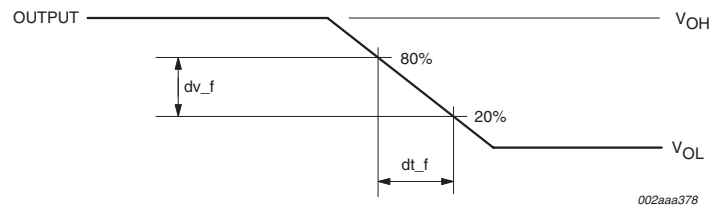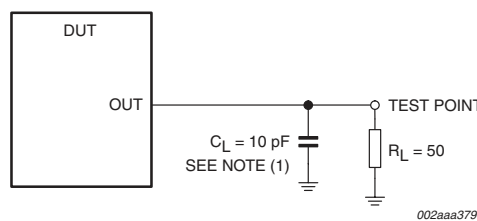
Figure 12 — Load circuit, HIGH-to-LOW slew measurement

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Figure 13 — Voltage waveforms, HIGH-to-LOW slew rate measurement

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(1) C_L includes probe and jig capacitance.

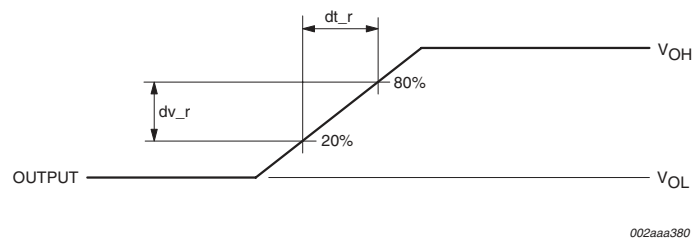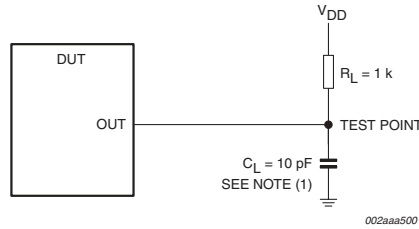**Figure 14 — Load circuit, LOW-to-HIGH slew measurement**

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Figure 15 — Voltage waveforms, LOW-to-HIGH slew rate measurement

Error output load circuit and voltage measurement information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; input slew rate = 1 V/ns ± 20%, unless otherwise specified.

(1) C_L includes probe and jig capacitance.

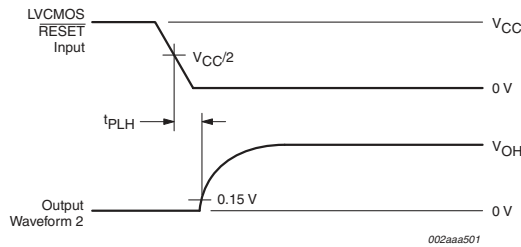**Figure 16 — Load circuit, error output measurements**

Figure 17 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to $\overline{\text{RESET}}$ input
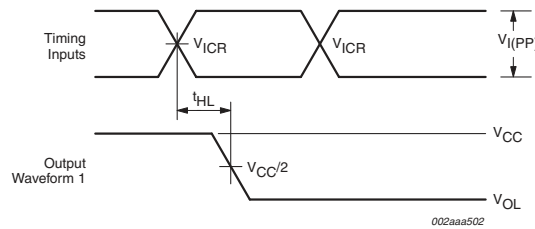

Figure 18 — Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs
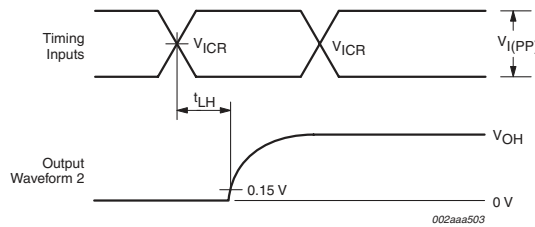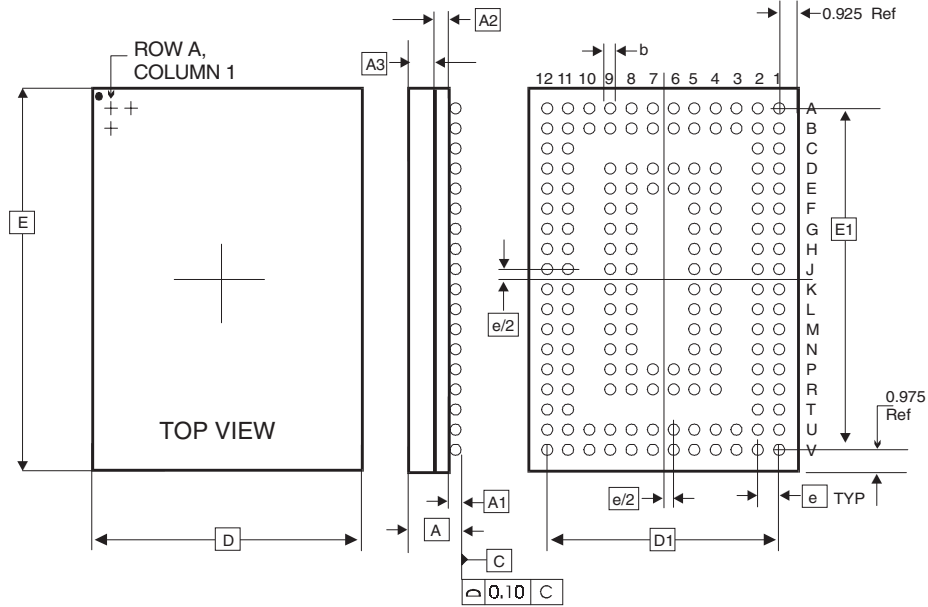

Figure 19 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs

Ball Grid Array (FBGA)
160 Balls, 9x13 mm, 12x18 Pattern

SYMBOL	MILLIMETER			INCH*		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.90	1.05	1.20	0.035	0.041	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.20	0.25	0.30	0.009	0.010	0.012
A3	0.45	0.50	0.55	0.018	0.020	0.022
b	0.35	0.40	0.45	0.014	0.016	0.018
D	9.00 BSC			0.354 BSC		
D1	7.15 BSC			0.281 BSC		
E	13.00 BSC			0.512 BSC		
E1	11.05 BSC			0.435 BSC		
e	0.65 BSC			0.026 BSC		

* For Reference Only. Controlling dimensions in mm.

Ordering Information

ICSSSTUA32S865AH(LF)-T

Example:

ICS XXXX y H (LF)- T

├─ **Designation for tape and reel packaging**

├─ **Annealed Lead Free (Optional)**

├─ **Package Type**
   H = BGA

├─ **Revision Designator** (will not correlate with datasheet revision)

├─ **Device Type**

└─ **Prefix**
   ICS = Standard Device