Dual and Quad 1mA, 12MHz, 50V/μs Op Amps

FEATURES

- **1mA Supply Current per Amplifier**
- 50V/μs Slew Rate
- 12MHz Gain-Bandwidth
- Unity-Gain Stable
- 330ns Settling Time to 0.1%, 10V Step
- 6V/mV DC Gain, R_L = 2kΩ
- 2mV Maximum Input Offset Voltage
- 100nA Maximum Input Offset Current
- 1μA Maximum Input Bias Current
- ±12V Minimum Output Swing into 2kΩ
- Wide Supply Range: ±2.5V to ±15V
- Drives Capacitive Loads

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Video and RF Amplification
- Cable Drivers
- Data Acquisition Systems

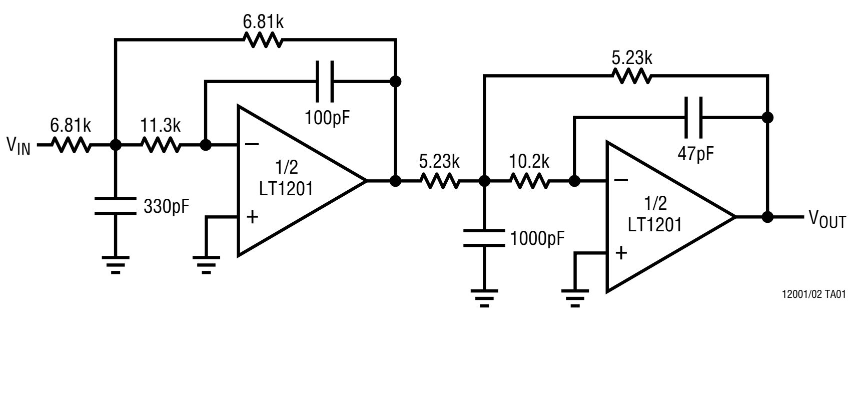
DESCRIPTION

The LT1201/LT1202 are dual and quad low power, high speed operational amplifiers with excellent DC performance. The LT1201/LT1202 feature much lower supply current than devices with comparable bandwidth and slew rate. Each amplifier is a single gain stage with outstanding settling characteristics. The fast settling time makes the circuit an ideal choice for data acquisition systems. Each output is capable of driving a 2kΩ load to ±12V with ±15V supplies and a 500Ω load to ±3V on ±5V supplies. The amplifiers are also capable of driving large capacitive loads which make them useful in buffer or cable driver applications.

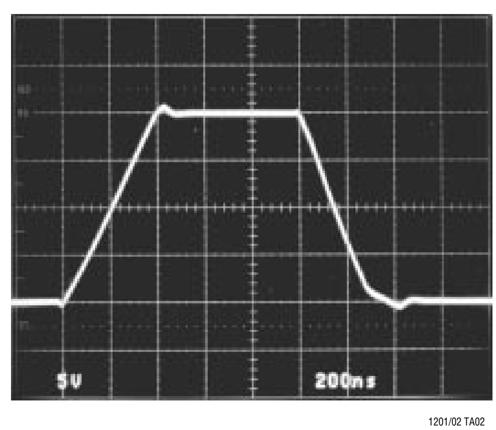
The LT1201/LT1202 are members of a family of fast, high performance amplifiers that employ Linear Technology Corporation's advanced bipolar complementary processing.

TYPICAL APPLICATION

100kHz, 4th Order Butterworth Filter



Inverter Pulse Response



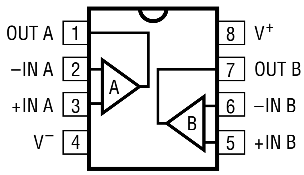
1201/02 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Differential Input Voltage .... ±6V
Input Voltage .... $\pm V_S$
Output Short-Circuit Duration (Note 1) .... Indefinite
Operating Temperature Range
LT1201C/LT1202C .... −40°C to 85°C
Specified Temperature Range (Note 5)
LT1201C/LT1202C .... 0°C to 70°C
Maximum Junction Temperature
Plastic Package .... 150°C
Storage Temperature Range .... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

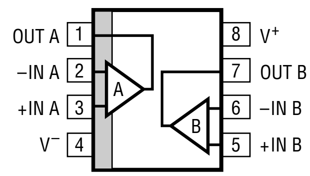


N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1201CN8

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 150°C/W

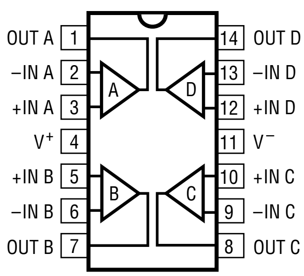
ORDER PART NUMBER

LT1201CS8

S8 PART MARKING

1201

TOP VIEW

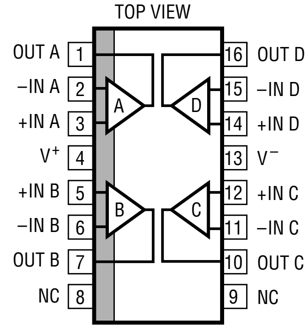


N PACKAGE
14-LEAD PLASTIC DIP
T_{JMAX} = 150°C, θ_{JA} = 70°C/W

ORDER PART NUMBER

LT1202CN

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SOIC
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1202CS

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_S = \pm15V$ (Note 2)		0.7	2.0	mV
		0°C to 70°C			3.0	mV
		$V_S = \pm5V$ (Note 2)		1.0	4.0	mV
		0°C to 70°C			4.5	mV
	Input V_{OS} Drift			11		µV/°C
I_{OS}	Input Offset Current	$V_S = \pm5V$ and $V_S = \pm15V$		50	100	nA
		0°C to 70°C			150	nA
I_B	Input Bias Current	$V_S = \pm5V$ and $V_S = \pm15V$		0.5	1.0	µA
		0°C to 70°C			1.2	µA
e_n	Input Noise Voltage	f = 10kHz		30		$nV/\sqrt{Hz}$
i_n	Input Noise Current	f = 10kHz		0.6		$pA/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS $V_S = \pm15V$, $T_A = 25°C$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_{IN}	Input Resistance	$V_{CM} = \pm12V$	48	90		MΩ
		Differential		500		kΩ
C_{IN}	Input Capacitance			2		pF
CMRR	Common-Mode Rejection Ratio	$V_S = \pm15V$, $V_{CM} = \pm12V$; $V_S = \pm5V$, $V_{CM} = \pm2.5V$	92	100		dB
		0°C to 70°C	90			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm5V$ to $\pm15V$	80	90		dB
		0°C to 70°C	80			dB
	Input Voltage Range$^+$	$V_S = \pm15V$	12.0	14		V
		$V_S = \pm5V$	2.5	4		V
	Input Voltage Range$^-$	$V_S = \pm15V$		–13	–12.0	V
		$V_S = \pm5V$		–3	–2.5	V
A_{VOL}	Large-Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 5k$	4.0	8		V/mV
		0°C to 70°C	3.5			V/mV
		$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 2k$	3.0	6		V/mV
		0°C to 70°C	2.5			V/mV
		$V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 2k$	2.5	5		V/mV
		0°C to 70°C	2.0			V/mV
		$V_S = \pm5V$, $V_{OUT} = \pm2.5V$, $R_L = 1k$	2.0	4		V/mV
		0°C to 70°C	1.6			V/mV
V_{OUT}	Output Swing	$V_S = \pm15V$, $R_L = 2k$, 0°C to 70°C	12.0	13.8		±V
		$V_S = \pm5V$, $R_L = 500\Omega$, 0°C to 70°C	3.0	4.0		±V
I_{OUT}	Output Current	$V_S = \pm15V$, $V_{OUT} = \pm12V$, 0°C to 70°C	6	12		mA
		$V_S = \pm5V$, $V_{OUT} = \pm3V$, 0°C to 70°C	6	12		mA
SR	Slew Rate	$V_S = \pm15V$, $A_{VCL} = -2$ (Note 3)	30	50		V/µs
		0°C to 70°C	27			V/µs
		$V_S = \pm5V$, $A_{VCL} = -2$ (Note 3)	20	33		V/µs
		0°C to 70°C	18			V/µs
	Full Power Bandwidth	$V_S = \pm15V$, 10V Peak (Note 4)		0.8		MHz
		$V_S = \pm5V$, 3V Peak (Note 4)		1.7		MHz
GBW	Gain-Bandwidth	$V_S = \pm15V$, f = 0.1MHz		12		MHz
		$V_S = \pm5V$, f = 0.1MHz		9		MHz
t_r, t_f	Rise Time, Fall Time	$V_S = \pm15V$, $A_{VCL} = 1$, 10% to 90%, 0.1V		18		ns
		$V_S = \pm5V$, $A_{VCL} = 1$, 10% to 90%, 0.1V		23		ns
	Overshoot	$V_S = \pm15V$, $A_{VCL} = 1$, 0.1V		25		%
		$V_S = \pm5V$, $A_{VCL} = 1$, 0.1V		20		%
	Propagation Delay	$V_S = \pm15V$, 50% V_{IN} to 50%V_{OUT}		18		ns
		$V_S = \pm5V$, 50% V_{IN} to 50%V_{OUT}		23		ns
t_s	Settling Time	$V_S = \pm15V$, 10V Step, 0.1%, $A_{VCL} = 1$		330		ns
		$V_S = \pm5V$, 5V Step, 0.1%, $A_{VCL} = 1$		300		ns
R_O	Output Resistance	$A_{VCL} = 1$, f = 0.1MHz		1.1		Ω
	Crosstalk	$V_{OUT} = \pm10V$, $R_L = 2k$		–110	–100	dB
I_S	Supply Current	Each Amplifier, $V_S = \pm5V$ and $V_S = \pm15V$		1	1.4	mA
		0°C to 70°C			1.6	mA

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Input offset voltage is pulse tested with automated test equipment and is exclusive of warm-up drift.

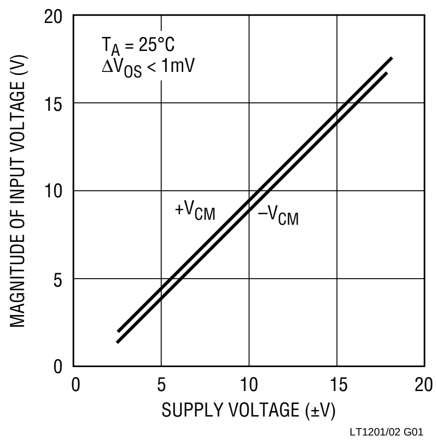
Note 3: Slew rate is measured in a gain of –2. For ±15V supplies measure between ±10V on the output with ±6V on the input. For ±5V supplies measure between ±2V on the output with ±1.75V on the input.

Note 4: Full power bandwidth is calculated from the slew rate measurement: $FPBW = SR/2\pi V_P$.

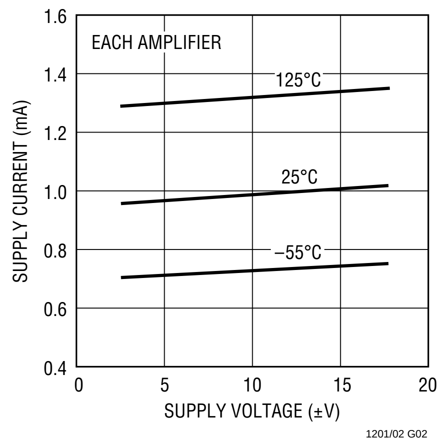
Note 5: Commercial grade parts are designed to operate over the temperature range of –40°C to 85°C but are neither tested nor guaranteed beyond 0°C to 70°C. Industrial grade parts specified and tested over –40°C to 85°C are available on special request. Consult factory.

TYPICAL PERFORMANCE CHARACTERISTICS

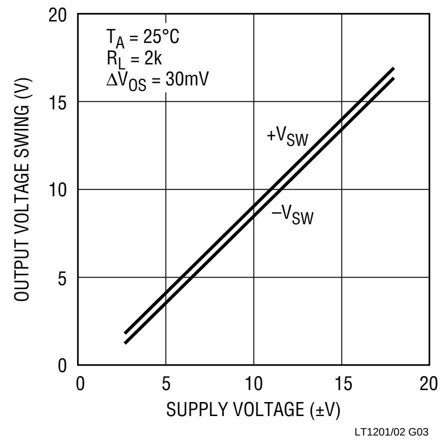
Input Common-Mode Range vs Supply Voltage



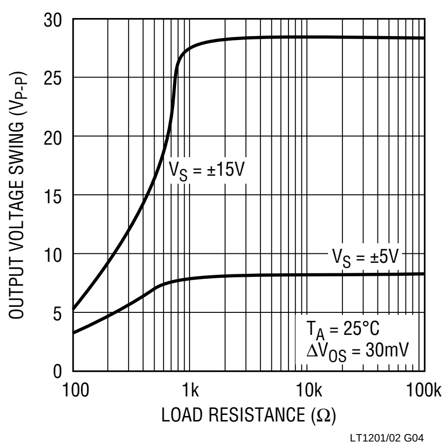
Supply Current vs Supply Voltage



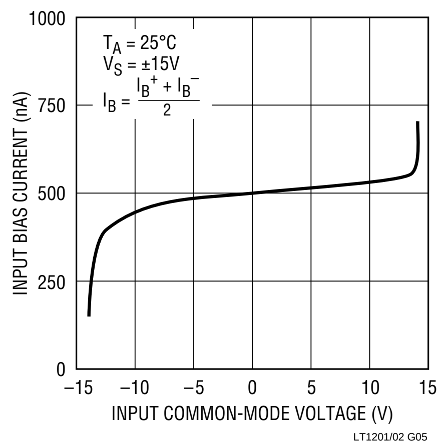
Output Voltage Swing vs Supply Voltage



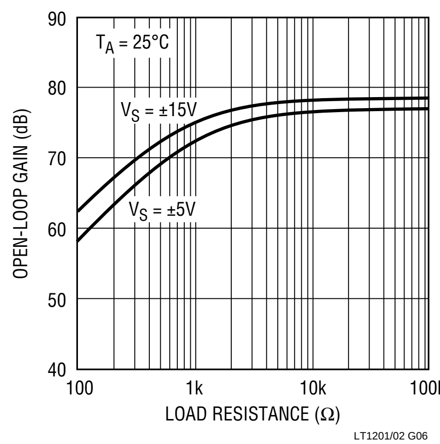
Output Voltage Swing vs Resistive Load



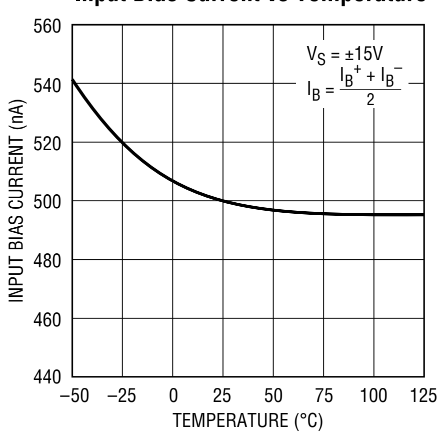
Input Bias Current vs Input Common-Mode Voltage



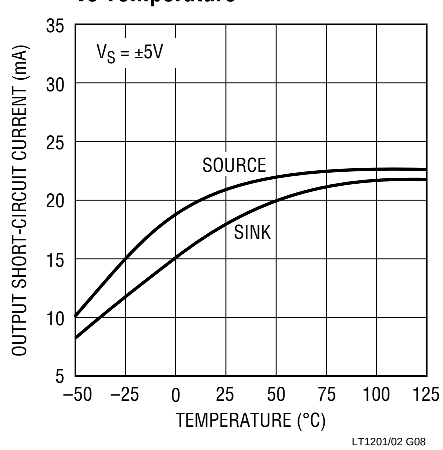
Open-Loop Gain vs Resistive Load



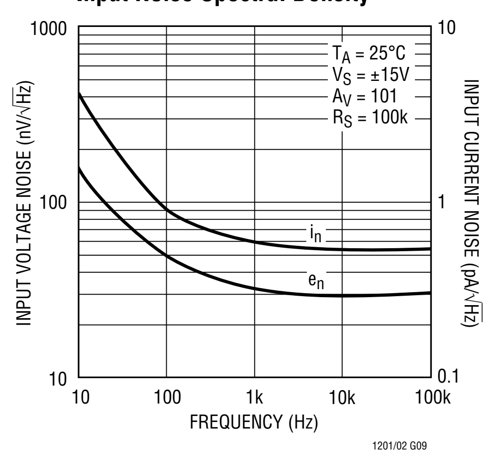
Input Bias Current vs Temperature



Output Short-Circuit Current vs Temperature

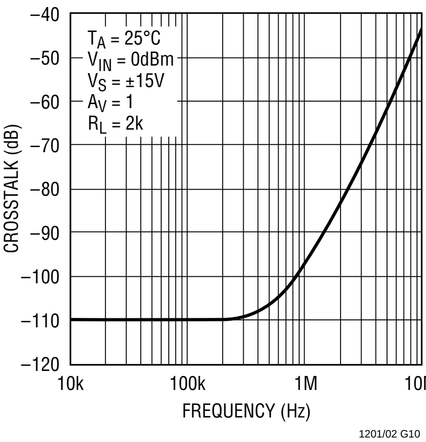


Input Noise Spectral Density

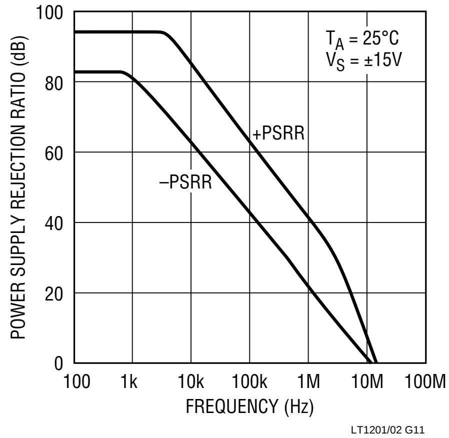


TYPICAL PERFORMANCE CHARACTERISTICS

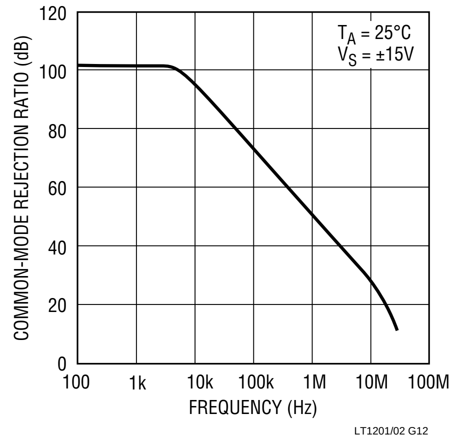
Crosstalk vs Frequency



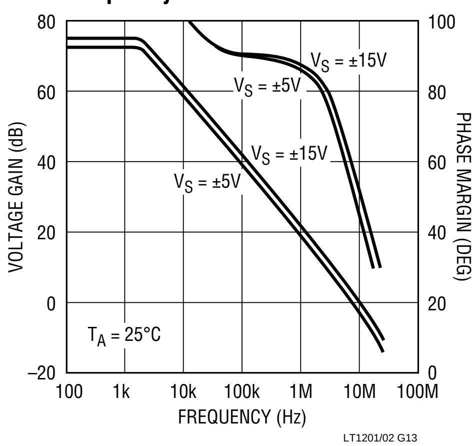
Power Supply Rejection Ratio vs Frequency



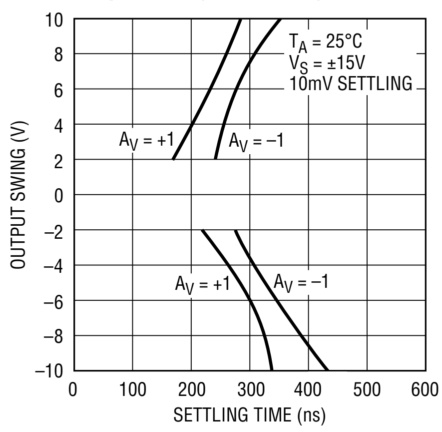
Common-Mode Rejection Ratio vs Frequency



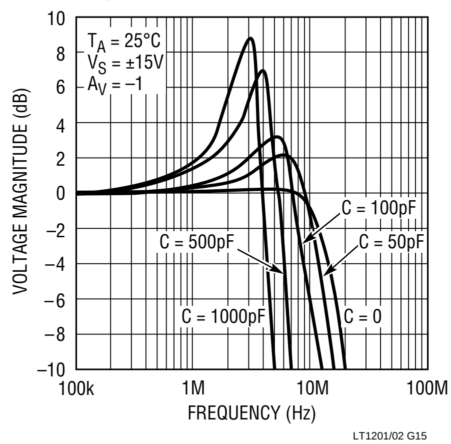
Voltage Gain and Phase vs Frequency



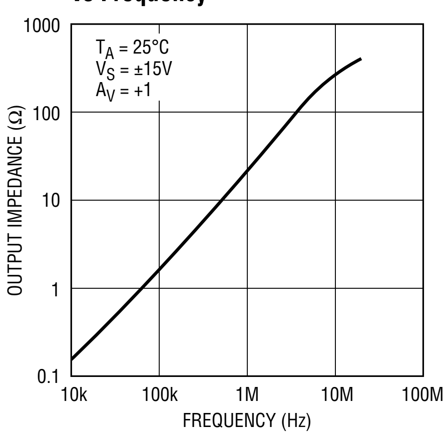
Output Swing vs Settling Time



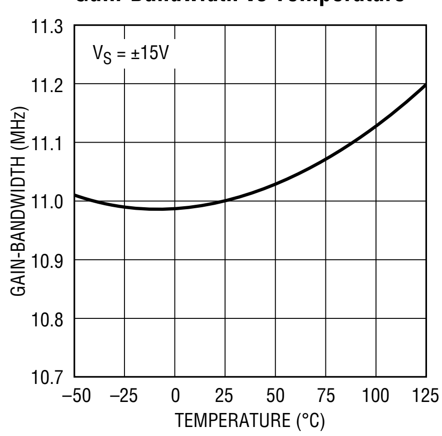
Frequency Response vs Capacitive Load



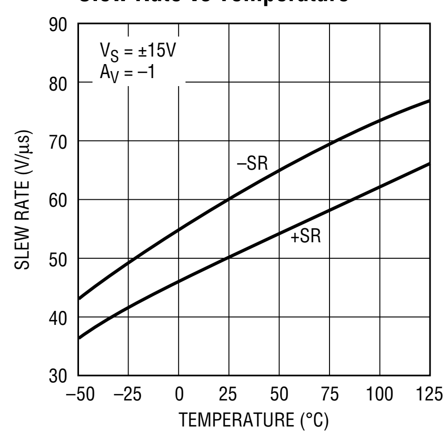
Closed-Loop Output Impedance vs Frequency



Gain-Bandwidth vs Temperature

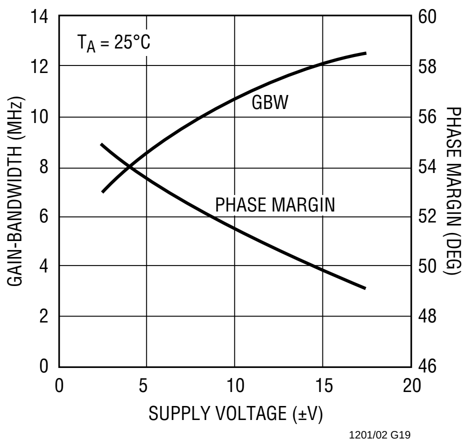


Slew Rate vs Temperature

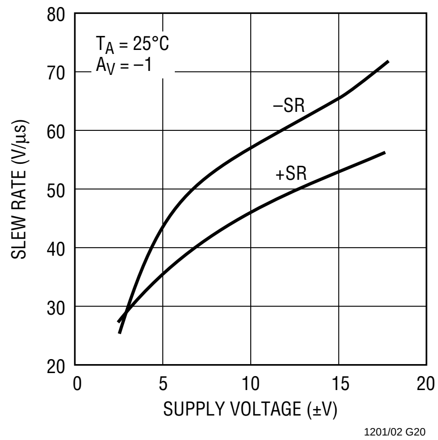


TYPICAL PERFORMANCE CHARACTERISTICS

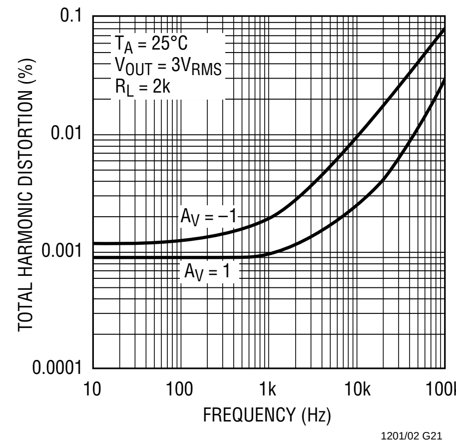
Gain-Bandwidth and Phase Margin vs Supply Voltage



Slew Rate vs Supply Voltage



Total Harmonic Distortion vs Frequency



APPLICATIONS INFORMATION

Layout and Passive Components

As with any high speed operational amplifier, care must be taken in board layout in order to obtain maximum performance. Key layout issues include: use of a ground plane, minimization of stray capacitance at the input pins, short lead lengths, RF-quality bypass capacitors located close to the device (typically 0.01µF to 0.1µF) and low ESR bypass capacitors for high drive current applications (typically 1µF to 10µF tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50. The parallel combination of the feedback resistor and gain setting resistor on the inverting input combine with the input capacitance to form a pole which can cause peaking. If feedback resistors greater than 5k are used, a parallel capacitor of value:

$$C_F \geq R_G \times C_{IN}/R_F$$

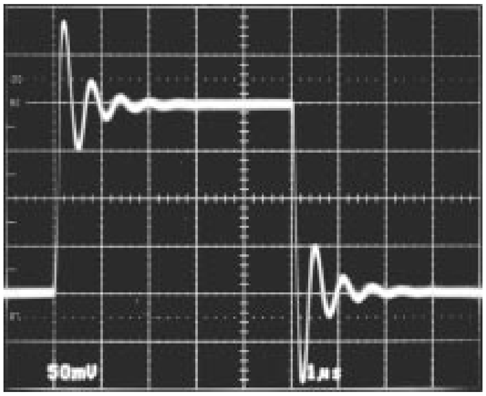
should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN}.

Capacitive Loading

The LT1201/LT1202 amplifiers are stable with all capacitive loads. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response. The photo of the small-signal response with 1000pF load shows 40% peaking. The large-signal response with a 10,000pF load shows the output slew rate being limited by the short-circuit current. To reduce peaking with capacitive loads, insert a small decoupling resistor between the output and the load, and add a capacitor between the output and inverting input to provide an AC feedback path. Coaxial cable can be driven directly, but for best pulse fidelity the cable should be doubly terminated with a resistor in series with the output. When driving a 150Ω load the minimum output current of 6mA limits the swing to ±0.9V.

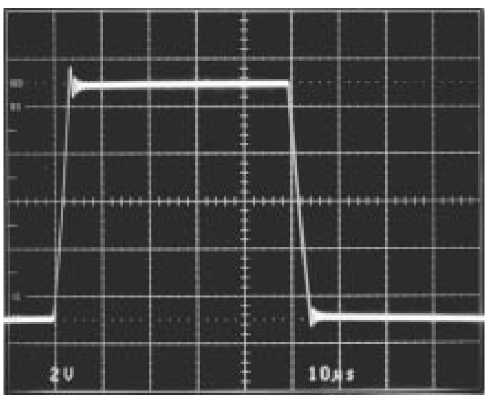
APPLICATIONS INFORMATION

Small-Signal Capacitive Loading



$A_V = -1$
$C_L = 1000pF$
1201/02 AI01

Large-Signal Capacitive Loading



$A_V = 1$
$C_L = 10,000pF$
1201/02 AI02

Input Considerations

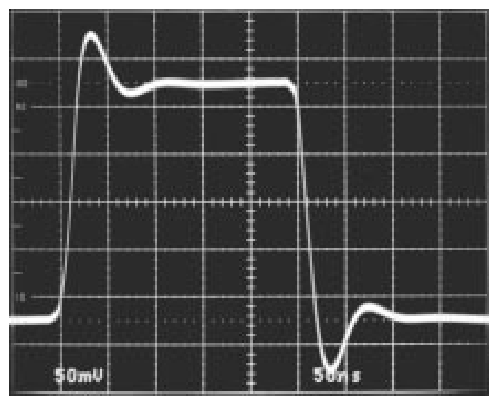
Resistors in series with the inputs are recommended for the LT1201/LT1202 in applications where the differential input voltage exceeds ±6V continuously or on a transient basis. An example would be in noninverting configurations with high input slew rates or when driving heavy capacitive loads. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized.

Transient Response

The LT1201/LT1202 gain-bandwidth is 12MHz when measured at 100kHz. The actual frequency response in unity-gain is considerably higher than 12MHz due to peaking caused by a second pole beyond the unity-gain crossover. This is reflected in the 50° phase margin and shows up as overshoot in the unity-gain small-signal transient response. Higher noise gain configurations exhibit less overshoot as seen in the inverting gain of one response.

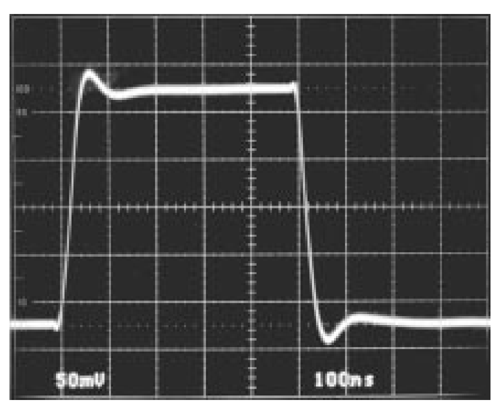
The large-signal response in both inverting and noninverting gain shows symmetrical slewing characteristics. Normally the noninverting response has a much faster rising edge due to the rapid change in input common-mode voltage which affects the tail current of the input differential pair. Slew enhancement circuitry has been added to the LT1201/LT1202 so that the falling edge slew rate is balanced.

Small-Signal Transient Response



$A_V = 1$
1201/02 AI03

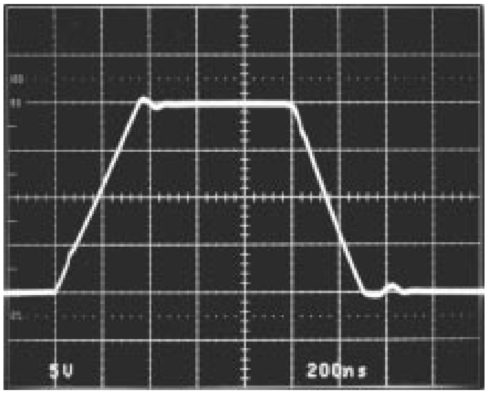
Small-Signal Transient Response



$A_V = -1$
1201/02 AI04

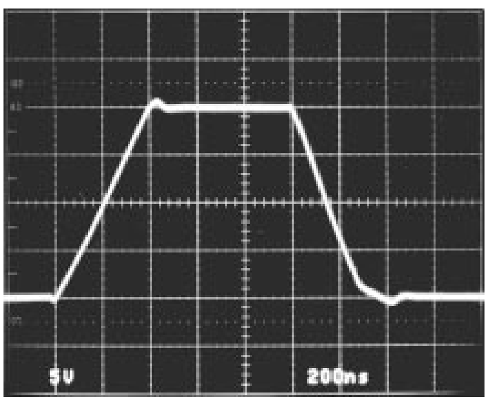
APPLICATIONS INFORMATION

Large-Signal Transient Response



$A_V = 1$ 1201/02 AI05

Large-Signal Transient Response



$A_V = -1$ 1201/02 AI06

Low Voltage Operation

The LT1201/LT1202 are functional at room temperature with only 3V of total supply voltage. Under this condition, however, the undistorted output swing is only $0.8V_{P-P}$. A more realistic condition is operation at ±2.5V supplies (or 5V and ground). Under these conditions at room temperature the typical input common-mode range is 2.2V to –1.5V, and a 1MHz, $2.5V_{P-P}$ sine wave can be accurately reproduced. With 5V total supply voltage the gain-bandwidth is reduced to 7MHz and the slew rate is reduced to 20V/µs.

DAC Current-to-Voltage Converter

The wide bandwidth, high slew rate and fast settling time of the LT1201/LT1202 make them well suited for current-to-voltage conversion after current output D/A converters. A typical application with a DAC-08 type converter (full-scale output of 2mA) uses a 5k feedback resistor. A 12pF compensation capacitor across the feedback resistor is used to null the pole at the inverting input caused by the DAC output capacitance. The combination of the LT1201/LT1202 and DAC settles to less than 40mV (1LSB) in 500ns for a 0V to 10V step or for a 10V to 0V step.

Active Filters

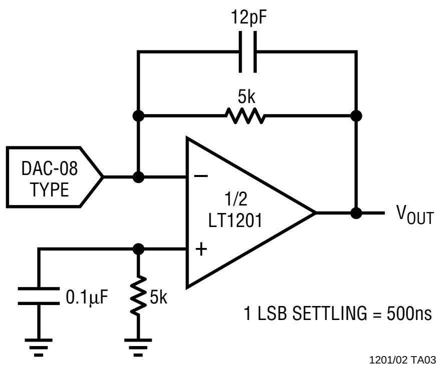
The LT1201/LT1202 are well suited to active filter applications such as the circuit shown on the front page of the data sheet. This particular example is a 4-pole Butterworth lowpass filter with a cutoff frequency of 100kHz. In choosing an amplifier for filter applications a good rule of thumb is:

$$f_O \times Q < GBW/20$$

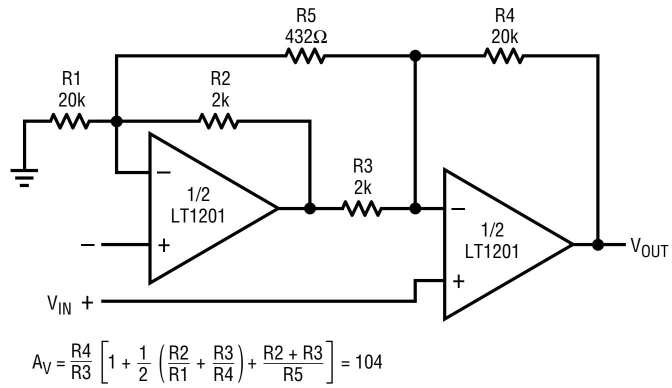
For our example the first section has Q = 0.54 and the second section has Q = 1.31, so the amplifier easily meets the gain-bandwidth requirement of 2.6MHz for f_O = 100kHz. This multiple feedback configuration and the Sallen-Key configuration (as shown in the Typical Applications section) are the most commonly used topologies. The multiple feedback configuration has an advantage over the noninverting Sallen-Key configuration in many cases because the amplifier does not see a frequency varying common-mode voltage and high frequency output impedance is not critical. The result is better frequency performance beyond f_O (for our particular example the stopband performance is dramatically better above 1MHz). Advantages of the Sallen-Key topology over the multiple feedback topology include: better gain accuracy, better DC accuracy, and unity-gain filters can be implemented more easily.

TYPICAL APPLICATIONS

DAC Current-to-Voltage Converter



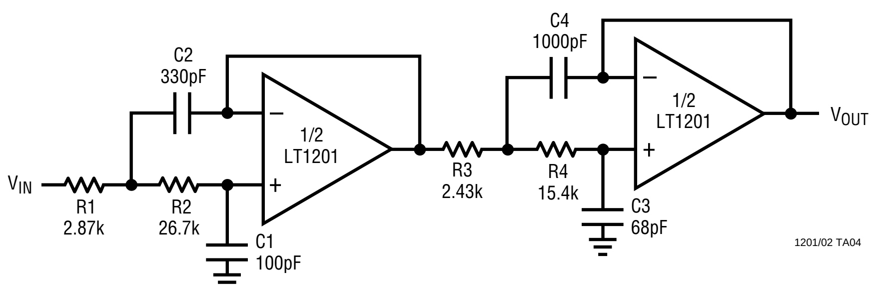
Instrumentation Amplifier



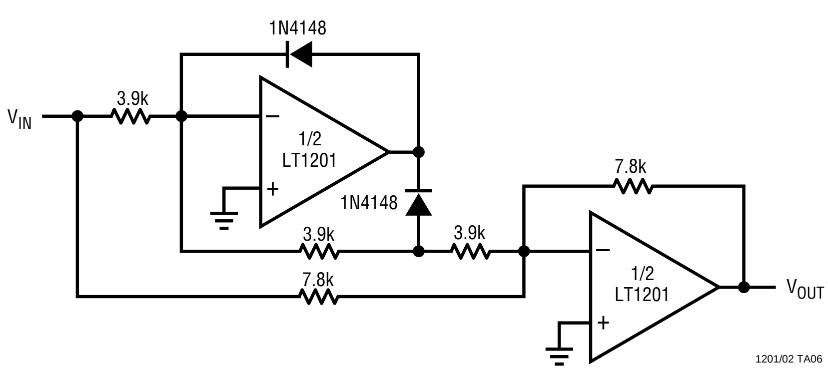
$$A_V = \frac{R4}{R3}\left[1 + \frac{1}{2}\left(\frac{R2}{R1} + \frac{R3}{R4}\right) + \frac{R2 + R3}{R5}\right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 120kHz

100kHz 4th Order Butterworth Filter (Sallen-Key)

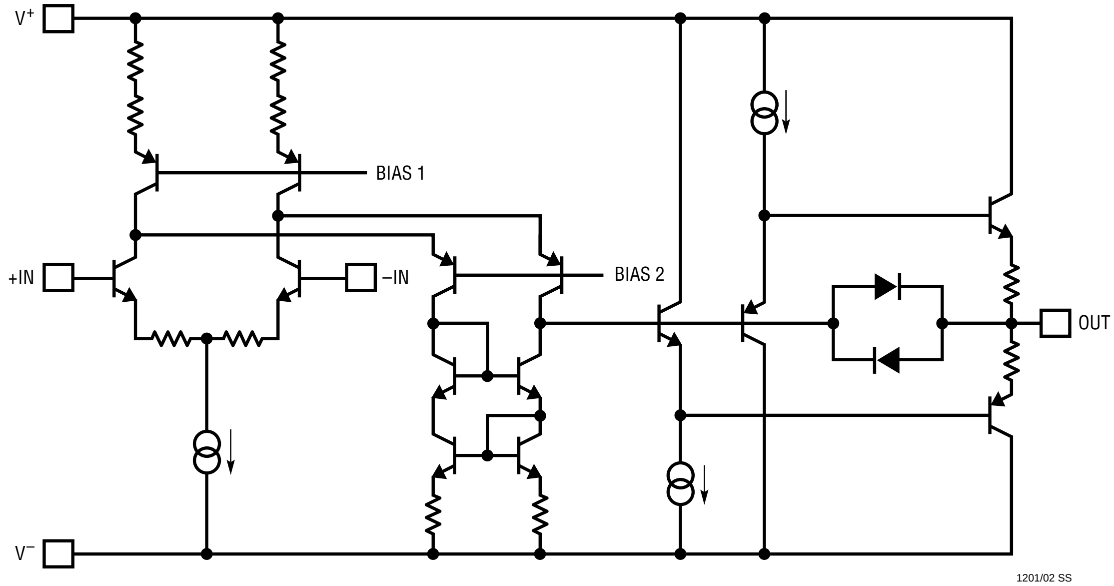


Full-Wave Rectifier



SIMPLIFIED SCHEMATIC

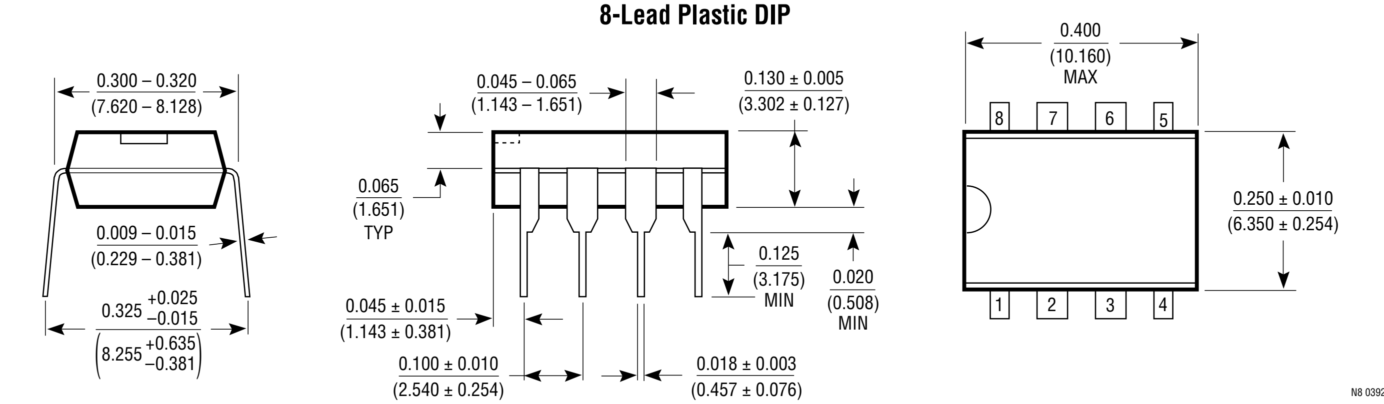
One amplifier shown.



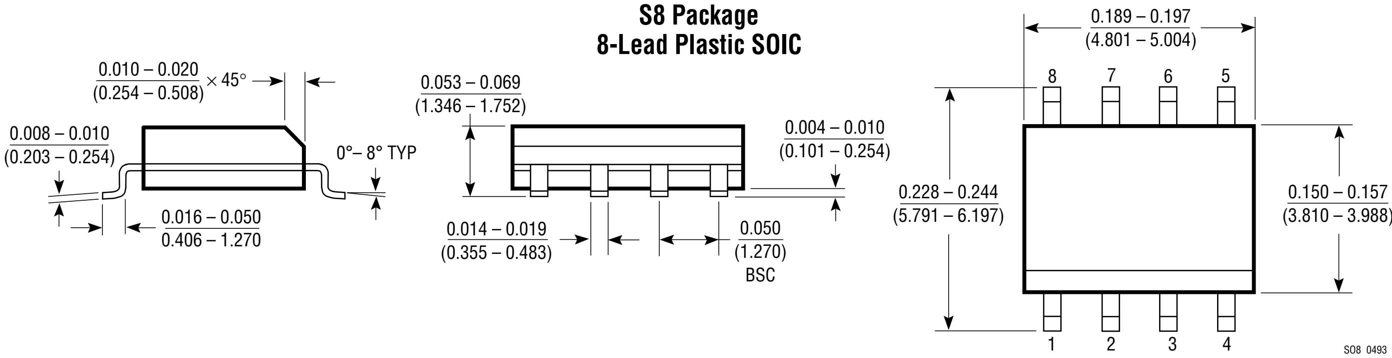
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP

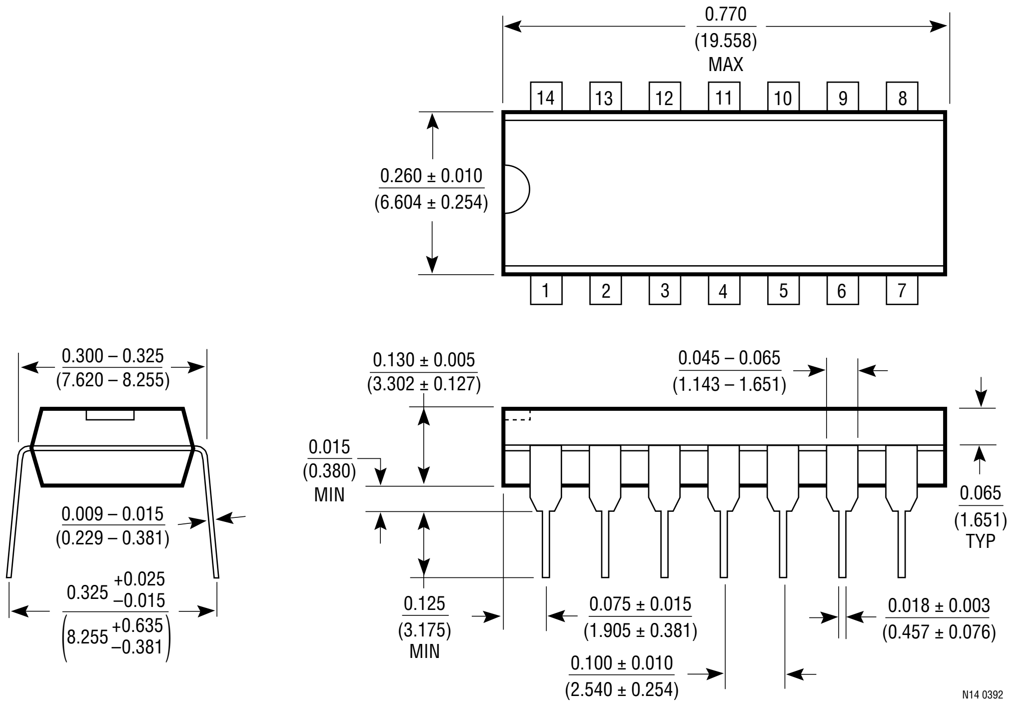


S8 Package
8-Lead Plastic SOIC

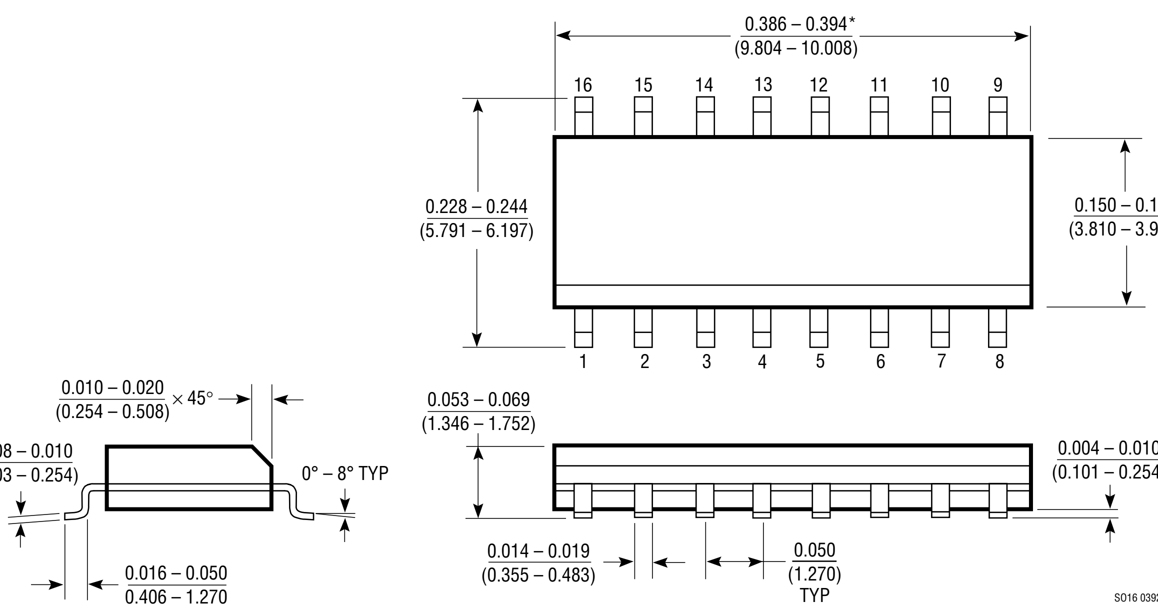


PACKAGE DESCRIPTION Dimensions in inches (millimeters) unless otherwise noted.

N Package
14-Lead Plastic DIP



S Package
16-Lead Plastic SOIC



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).

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