

CMOS 8-BIT MICROCONTROLLERS

TMP91P640N - 10 / TMP91P640F - 10

1. OUTLINE AND CHARACTERISTICS

The TMP91P640 is a system evaluation LSI having a built in One-Time PROM for TMP91C640.

A programming and verification for the internal PROM is achieved by using a general EPROM programmer with an adapter socket.

The function of this device is exactly same as the TMP91C640 or TMP90C840A by programming to the internal PROM.

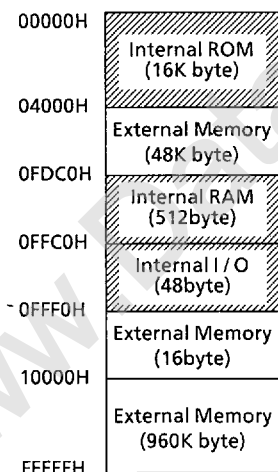
The different points between TMP91P640 and TMP90C840A are the memory size (ROM/RAM) and maximum operating frequency.

The operating frequency range of TMP91P640 is from 1MHz to 10MHz, against that of TMP91C640/TMP90C840A is from 1MHz to 12.5MHz.

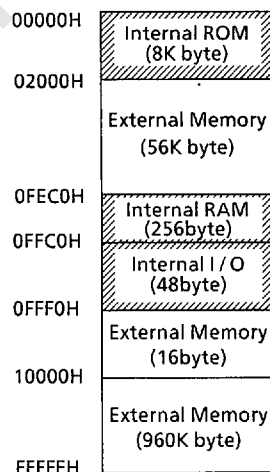
The TMP91P640N-10 is in a Shrink Dual Inline Package (SDIP64-P-750).

The TMP91P640F-10 is in a Quad Flat Package (QFP64-P-1420A).

The following are the memory map of TMP91C640 and TMP90C840A.



TMP91C640 Memory Map

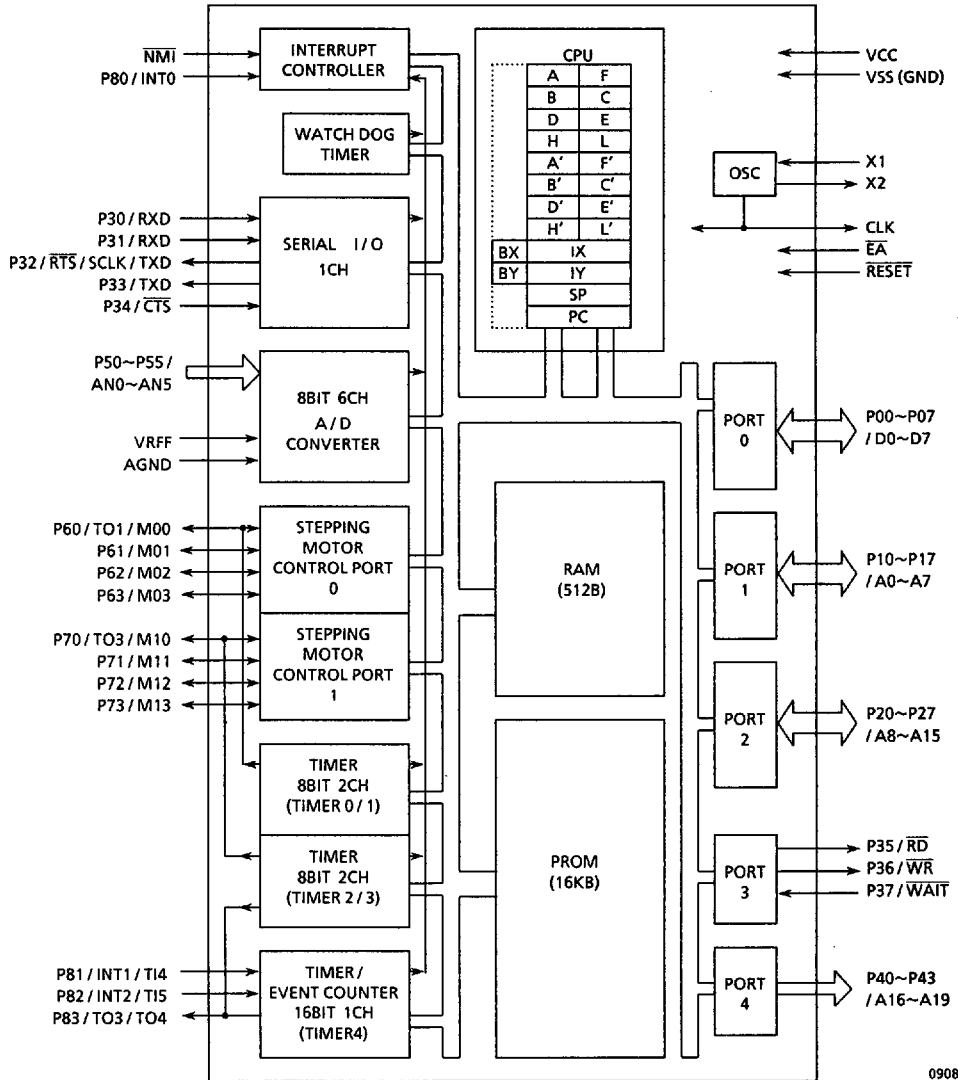


TMP90C840A Memory Map

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PARTS NO.	ROM	RAM	PACKAGE	ADAPTER SOCKET NO.
TMP91P640N-10	OTP 16384 x 8bit	512 x 8bit	64-SDIP	BM1115A
TMP91P640F-10			64-FP	BM1116A

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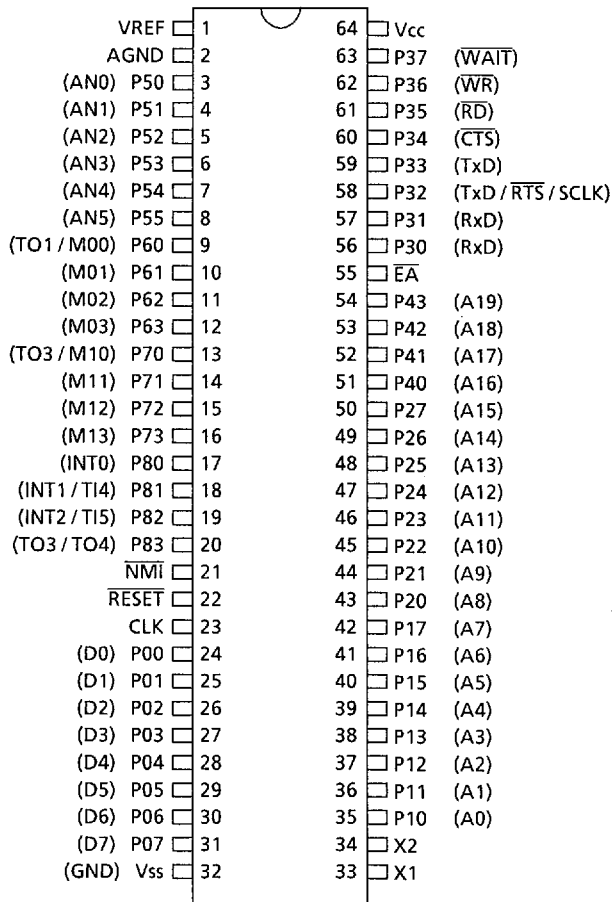
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Figure 1 TMP91P640-10 Block Diagram

## 2. PIN ASSIGNMENT AND FUNCTIONS

### 2.1 Pin Assignment

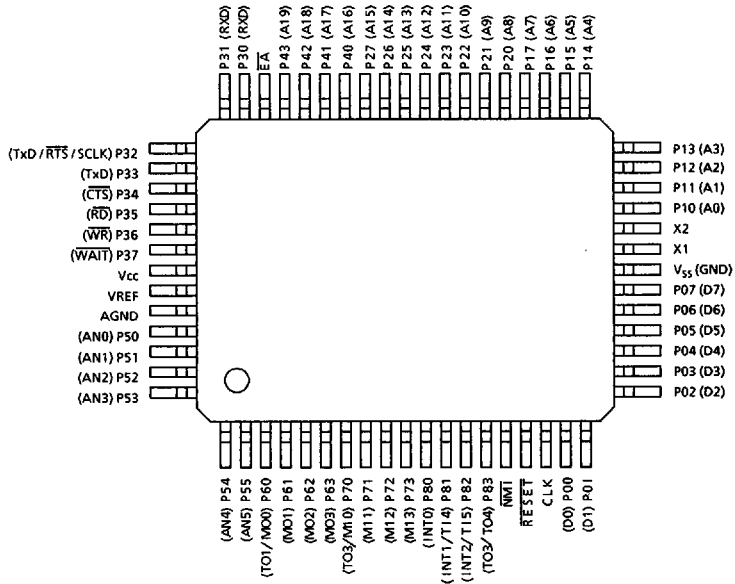
Figure 2.1 (1) shows pin assignment of the TMP91P640N-10.



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Figure 2.1 (1) Pin Assignment (64-SDIC / SDIP)

Figure 2.1 (2) shows pin assignment of the TMP91P640F-10.



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Figure 2.1 (2) Pin Assignment (64-FP)

## 2.2 Pin Names and Functions

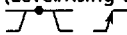


The TMP91P640 has MCU mode and PROM mode.

## (1) MCU Mode (The TMP91C640 and the TMP91P640 are pin compatible)

Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O 3 states	Function
P00~P07 /D0~D7	8	I/O	Port 0: 8-bit I/O port that allows selection of input/output on byte basis
		3 states	Data bus: Also functions as 8-bit bidirectional data bus for external memory
P10~P17 /A0~A7	8	I/O	Port 1: 8-bit I/O port that allows selection on byte basis
		Output	Address bus: The lower 8 bits address bus for external memory
P20~P27 /A8~A15	8	I/O	Port 2: 8-bit I/O port that allows selection on bit basis
		Output	Address bus: The upper 8 bits address bus for external memory
P30 /RxD	1	Input	Port 30: 1-bit input port
			Receiver Serial Data
P31 /RxD	1	Input	Port 31: 1-bit input port
			Receiver Serial Data
P32 /TxD /RTS /SCLK	1	Output	Port 32: 1-bit output port
			Transmitter serial Data
			Request to send serial data
			Serial clock output
P33 /TxD	1	Output	Port 33: 1-bit output port
			Transmitter Serial Data
P34 /CTS	1	Input	Port 34: 1-bit input port
			Clear to send Serial data
P35 /RD	1	Output	Port 35: 1-bit output port
			Read: Generates strobe signal for reading external memory
P36 /WR	1	Output	Port 36: 1-bit output port
			Write: Generates strobe signal for writing into external memory
P37 /WAIT	1	Input	Port 37: 1-bit input port
			Wait: Input pin for connecting slow speed memory or peripheral LSI
P40~P43 /A16~A19	4	Output	Port 4: 4-bit output port that allows selection of Port/Address Bus on bit basis
			Address bus: Also functions as address bus for external memory (4 bits of bank address)
P50~P55 /AN0~AN5	6	Input	Port 5: 6-bit input port
			Analog input: 6 analog inputs to A/D converter

## Pin Names and Functions (2/2)

Pin Name	No. of pins	I/O 3 states	Function
VREF	1		Input of reference voltage to A/D converter
AGND	1		Ground pin for A/D converter
P60~P63 /M00~M03 /TO1	4	I/O Output Output	Port 6: 4-bit I/O port that allows I/O selection on bit basis Stepping motor control port 0 Timer output 1: Output of Timer 0 or 1
P70~P73 /M10~M13 /TO3	4	I/O Output Output	Port 7: 4-bit I/O port that allows I/O selection on bit basis Stepping motor control port 1 Timer output 3: Output of Timer 2 or 3
P80 /INT0	1	Input	Port 80: 1-bit input port Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable) 
P81 /INT1 /TI4	1	Input	Port 81: 1-bit input port Interrupt request pin 1: interrupt request pin (Rising/falling edge is programmable)  Timer input 4: Counter/capture trigger signal for Timer 4
P82 /INT2 /TI5	1	Input	Port 82: 1-bit input port Interrupt request pin 2: rising edge interrupt request pin Timer input 5: capture trigger signal for Timer 4
P83 /TO3/TO4	1	Output	Port 83: 1-bit output port Timer output 3/4: Output of Timer 2, 3 or 4
NMI	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin 
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
EA	1	Input	External access: Connects with Vcc pin using internal ROM, and with GND pin not using internal ROM.
RESET	1	Input	Reset : Initializes the LSI. (Built in pull-up resistor)
X1/X2	2	Input/ Output	Pin for quartz crystal or ceramic resonator
Vcc	1		Power supply (+ 5V)
Vss (GND)	1		Ground (0V)

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## (2) PROM Mode

Table 2.1

Pin Function Name	No. of pins	I/O	Function	Pin Name (MCU mode)
A7~A0	8	Input	Address Input	P17~P10
A13~A8	6	Input		P25~P20
A14	2	Input	Befixed to "L" level.	P26
A15				P27
D7~D0	8	I/O	Data Input/Output	P07~P00
$\overline{OE}$	1	Input	Output Enable Input	P35
$\overline{CE}$	1	Input	Chip Enable Input	P36
VPP	1	Power Supply	12.5V / 5V (Programming Power Supply)	E $\overline{A}$
VCC	1	Power Supply	5V	VCC
VSS	1	Power Supply	0V	VSS
Pin Name	No. of pins	I/O	Pin Setting	
P30, P31	2	Input	Be fixed to "L" level.	
P32, P33	2	Output	Open	
P34, P37	2	Input	Be fixed to "L" level.	
P43~P40	4	Output	Open	
P55~P50	6	Input	Be fixed to "L" level.	
P63~P60	4			
P73~P70	4			
P82~P80	3			
P83	1	Output	Open	
VREF	1		Be fixed to "L" level.	
AGND	1		Be fixed to "L" level.	
$\overline{RESET}$	1	Input	Be fixed to "L" level.	
CLK	1	Input	Be fixed to "L" level.	
$\overline{NMI}$	1	Input	Be fixed to "H" level.	
X1	1	Input	Resonator connection pin	
X2	1	Output		

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### 3. OPERATION

The TMP91P640 is the OTP version of the TMP91C640 that is replaced an internal ROM from Mask ROM to One-Time PROM.

The function of TMP91P640 is exactly same as that of TMP90C840A except the internal ROM/RAM size.

Refer to the TMP90C840A except the functions which are not described this section.

The following is an explanation of the hardware configuration and operation in relation to the TMP91P640.

The TMP91P640 has an MCU mode and a PROM mode.

#### 3.1 MCU Mode

##### (1) Mode Setting and Function

The MCU mode is set by opening the CLK pin (Output status).

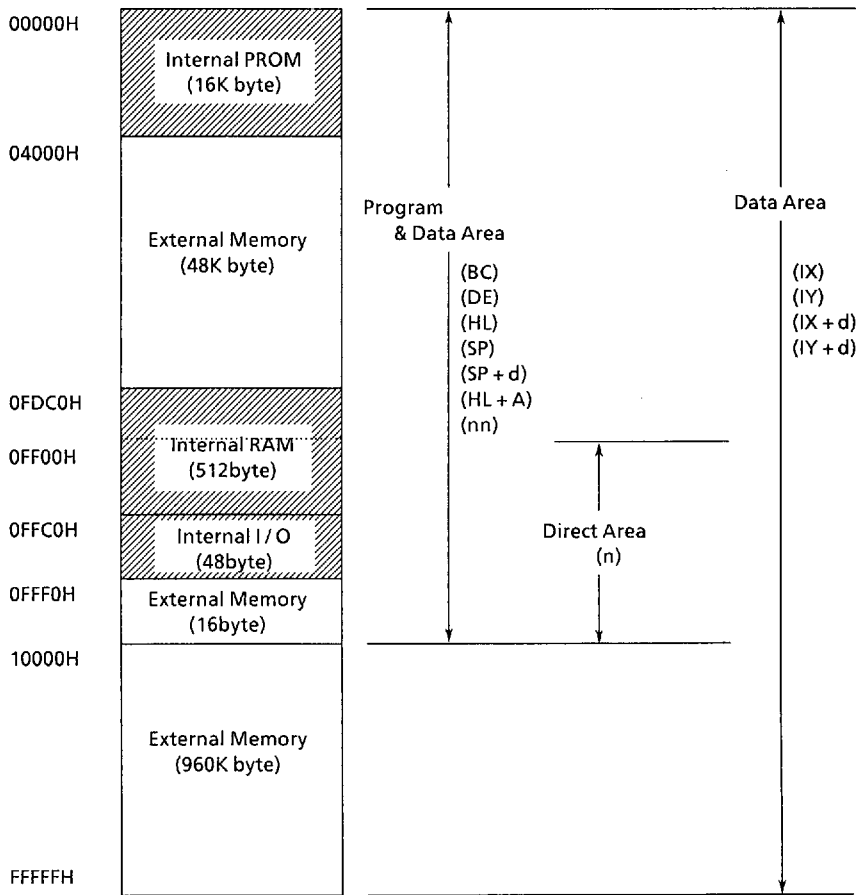
In the MCU mode, the operation is same as that of TMP91C640.

##### (2) Memory Map

The memory map is same as that of TMP91C640.

Figure 3.1 shows the memory map of TMP91P640, and the accessing area by the respective addressing mode.





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Figure 3.1 TMP91P640 Memory Map

3.2 PROM Mode

(1) Mode Setting and Function

PROM mode is set by setting the  $\overline{\text{RESET}}$  and CLK pins to the "L" level.

The programming and verification for the internal PROM is achieved by using a general EPROM programmer with the adaptor socket. The device selection (ROM Type) should be "27256" with following conditions.

size : 256Kbit (32K×8bit) VPP : 12.5V TPW : 1ms

The TMP91P640-10 is not supported an electric signature mode.

Figure 3.2 shows the setting of pins in PROM mode.

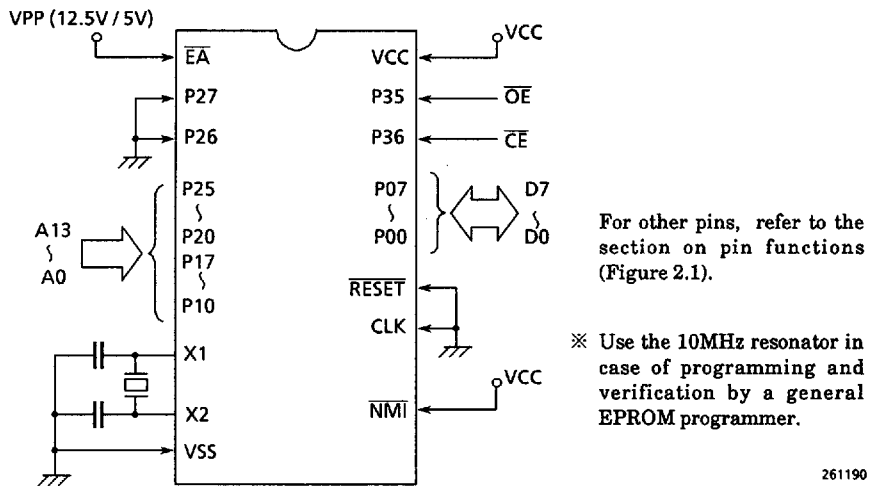


Figure 3.2 PROM Mode Pin Setting

(2) Programming Flow Chart

The programming mode is set by applying 12.5V (programming voltage) to the VPP pin when the following pins are set as follows,

( Vcc : 6.0V  
 $\overline{\text{RESET}}$  : "L" level  
 CLK : "L" level )

\* These conditions can be obtained by using adaptor socket.

After the address and data have been fixed, a data on the Data Bus is programmed when the  $\overline{\text{CE}}$  pin is set to "Low" (1ms plus is required).

General programming procedure of an EPROM programmer is as follows,

- Write a data to a specified address for 1ms.
- Verify the data. If the read-out data does not match the expected data, another writing is performed until the correct data is written (Max. 25 times).

After the correct data is written, an additional writing is performed by using three times longer programming pulse width (1ms×programming times), or using three times more programming pulse number. Then, verify the data and increment the address.

The verification for all data is done under the condition of  $V_{pp}=V_{cc}=5V$  after all data were written.

Figure 3.3 shows the programming flow chart.

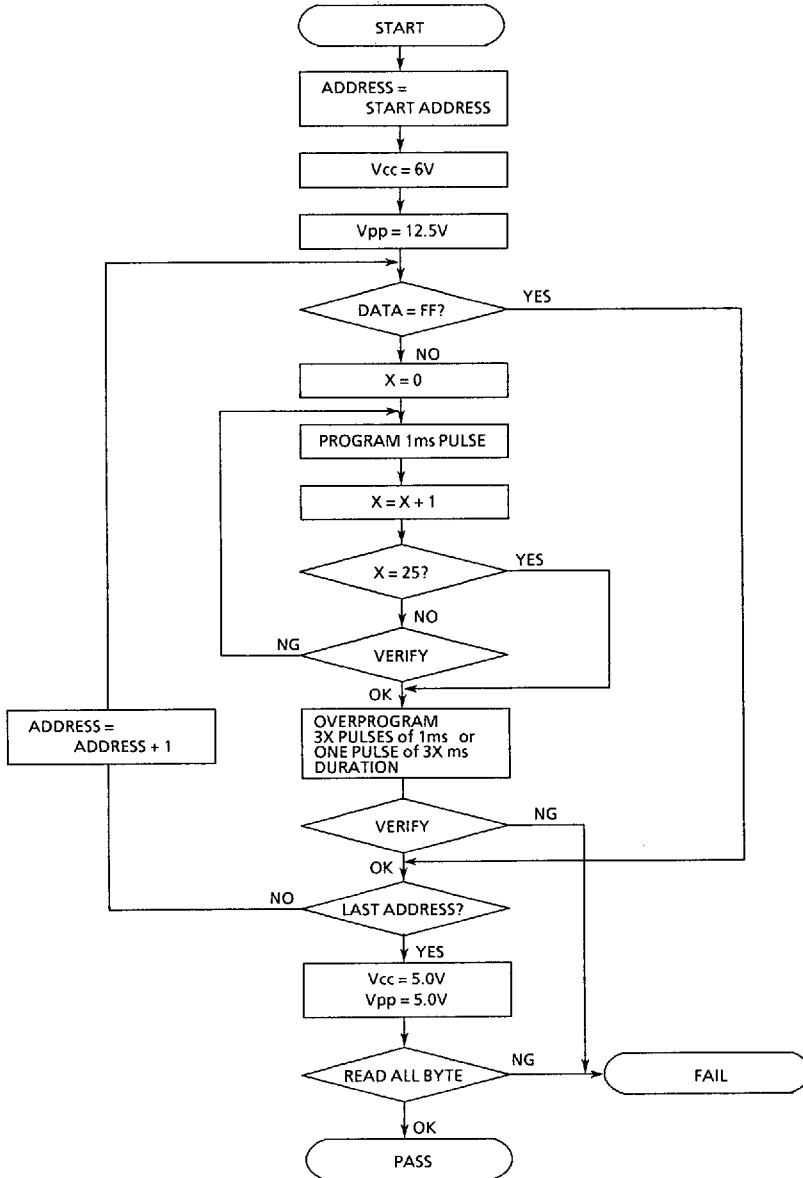


Figure 3.3 Flow Chart

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## 4. ELECTRICAL CHARACTERISTICS

## TMP91P640N-10/TMP91P640F-10

## 4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>CC</sub>	Supply voltage	-0.5~+7	V
V <sub>IN</sub>	Input voltage	-0.5~V <sub>CC</sub> +0.5	V
P <sub>D</sub>	Power dissipation (Ta = 85°C)	F 500 N 600	mW
T <sub>SOLDER</sub>	Soldering temperature (10 s)	260	°C
T <sub>STG</sub>	Storage temperature	-65 ~ 150	°C
T <sub>OPR</sub>	Operating temperature	-40 ~ 85	°C

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## 4.2 DC Characteristics

V<sub>CC</sub> = 5V ± 10% TA = -40~85°C (1~10MHz)Typical Values are for TA = 25°C and V<sub>CC</sub> = 5V.

Symbol	Parameter	Min	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage (P0)	-0.3	0.2V <sub>CC</sub> - 0.1	V	
V <sub>IL1</sub>	P1, P2, P3, P4, P5, P6, P7, P8	-0.3	0.3V <sub>CC</sub>	V	
V <sub>IL2</sub>	RESET, INTO (P80), NMI	-0.3	0.25V <sub>CC</sub>	V	
V <sub>IL3</sub>	EA	-0.3	0.3	V	
V <sub>IL4</sub>	X1	-0.3	0.2V <sub>CC</sub>	V	
V <sub>IH</sub>	Input High Voltage (P0)	0.2V <sub>CC</sub> + 1.1	V <sub>CC</sub> + 0.3	V	
V <sub>IH1</sub>	P1, P2, P3, P4, P5, P6, P7, P8	0.7V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V	
V <sub>IH2</sub>	RESET, INTO (P80), NMI	0.75V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V	
V <sub>IH3</sub>	EA	V <sub>CC</sub> - 0.3	V <sub>CC</sub> + 0.3	V	
V <sub>IH4</sub>	X1	0.8V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 1.6mA
V <sub>OH</sub> V <sub>OH1</sub> V <sub>OH2</sub>	Output High Voltage	2.4 0.75V <sub>CC</sub> 0.9V <sub>CC</sub>		V V V	I <sub>OH</sub> = -400μA I <sub>OH</sub> = -100μA I <sub>OH</sub> = -20μA
I <sub>DAR</sub>	Darlington Drive Current (8 I/O pins)	-1.0	-3.5	mA	V <sub>EXT</sub> = 1.5V R <sub>EXT</sub> = 1.1 kΩ
I <sub>LI</sub>	Input Leakage Current	0.02 (Typ)	±5	μA	0.0 ≤ V <sub>in</sub> ≤ V <sub>CC</sub>
I <sub>LO</sub>	Output Leakage Current	0.05 (Typ)	±10	μA	0.2 ≤ V <sub>in</sub> ≤ V <sub>CC</sub> - 0.2
I <sub>CC</sub>	Operating Current (RUN) Idle 1 Idle 2	20 (Typ) 1.5 (Typ) 9 (Typ)	40 5 15	mA mA mA	fosc = 10MHz
	STOP (TA = -40~85°C) STOP (TA = 0~50°C)	0.2 (Typ)	50 10	μA μA	0.2 ≤ V <sub>in</sub> ≤ V <sub>CC</sub> - 0.2
V <sub>STOP</sub>	Power Down Voltage (@STOP) RAM BACK UP	2	6	V	V <sub>IL2</sub> = 0.2V <sub>CC</sub> , V <sub>IH2</sub> = 0.8V <sub>CC</sub>
R <sub>RST</sub>	RESET Pull Up Resistor	50	150	kΩ	
C <sub>IO</sub>	Pin Capacitance		10	pF	testfreq = 1MHz
V <sub>TH</sub>	Schmitt width RESET, NMI, INTO	0.4	1.0 (Typ)	V	

Note : I<sub>DAR</sub> is guaranteed for a total of up to 8 optional ports.

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## 4.3 AC Characteristics

$V_{CC} = 5V \pm 10\%$   $T_A = -40 \sim 85^\circ\text{C}$  (1~10MHz)  
 $CL = 50\text{pF}$

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t <sub>OSC</sub>	OSC. Period = x	100	1000	100		ns
t <sub>CLK</sub>	CLK Period	4x	4x	400		ns
t <sub>WL</sub>	CLK Low width	2x - 40		160		ns
t <sub>WH</sub>	CLK High width	2x - 40		160		ns
t <sub>AS</sub>	Address Setup to $\overline{RD}$ , $\overline{WR}$	x - 45		55		ns
t <sub>RR</sub>	$\overline{RD}$ Low width	2.5x - 40		210		ns
t <sub>CA</sub> *	Address Hold Time After $\overline{RD}$ , $\overline{WR}$	0.5x - 40		10		ns
t <sub>AD</sub>	Address to Valid Data In		3.5x - 95		255	ns
t <sub>RD</sub>	$\overline{RD}$ to Valid Data In		2.5x - 80		170	ns
t <sub>HR</sub>	Input Data Hold After $\overline{RD}$	0		0		ns
t <sub>WW</sub>	$\overline{WR}$ Low width	2.5x - 40		210		ns
t <sub>DW</sub>	Data Setup to $\overline{WR}$	2x - 50		150		ns
t <sub>WD</sub>	Data Hold After $\overline{WR}$	30	90	30	90	ns
t <sub>CWA</sub>	$\overline{RD}$ , $\overline{WR}$ to Valid $\overline{WAIT}$		1.5x - 100		50	ns
t <sub>AWA</sub>	Address to Valid $\overline{WAIT}$		2.5x - 130		120	ns
t <sub>WAS</sub>	$\overline{WAIT}$ Setup to CLK	70		70		ns
t <sub>WAH</sub>	$\overline{WAIT}$ Hold After CLK	0		0		ns
t <sub>RV</sub>	$\overline{RD}/\overline{WR}$ Recovery Time	1.5x - 35		115		ns
t <sub>CPW</sub>	CLK to Port Data Output		x + 200		300	ns
t <sub>PRC</sub>	Port Data Setup to CLK	200		200		ns
t <sub>PCR</sub>	Port Data Hold After CLK	100		100		ns
t <sub>CHCL</sub>	$\overline{RD}/\overline{WR}$ Hold After CLK	x - 60		40		ns
t <sub>CLC</sub>	$\overline{RD}/\overline{WR}$ Setup to CLK	1.5x - 50		100		ns
t <sub>CLHA</sub>	Address Hold After CLK	1.5x - 80		70		ns
t <sub>ACL</sub>	Address Setup to CLK	2.5x - 80		170		ns
t <sub>CLD</sub>	Data Setup to CLK	x - 50		50		ns

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- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 - D7)  
 High 0.8V<sub>CC</sub>/Low 0.2V<sub>CC</sub> (excluding D0 - D7)

\* t<sub>CA</sub> spec is different from other parts of TLCS-90.

4.4 A/D Conversion Characteristics

V<sub>CC</sub> = 5V ± 10% TA = -40~85°C (1~10MHz)

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>REF</sub>	Analog reference voltage	V <sub>CC</sub> - 1.5	V <sub>CC</sub>	V <sub>CC</sub>	V
A <sub>GN</sub> D	Analog reference voltage	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	
V <sub>AIN</sub>	Allowable analog input voltage	V <sub>SS</sub>		V <sub>CC</sub>	
I <sub>REF</sub>	Supply current for analog reference voltage		0.5	1.0	mA
Error	Total error (TA = 25°C, V <sub>CC</sub> = V <sub>REF</sub> = 5.0V)		1.5		LSB
	Total error			3.0	

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4.5 Zero- Cross Characteristics

V<sub>CC</sub> = 5V ± 10% TA = -40~85°C (1~10MHz)

Symbol	Parameter	Condition	Min	Max	Unit
V <sub>ZX</sub>	Zero- cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p - p
A <sub>ZX</sub>	Zero- cross accuracy	50/60Hz sine wave		135	mV
F <sub>ZX</sub>	Zero- cross detection input frequency		0.04	1	kHz

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4.6 Serial Channel Timing - I/O Interface Mode

V<sub>CC</sub> = 5V ± 10% TA = -40~85°C (1~10MHz)  
CL = 50pF

Symbol	Parameter	Variable		10MHz Clock		Unit
		Min	Max	Min	Max	
t <sub>SCY</sub>	Serial Port Clock Cycle Time	8x		800		ns
t <sub>OSS</sub>	Output Data Setup SCLK Rising Edge	6x - 150		450		ns
t <sub>OHS</sub>	Output Data Hold After SCLK Rising Edge	2x - 120		80		ns
t <sub>HSR</sub>	Input Data Hold After SCLK Rising Edge	0		0		ns
t <sub>SRD</sub>	SCLK Rising Edge to Input DATA Valid		6x - 150		450	ns

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4.7 16-bit Event Counter





V<sub>CC</sub> = 5V ± 10% TA = -40~85°C (1~10MHZ)

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t <sub>VCK</sub>	TI4 clock cycle	8x + 100		900		ns
t <sub>VCKL</sub>	TI4 Low clock pulse width	4x + 40		440		ns
t <sub>VCKH</sub>	TI4 High clock pulse width	4x + 40		440		ns

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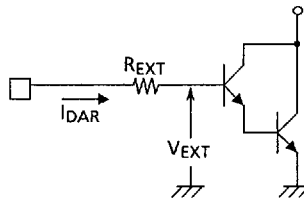
4.8 Interrupt Operation

V<sub>CC</sub> = 5V ± 10% TA = -40~85°C (1~10MHZ)

Symbol	Parameter	Variable		10MHz Clock		Units
		Min	Max	Min	Max	
t <sub>INTAL</sub>	NMI, INT0 Effective pulse width (  )	4x		400		ns
t <sub>INTAH</sub>	$\bar{NMI}$ , INT0 Effective pulse width (  )	4x		400		ns
t <sub>INTBL</sub>	INT1, INT2 Effective pulse width (  )	8x + 100		900		ns
t <sub>INTBH</sub>	INT1, INT2 Effective pulse width (  )	8x + 100		900		ns

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(Reference) Definition of I<sub>DAR</sub>



## 4.9 Read Operation (PROM Mode)

## DC Characteristic, AC Characteristic

TA = -40~85°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
V <sub>PP</sub>	V <sub>pp</sub> Read Voltage	-	4.5	5.5	V
V <sub>IH1</sub>	Input High Voltage (A0~A15, $\overline{CE}$ , $\overline{OE}$ )	-	0.7 × V <sub>CC</sub>	V <sub>CC</sub> + 0.3	V
V <sub>IL1</sub>	Input Low Voltage (A0~A15, $\overline{CE}$ , $\overline{OE}$ )	-	-0.3	0.3 × V <sub>CC</sub>	V
t <sub>ACC</sub>	Address to Output Delay	C <sub>L</sub> = 50pF	-	2.25TCYC + α	ns

TCYC = 400ns (10MHz Clock)

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α = 200ns

## 4.10 Programming Operation (PROM Mode)

## DC Characteristic, AC Characteristic

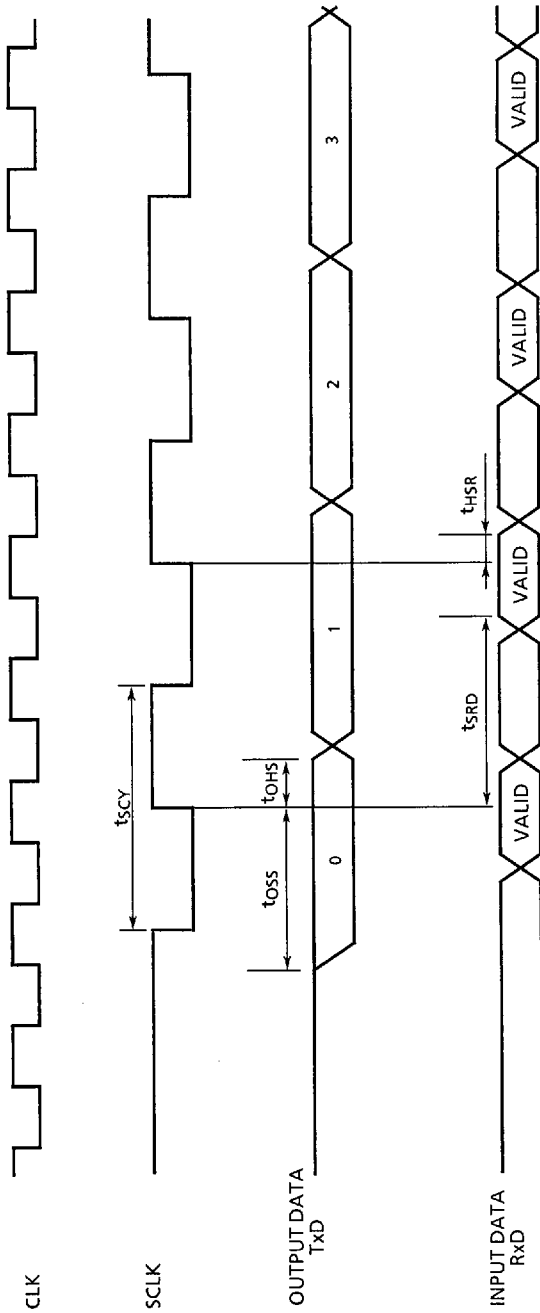
TA = 25 ± 5°C Vcc = 6V ± 0.25V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V <sub>PP</sub>	Programing Voltage	-	12.25	12.50	12.75	V
V <sub>IH</sub>	Input High Voltage (D0~D7)	-	0.2V <sub>CC</sub> + 1.1		V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input Low Voltage (D0~D7)	-	-0.3		0.2V <sub>CC</sub> - 0.1	V
V <sub>IH1</sub>	Input High Voltage (A0~A15, $\overline{CE}$ , $\overline{OE}$ )	-	0.7V <sub>CC</sub>		V <sub>CC</sub> + 0.3	V
V <sub>IL1</sub>	Input Low Voltage (A0~A15, $\overline{CE}$ , $\overline{OE}$ )	-	-0.3		0.3V <sub>CC</sub>	V
I <sub>CC</sub>	V <sub>CC</sub> Supply Current	f <sub>OSC</sub> = 10MHz	-		50	mA
I <sub>PP</sub>	V <sub>PP</sub> Supply Current	V <sub>PP</sub> = 13.00V	-		50	mA
tpw	$\overline{CE}$ Programming Pulse Width	C <sub>L</sub> = 50pF	0.95	1.00	1.05	ms

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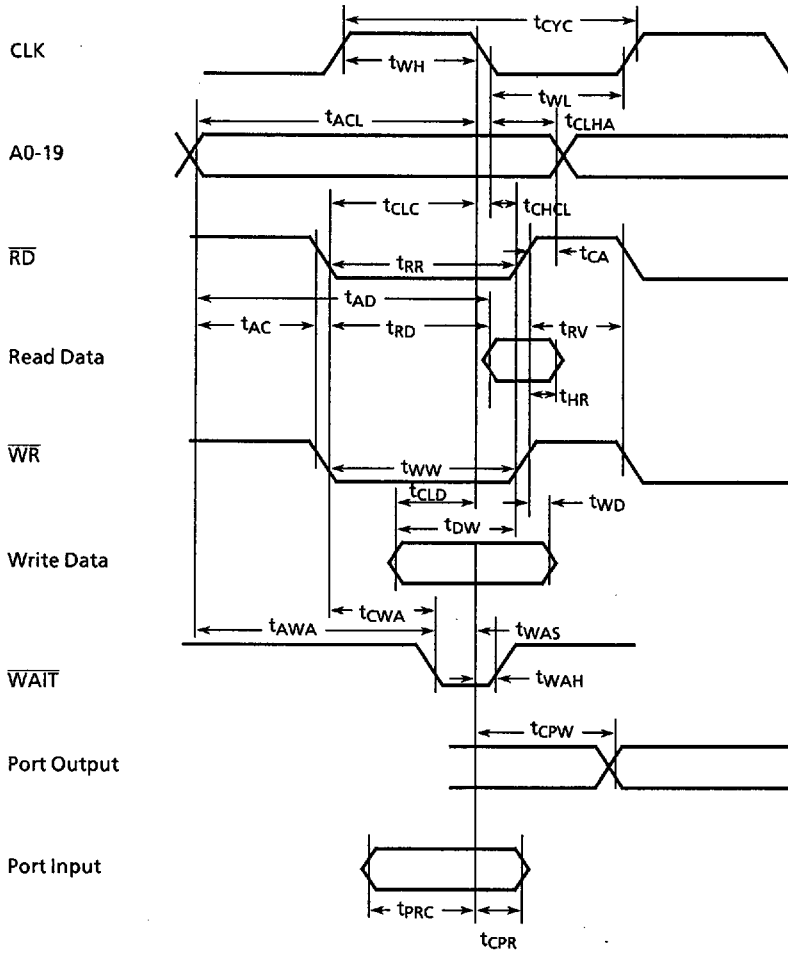


4.11 I/O Interface Mode Timing Chart



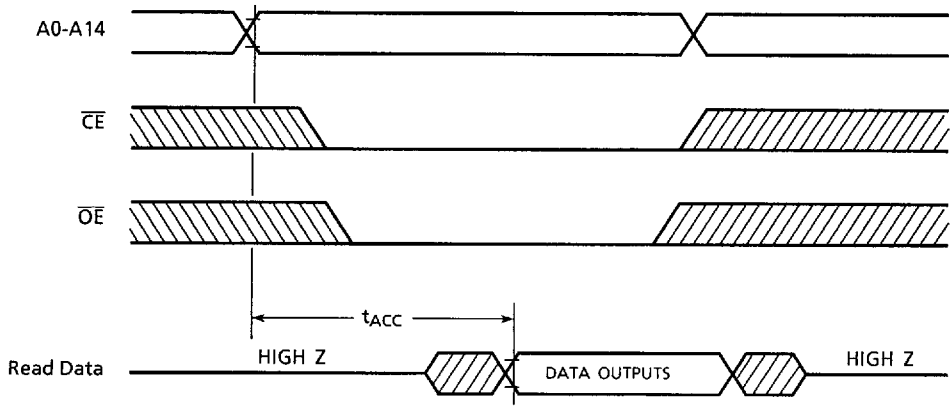
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4.12 Timing Chart



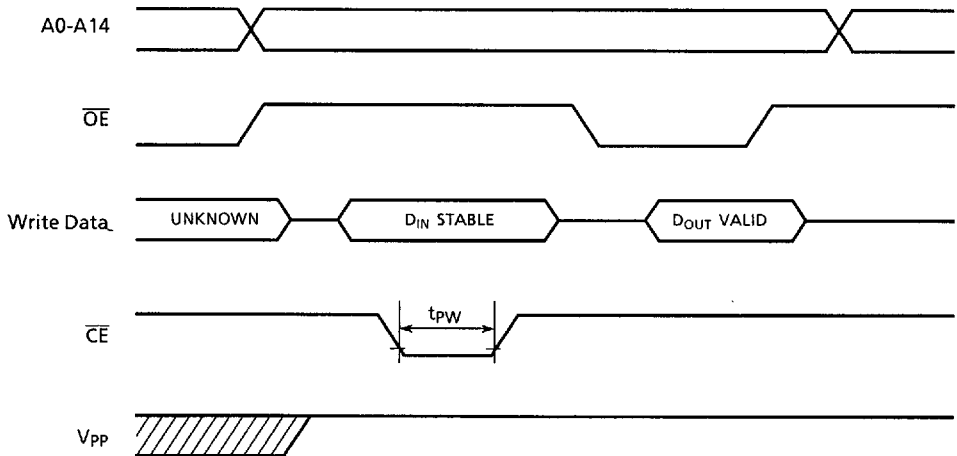
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4.13 Read Operation Timing Chart (PROM Mode)



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4.14 Programming Operation Timing Chart (PROM Mode)



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