

# T6C24

## ROW DRIVER LSI FOR A DOT MATRIX LCD

The TOSHIBA T6C24 is a row (common) driver LSI for a small-interface or medium-scale dot matrix LCD.

The T6C24 generates the timing signals for the display using a built-in oscillator and also controls the T6C23 column (segment) LCD driver.

The T6C24 features a low-impedance 240-output row driver.

The T6C24 also includes internal resistors to divide the bias voltage, a power supply op-amp and a contrast control circuit.

The T6C24 can be used in conjunction with the T6C23 to construct a low-power LCD system.

Unit: mm		
T6C24	LEAD PITCH	
	IN	OUT
(UAW)	1.2	0.22
(UBW)	1.2	0.21
(UFW, 6FS)	1.2	0.21

Please contact Toshiba or on authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

### FEATURES

- Row signal output for LCD
- Built-in oscillator (additional external resistor)
- Duty: 1 / 240
- Display-off function: /DSPOF = L, all LCD outputs = V<sub>SS</sub>
- Low power consumption
- Logic power supply: 2.7 to 5.5V
- LCD power supply: 8.0V to 30.0V
- CMOS process
- Package: TCP (Tape Carrier Package)

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● Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.

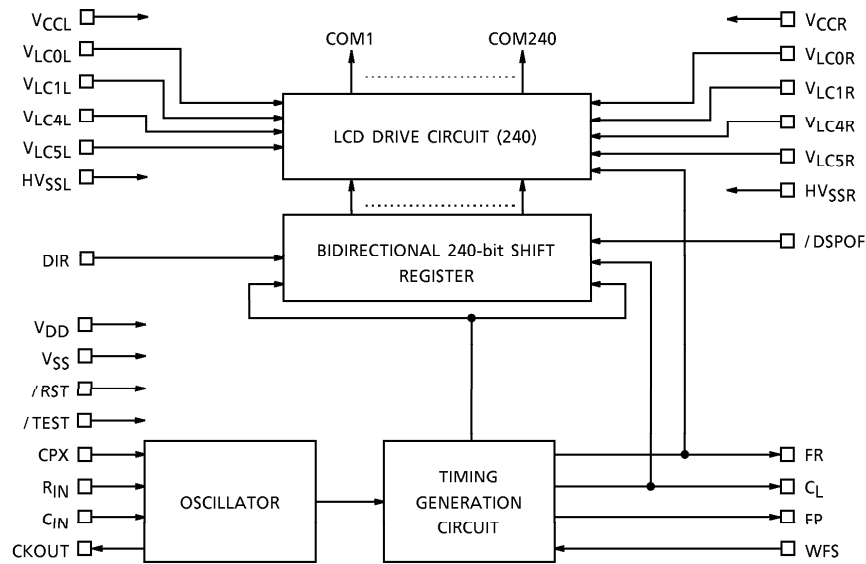
● Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction. This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.

● The products described in this document are subject to foreign exchange and foreign trade control laws.

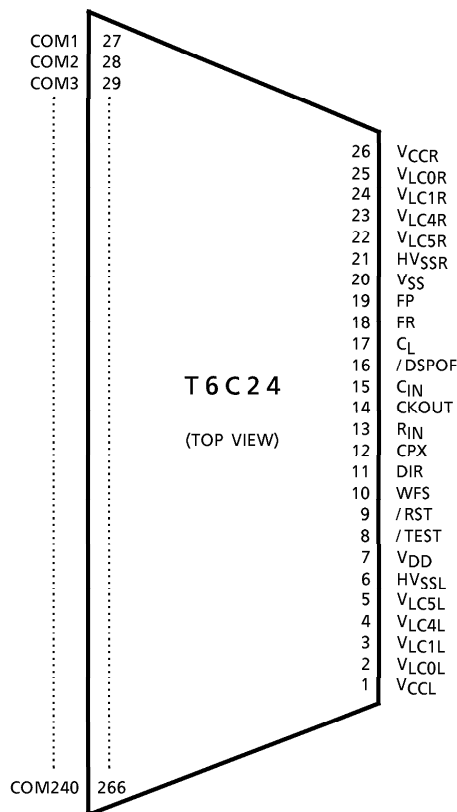
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BLOCK DIAGRAM



PIN ASSIGNMENT



(\*) The above diagram shows the pin configuration of the LSI chip; it does not show the configuration of the tape carrier package.

**PIN FUNCTIONS**

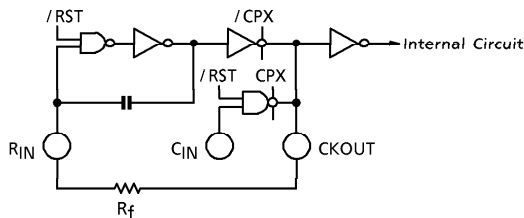
PIN NAME	PIN No.	I/O	FUNCTIONS						
COM1 to COM240	27 to 266	Output	Row driver outputs						
C <sub>L</sub>	17	Output	Shift clock pulse						
FP	19	Output	Display synchronous signal						
FR	18	Output	Frame signal						
DIR	11	Input	Data flow direction select. Usually connected to V <sub>DD</sub> <table border="1" style="margin-left: 20px;"> <tr> <th>DIR</th> <th>DATA FLOW</th> </tr> <tr> <td>H</td> <td>COM1→COM240</td> </tr> <tr> <td>L</td> <td>COM240→COM1</td> </tr> </table>	DIR	DATA FLOW	H	COM1→COM240	L	COM240→COM1
DIR	DATA FLOW								
H	COM1→COM240								
L	COM240→COM1								
WFS	10	Input	Frame signal inversion select. Usually connected to V <sub>DD</sub> . WFS = H: FR phase change per 13 lines. WFS = L: FR phase change per 17 lines.						
/DSPOF	16	Input	Display off. Usually connected to V <sub>DD</sub> /DSPOF = H: Display-on mode, (COM1 to COM240) are operational. /DSPOF = L: Display-off mode, (COM1 to COM240) are at the V <sub>SS</sub> level.						
/RST	9	Input	/RST = L: Reset state. Usually connected to V <sub>DD</sub>						
CPX	12	Input	Crystal oscillation / CR oscillation Select CPX = L: CR oscillation CPX = H: Crystal oscillation or external clock input from C <sub>IN</sub>						
R <sub>IN</sub>	13	Input	Connected to resistor for built-in oscillator						
C <sub>IN</sub>	15	Input	Connected to crystal						
CKOUT	14	Output	Connected to resistor or crystal for built-in oscillator						
/TEST	8	Input	Test pin. Usually connected to V <sub>DD</sub>						
V <sub>DD</sub> , V <sub>SS</sub>	7, 20	—	Power supply						
V <sub>CC1</sub> , V <sub>CC2</sub> V <sub>LC0L</sub> , V <sub>LC0R</sub> V <sub>LC1L</sub> , V <sub>LC1R</sub> V <sub>LC4L</sub> , V <sub>LC4R</sub> V <sub>LC5L</sub> , V <sub>LC5R</sub> HV <sub>SSL</sub> , HV <sub>SSR</sub>	1, 26 2, 25 3, 24 4, 23 5, 22 6, 21	—	Power supply for LCD drive						

**FUNCTION OF EACH BLOCK**

- Oscillator

The T6C24 has an on-chip oscillator (an external resistor is required).

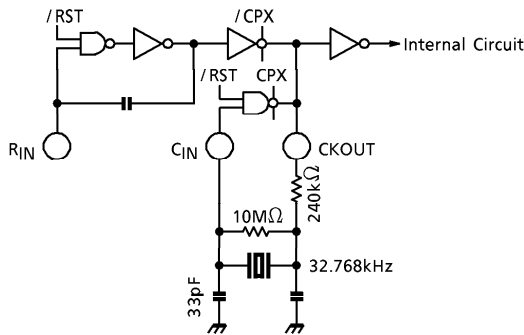
(1) CPX = L



$R_f$	$f_{osc}$
390k $\Omega$	54kHz
620k $\Omega$	34kHz
780k $\Omega$	27kHz

(Note) The resistor values are typical values. The oscillation frequency depends on how the device has been mounted. Hence  $R_f$  must be adjusted to achieve the target oscillation frequency.

(2) CPX = H



- Timing generation circuit

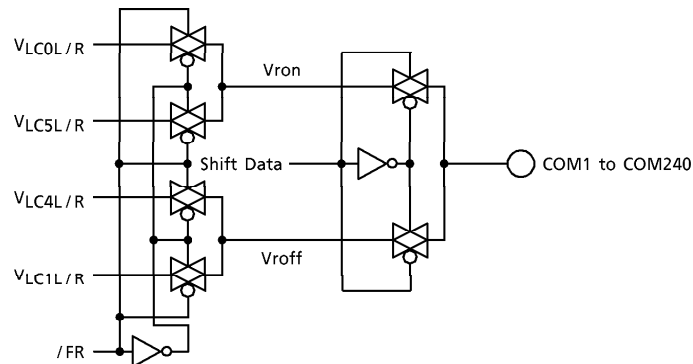
This circuit divides the oscillator frequency and generates the display timing signals ( $C_L$ , FP and FR).

- Shift register

240-bit shift register

● Row driver circuit and LCD voltage generation circuit

The T6C24 has 240 row drivers and four different LCD drive output voltage levels. The display data from the latch circuit and the M signal determine which of the four LCD drive voltage is selected. The voltage generation circuit and row driver circuit are shown in the following diagram.



**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V <sub>DD</sub> (Note 2)	-0.3 to 7.0	V
Supply Voltage (2)	(Note 1, 2)	-0.3 to 32.0	V
Input Voltage	V <sub>in</sub> (Note 2, 3)	-0.3 to V <sub>DD</sub> + 0.3	V
Operating Temperature	T <sub>opr</sub>	-20 to 75	°C
Storage Temperature	T <sub>stg</sub>	-55 to 125	°C

(Note 1) V<sub>CCL</sub>, V<sub>CCR</sub>, V<sub>LC0L/R</sub>, V<sub>LC0R</sub>, V<sub>LC1L/R</sub>, V<sub>LC1R</sub>, V<sub>LC4L/R</sub>, V<sub>LC4R</sub>, V<sub>LC5L/R</sub> and V<sub>LC5R</sub>

(Note 2) Referenced to V<sub>SS</sub>, HV<sub>SSL</sub> and HV<sub>SSR</sub>

(Note 3) Applies to all data bus and I/O pins.

(Note 4) Ensure that the following condition is always maintained.

$$V_{CCL/R} \geq V_{LC0L/R} \geq V_{LC1L/R} \geq V_{LC4L/R} \geq V_{LC5L/R} \geq HV_{SSL/R}$$

## ELECTRICAL CHARACTERISTICS

## DC CHARACTERISTICS

## TEST CONDITIONS (1)

(Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 3.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V \pm 10\%$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Supply (1)	$V_{DD}$	—	—	2.7	—	3.3	V	$V_{DD}$
Operating Supply (2)	$V_{CC}$	—	—	8.0	—	30.0	V	$V_{CCL}$ , $V_{CCR}$
Input Voltage	H Level	$V_{IH}$	—	0.7 $V_{DD}$	—	$V_{DD}$	V	WFS, CPX, DIR, /DSPOF, /RST, /TEST
	L Level	$V_{IL}$	—	0	—	0.3 $V_{DD}$	V	
Output Voltage	H Level	$V_{OH}$	—	$I_{OH} = -400\mu A$	$V_{DD}$ -0.4	—	V	$C_L$ , FP, FR
	L Level	$V_{OL}$	—	$I_{OL} = 400\mu A$	$V_{SS}$	$V_{SS}$ +0.4	V	
Row Driver Output Resistance	$R_{row}$	—	(Note 5) Load voltage = output level of 0.5V	—	—	1.5	$k\Omega$	COM1 to COM240
Input Leakage	$I_{IL}$	—	$V_{IN} = V_{DD}$ to GND	-1	—	1	$\mu A$	WFS, CPX, DIR, /DSPOF, /RST, /TEST
Current Consumption (1)	$I_{SS}$	—	(Note 1)	—	-35	-50	$\mu A$	$V_{DD}$
Current Consumption (2)	$I_{CC}$	—	(Note 2)	—	10	20	$\mu A$	$V_{CCL}$ , $V_{CCR}$ $V_{LC0L}$ , $V_{LC0R}$
Current Consumption (3)	$I_{DOF}$	—	(Note 3)	—	25	40	$\mu A$	$V_{SS}$ , $V_{SSL}$ , $V_{SSR}$ $V_{LC5L}$ , $V_{LC5R}$
Current Consumption (4)	$I_{STB}$	—	(Note 4)	-1	—	1	$\mu A$	$V_{SS}$ , $V_{SSL}$ , $V_{SSR}$ $V_{LC5L}$ , $V_{LC5R}$
Operating Freq.	$f_{OSC}$	—	—	20	—	100	kHz	$R_{IN}$ , $C_{IN}$
External Clock Frequency	$f_{ex}$	—	—	20	—	100	kHz	$C_{IN}$
External Clock Duty	$f_{duty}$	—	—	40	50	60	%	$C_{IN}$
External Clock Rise/ Fall Time	$t_r / t_f$	—	—	—	—	50	ns	$C_{IN}$

(Note 1) Logic current:  $V_{DD} = 3.0V \pm 10\%$ ,  $T_a = 25^\circ C$ ,  $R_f = 620k\Omega$  (33.6kHz), no load(Note 2) LCD driver current:  $V_{DD} = 3.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V$ ,  $T_a = 25^\circ C$ , 1/13 bias,  $R_f = 620k\Omega$ , no load(Note 3) Display-off current:  $V_{DD} = 3.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V$ ,  $T_a = 25^\circ C$ , 1/13 bias,  $R_f = 620k\Omega$ , /DSPOF = L, no load(Note 4) Standby current:  $V_{DD} = 3.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V$ ,  $T_a = 25^\circ C$ , 1/13 bias,  $R_f = 620k\Omega$ , /RST = L, no load(Note 5)  $V_{CCL}/R = V_{LC0L}/R = 23.0V$ ,  $V_{LC1L}/R = V_{CC} \times 12/13$ ,  $V_{LC4L}/R = V_{CC} \times 1/13$ ,  $HV_{SSL}/R = V_{LC5L}/R = 0V$

## TEST CONDITIONS (2)

(Unless otherwise noted,  $V_{SS} = 0V$ ,  $V_{DD} = 5.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V \pm 10\%$ ,  $T_a = -20$  to  $75^\circ C$ )

ITEM	SYMBOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Supply (1)	$V_{DD}$	—	—	4.5	—	5.5	V	$V_{DD}$
Operating Supply (2)	$V_{CC}$	—	—	8.0	—	30.0	V	$V_{CCL}$ , $V_{CCR}$
Input Voltage	H Level	$V_{IH}$	—	0.7 $V_{DD}$	—	$V_{DD}$	V	WFS, CPX, DIR, /DSPOF, /RST, /TEST
	L Level	$V_{IH}$	—	0	—	0.3 $V_{DD}$	V	
Output Voltage	H Level	$V_{OH}$	—	$I_{OH} = -400\mu A$	$V_{DD}$ -0.4	—	V	CL, FP, FR
	L Level	$V_{OL}$	—	$I_{OL} = 400\mu A$	$V_{SS}$	—	$V_{SS}$ +0.4	
Row Driver Output Resistance	$R_{row}$	—	(Note 5) Load voltage = output level of 0.5V	—	—	1.5	k $\Omega$	COM1 to COM240
Input Leakage	$I_{IL}$	—	$V_{IN} = V_{DD}$ to GND	-1	—	1	$\mu A$	WFS, CPX, DIR, /DSPOF, /RST, /TEST
Current Consumption (1)	$I_{SS}$	—	(Note 1)	—	-60	-90	$\mu A$	$V_{DD}$
Current Consumption (2)	$I_{CC}$	—	(Note 2)	—	10	20	$\mu A$	$V_{CCL}$ , $V_{CCR}$ $V_{LC0L}$ , $V_{LC0R}$
Current Consumption (3)	$I_{DOF}$	—	(Note 3)	—	50	80	$\mu A$	$V_{SS}$ , $V_{SSL}$ , $V_{SSR}$ $V_{LC5L}$ , $V_{LC5R}$
Current Consumption (4)	$I_{STB}$	—	(Note 4)	-1	—	1	$\mu A$	$V_{SS}$ , $V_{SSL}$ , $V_{SSR}$ $V_{LC5L}$ , $V_{LC5R}$
Operating Freq.	$f_{OSC}$	—	—	20	—	100	kHz	$R_{IN}$ , $C_{IN}$
External Clock Frequency	$f_{ex}$	—	—	20	—	100	kHz	$C_{IN}$
External Clock Duty	$f_{duty}$	—	—	40	50	60	%	$C_{IN}$
External Clock Rise / Fall Time	$t_r / t_f$	—	—	—	—	50	ns	$C_{IN}$

(Note 1) Logic current:  $V_{DD} = 5.0V \pm 10\%$ ,  $T_a = 25^\circ C$ ,  $R_f = 620k\Omega$  (33.6kHz), no load(Note 2) LCD driver current:  $V_{DD} = 5.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V$ ,  $T_a = 25^\circ C$ , 1 / 13 bias,  $R_f = 620k\Omega$ , no load(Note 3) Display-off current:  $V_{DD} = 5.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V$ ,  $T_a = 25^\circ C$ , 1 / 13 bias,  $R_f = 620k\Omega$ , /DSPOF = L, no load(Note 4) Standby current:  $V_{DD} = 5.0V \pm 10\%$ ,  $V_{CCL}/R = 23.0V$ ,  $T_a = 25^\circ C$ , 1 / 13 bias,  $R_f = 620k\Omega$ , /RST = L, no load(Note 5)  $V_{CCL}/R = V_{LC0L}/R = 23.0V$ ,  $V_{LC1L}/R = V_{CC} \times 12 / 13$ ,  $V_{LC4L}/R = V_{CC} \times 1 / 13$ ,  $HV_{SSL}/R = V_{LC5L}/R = 0V$