**Freescale Semiconductor**
Hardware Specification

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# MCF5275 Integrated Microprocessor Family Hardware Specification

by: Microcontroller Division

The MCF5275 family is a highly integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document describes pertinent features and functions characteristics of the MCF5275 family. The MCF5275 family includes the MCF5275, MCF5275L, MCF5274 and MCF5274L microprocessors. The differences between these parts are summarized in Table 1. This document is written from the perspective of the MCF5275 and unless otherwise noted, the information applies also to the MCF5275L, MCF5274 and MCF5274L.

The MCF5275 family delivers a new level of performance and integration on the popular version 2 ColdFire core with up to 159 (Dhrystone 2.1) MIPS @ 166MHz. These highly integrated microprocessors build upon the widely used peripheral mix on the popular MCF5272 ColdFire microprocessor (10/100 Mbps Ethernet MAC and USB device) by adding a second 10/100 Mbps Ethernet MAC (MCF5274 and MCF5275) and hardware encryption (MCF5275L and MCF5275).

**Contents**

In addition, the MCF5275 family features an enhanced multiply accumulate unit (EMAC), large on-chip memory (64 Kbytes SRAM, 16 Kbytes configurable cache), and a 16-bit DDR SDRAM memory controller.

These devices are ideal for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming, and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.freescale.com/coldfire.

# 1 MCF5275 Family Configurations

**Table 1. MCF5275 Family Configurations**

| Module | MCF5274L | MCF5275L | MCF5274 | MCF5275 |
|---|---|---|---|---|
| ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit) | x | x | x | x |
| System Clock | up to 166 MHz | | | |
| Performance (Dhrystone 2.1 MIPS) | up to 159 | | | |
| Instruction/Data Cache | 16 Kbytes (configurable) | | | |
| Static RAM (SRAM) | 64 Kbytes | | | |
| Interrupt Controllers (INTC) | 2 | 2 | 2 | 2 |
| Edge Port Module (EPORT) | x | x | x | x |
| External Interface Module (EIM) | x | x | x | x |
| 4-channel Direct-Memory Access (DMA) | x | x | x | x |
| DDR SDRAM Controller | x | x | x | x |
| Fast Ethernet Controller (FEC) | 1 | 1 | 2 | 2 |
| Watchdog Timer Module (WDT) | x | x | x | x |
| 4-channel Programmable Interval Timer Module (PIT) | x | x | x | x |
| 32-bit DMA Timers | 4 | 4 | 4 | 4 |
| USB | x | x | x | x |
| QSPI | x | x | x | x |
| UART(s) | 3 | 3 | 3 | 3 |
| $I^2C$ | x | x | x | x |
| PWM | 4 | 4 | 4 | 4 |
| General Purpose I/O Module (GPIO) | x | x | x | x |
| CIM = Chip Configuration Module + Reset Controller Module | x | x | x | x |
| Debug BDM | x | x | x | x |
| JTAG - IEEE 1149.1 Test Access Port | x | x | x | x |
| Hardware Encryption | — | x | — | x |
| Package | 196 MAPBGA | 196 MAPBGA | 256 MAPBGA | 256 MAPBGA |

# 2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package.

Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

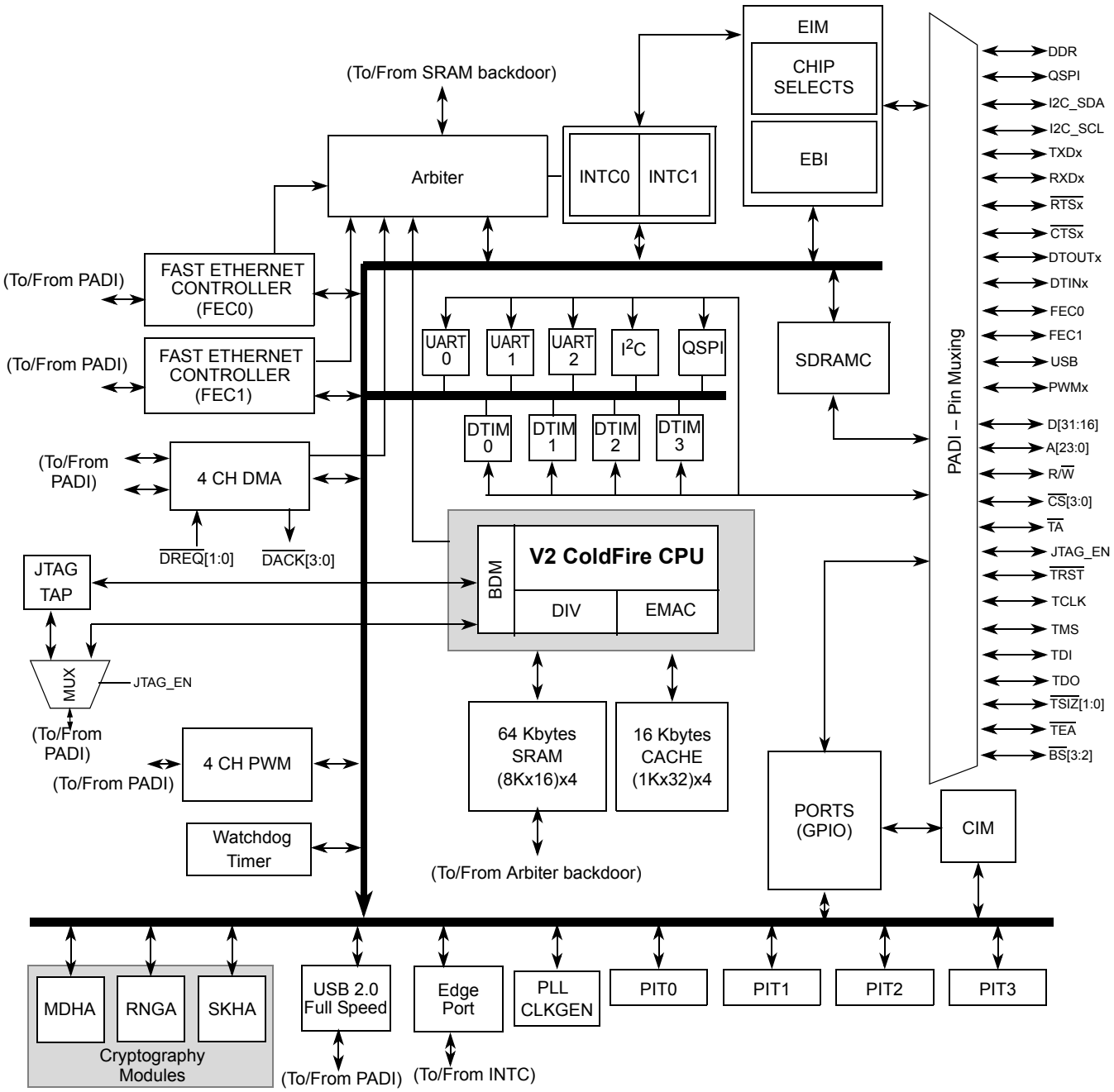



**Figure 1. MCF5275 Block Diagram**

# 3 Features

For a detailed feature list see the *MCF5275 Reference Manual* (MCF5275RM).

# 4 Signal Descriptions

This section describes signals that connect off chip, including a table of signal properties. For a more detailed discussion of the MCF5275 signals, consult the *MCF5275 Reference Manual* (MCF5275RM).

Table 2 lists the signals for the MCF5275 in functional group order. The "Dir" column is the direction for the primary function of the pin. Refer to Section 6, "Mechanicals/Pinouts," for package diagrams.

**NOTE**

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

**NOTE**

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274<br>MCF5275<br>256 MAPBGA | MCF5274L<br>MCF5275L<br>196 MAPBGA |
|---|---|---|---|---|---|---|
| **Reset** | | | | | | |
| $\overline{\text{RESET}}$ | — | — | — | I | N15 | K12 |
| $\overline{\text{RSTOUT}}$ | — | — | — | O | N14 | L12 |
| **Clock** | | | | | | |
| EXTAL | — | — | — | I | L16 | M14 |
| XTAL | — | — | — | O | M16 | N14 |
| CLKOUT | — | — | — | O | T12 | P9 |
| **Mode Selection** | | | | | | |
| CLKMOD[1:0] | — | — | — | I | N13, P13 | M11, N11 |
| $\overline{\text{RCON}}$ | — | — | — | I | P8 | M6 |
| **External Memory Interface and Ports** | | | | | | |
| A[23:21] | PADDR[7:5] | $\overline{\text{CS}}$[6:4] | — | O | A11, B11, C11 | A8, B8, C8 |

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274 MCF5275 256 MAPBGA | MCF5274L MCF5275L 196 MAPBGA |
|---|---|---|---|---|---|---|
| A[20:0] | — | — | — | O | A12, B12, C12, A13, B13, C13, A14, B14, C14, B15, C15, B16, C16, D14, D15, E14:16, F14:16 | B9, D9, C9, C10, B10, A11, C11, B11, A12, D11, C12, B13, C13, D12, E11, D13, E12, F11, D14, E13, F13 |
| D[31:16] | — | — | — | O | M1, N1, N2, N3, P1, P2, R1, R2, P3, R3, T3, N4, P4, R4, T4, N5 | J3, L1, K2, K3, M1, L2, L3, L4, K4, J4, M2, N1, N2, M3, M4, N3 |
| $\overline{BS}$[3:2] | $\overline{PBS}$[3:2] | $\overline{CAS}$[3:2] | — | O | M3, R5 | K1, L5 |
| $\overline{OE}$ | PBUSCTL[7] | — | — | O | K1 | H4 |
| $\overline{TA}$ | PBUSCTL[6] | — | — | I | L13 | K14 |
| $\overline{TEA}$ | PBUSCTL[5] | $\overline{DREQ1}$ | — | I | T8 | — |
| R/$\overline{W}$ | PBUSCTL[4] | — | — | O | P7 | L6 |
| TSIZ1 | PBUSCTL[3] | DACK1 | — | O | D16 | B14 |
| TSIZ0 | PBUSCTL[2] | DACK0 | — | O | G16 | E14 |
| $\overline{TS}$ | PBUSCTL[1] | DACK2 | — | O | L4 | H2 |
| $\overline{TIP}$ | PBUSCTL[0] | $\overline{DREQ0}$ | — | O | P6 | — |
| **Chip Selects** | | | | | | |
| $\overline{CS}$[7:1] | PCS[7:1] | — | — | O | D10:13, E13, F13, N7 | D8, A9, A10, D10, B12, C14, P4 |
| $\overline{CS0}$ | — | — | — | O | R6 | N5 |
| **DDR SDRAM Controller** | | | | | | |
| DDR_CLKOUT | — | — | — | O | T7 | P6 |
| $\overline{DDR\_CLKOUT}$ | — | — | — | O | T6 | P5 |
| $\overline{SD\_CS}$[1:0] | PSDRAM[7:6] | $\overline{CS}$[3:2] | — | O | M2, T5 | H3, M5 |
| $\overline{SD\_SRAS}$ | PSDRAM[5] | — | — | O | L2 | H1 |
| $\overline{SD\_SCAS}$ | PSDRAM[4] | — | — | O | L1 | G3 |
| $\overline{SD\_WE}$ | PSDRAM[3] | — | — | O | K2 | G4 |
| SD_A10 | — | — | — | O | N6 | N4 |
| $\overline{SD\_DQS}$[3:2] | PSDRAM[2:1] | — | — | I/O | M4, P5 | J2, P3 |
| SD_CKE | PSDRAM[0] | — | — | O | L3 | J1 |
| SD_VREF | — | — | — | I | A15, T2 | A13, P2 |

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274<br>MCF5275<br>256 MAPBGA | MCF5274L<br>MCF5275L<br>196 MAPBGA |
|---|---|---|---|---|---|---|
| **External Interrupts Port** | | | | | | |
| $\overline{\text{IRQ}}$[7:5] | PIRQ[7:5] | — | — | I | G13, H16, H15 | F14, G13, G14 |
| $\overline{\text{IRQ}}$[4] | PIRQ[4] | $\overline{\text{DREQ2}}$ | — | I | H14 | H11 |
| $\overline{\text{IRQ}}$[3:2] | PIRQ[3:2] | $\overline{\text{DREQ}}$[3:2] | — | I | J14, J13 | H14, H12 |
| $\overline{\text{IRQ1}}$ | PIRQ[1] | — | — | I | K13 | J13 |
| **FEC0** | | | | | | |
| FEC0_MDIO | PFECI2C[5] | I2C_SDA | U2RXD | I/O | A7 | A3 |
| FEC0_MDC | PFECI2C[4] | I2C_SCL | U2TXD | O | B7 | C5 |
| FEC0_TXCLK | PFEC0H[7] | — | — | I | C3 | C1 |
| FEC0_TXEN | PFEC0H[6] | — | — | O | D4 | C3 |
| FEC0_TXD[0] | PFEC0H[5] | — | — | O | G4 | D2 |
| FEC0_COL | PFEC0H[4] | — | — | I | A6 | B4 |
| FEC0_RXCLK | PFEC0H[3] | — | — | I | B6 | B3 |
| FEC0_RXDV | PFEC0H[2] | — | — | I | B5 | C4 |
| FEC0_RXD[0] | PFEC0H[1] | — | — | I | C6 | D5 |
| FEC0_CRS | PFEC0H[0] | — | — | I | C7 | A2 |
| FEC0_TXD[3:1] | PFEC0L[7:5] | — | — | O | E3, F3, F4 | D1, E3, D3 |
| FEC0_TXER | PFEC0L[4] | — | — | O | D3 | C2 |
| FEC0_RXD[3:1] | PFEC0L[3:1] | — | — | I | D5, C5, D6 | D4, B1, B2 |
| FEC0_RXER | PFEC0L[0] | — | — | I | C4 | E4 |
| **FEC1** | | | | | | |
| FEC1_MDIO | PFECI2C[3] | — | — | I/O | G1 | — |
| FEC1_MDC | PFECI2C[2] | — | — | O | G2 | — |
| FEC1_TXCLK | PFEC1H[7] | — | — | I | C1 | — |
| FEC1_TXEN | PFEC1H[6] | — | — | O | D2 | — |
| FEC1_TXD[0] | PFEC1H[5] | — | — | O | F1 | — |
| FEC1_COL | PFEC1H[4] | — | — | I | A5 | — |
| FEC1_RXCLK | PFEC1H[3] | — | — | I | B4 | — |
| FEC1_RXDV | PFEC1H[2] | — | — | I | A3 | — |
| FEC1_RXD[0] | PFEC1H[1] | — | — | I | B3 | — |
| FEC1_CRS | PFEC1H[0] | — | — | I | A4 | — |

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274<br>MCF5275<br>256 MAPBGA | MCF5274L<br>MCF5275L<br>196 MAPBGA |
|---|---|---|---|---|---|---|
| FEC1_TXD[3:1] | PFEC1L[7:5] | — | — | O | E1, E2, F2 | — |
| FEC1_TXER | PFEC1L[4] | — | — | O | D1 | — |
| FEC1_RXD[3:1] | PFEC1L[3:1] | — | — | I | B1, B2, A2 | — |
| FEC1_RXER | PFEC1L[0] | — | — | I | C2 | — |
| **I²C** | | | | | | |
| I2C_SDA | PFECI2C[1] | U2RXD | — | I/O | B10 | B7 |
| I2C_SCL | PFECI2C[0] | U2TXD | — | I/O | C10 | A7 |
| **DMA** | | | | | | |
| DACK[3:0] and $\overline{\text{DREQ}}$[3:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: PCS3/PWM3 for DACK3, PCS2/PWM2 for DACK2, TSIZ1 for DACK1, TSIZ0 for DACK0, $\overline{\text{IRQ3}}$ for $\overline{\text{DREQ3}}$, $\overline{\text{IRQ2}}$ and $\overline{\text{TA}}$ for $\overline{\text{DREQ2}}$, $\overline{\text{TEA}}$ for $\overline{\text{DREQ1}}$, and $\overline{\text{TIP}}$ for $\overline{\text{DREQ0}}$. | | | | | — | — |
| **QSPI** | | | | | | |
| QSPI_CS[3:2] | PQSPI[6:5] | PWM[3:2] | DACK[3:2] | O | R13, N12 | P10, N9 |
| QSPI_CS1 | PQSPI[4] | — | — | O | T14 | N10 |
| QSPI_CS0 | PQSPI[3] | — | — | O | P12 | M9 |
| QSPI_CLK | PQSPI[2] | I2C_SCL | — | O | T15 | L11 |
| QSPI_DIN | PQSPI[1] | I2C_SDA | — | I | T13 | M10 |
| QSPI_DOUT | PQSPI[0] | — | — | O | R12 | L10 |
| **UARTs** | | | | | | |
| U2RXD | PUARTH[3] | — | — | I | T9 | — |
| U2TXD | PUARTH[2] | — | — | O | R9 | — |
| $\overline{\text{U2CTS}}$ | PUARTH[1] | PWM1 | — | I | P9 | — |
| $\overline{\text{U2RTS}}$ | PUARTH[0] | PWM0 | — | O | R8 | — |
| U1RXD | PUARTL[7] | — | — | I | A9 | A6 |
| U1TXD | PUARTL[6] | — | — | O | B9 | D7 |
| $\overline{\text{U1CTS}}$ | PUARTL[5] | — | — | I | C9 | C7 |
| $\overline{\text{U1RTS}}$ | PUARTL[4] | — | — | O | D9 | B6 |
| U0RXD | PUARTL[3] | — | — | I | A8 | A4 |
| U0TXD | PUARTL[2] | — | — | O | B8 | A5 |
| $\overline{\text{U0CTS}}$ | PUARTL[1] | — | — | I | C8 | C6 |

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274 MCF5275 256 MAPBGA | MCF5274L MCF5275L 196 MAPBGA |
|---|---|---|---|---|---|---|
| $\overline{\text{U0RTS}}$ | PUARTL[0] | — | — | O | D7 | B5 |
| **USB** | | | | | | |
| USB_SPEED | PUSBH[0] | — | — | I/O | G14 | G11 |
| USB_CLK | PUSBL[7] | — | — | I | G15 | F12 |
| USB_RN | PUSBL[6] | — | — | I | J16 | H13 |
| USB_RP | PUSBL[5] | — | — | I | J15 | J11 |
| USB_RXD | PUSBL[4] | — | — | I | L15 | L14 |
| USB_SUSP | PUSBL[3] | — | — | O | M13 | N13 |
| USB_TN | PUSBL[2] | — | — | O | K14 | J14 |
| USB_TP | PUSBL[1] | — | — | O | K15 | J12 |
| USB_TXEN | PUSBL[0] | — | — | O | L14 | K13 |
| **Timers (and PWMs)** | | | | | | |
| DT3IN | PTIMERH[3] | DT3OUT | $\overline{\text{U2RTS}}$ | I | J4 | G2 |
| DT3OUT | PTIMERH[2] | PWM3 | $\overline{\text{U2CTS}}$ | O | K3 | G1 |
| DT2IN | PTIMERH[1] | DT2OUT | — | I | J2 | F3 |
| DT2OUT | PTIMERH[0] | PWM2 | — | O | J3 | F4 |
| DT1IN | PTIMERL[3] | DT1OUT | — | I | H1 | F1 |
| DT1OUT | PTIMERL[2] | PWM1 | — | O | H2 | F2 |
| DT0IN | PTIMERL[1] | DT0OUT | — | I | H3 | E1 |
| DT0OUT | PTIMERL[0] | PWM0 | — | O | G3 | E2 |
| **BDM/JTAG[2]** | | | | | | |
| DSCLK | — | $\overline{\text{TRST}}$ | — | I | P14 | P13 |
| PSTCLK | — | TCLK | — | O | P16 | P12 |
| $\overline{\text{BKPT}}$ | — | TMS | — | I | R15 | N12 |
| DSI | — | TDI | — | I | R16 | M12 |
| DSO | — | TDO | — | O | P15 | K11 |
| JTAG_EN | — | — | — | I | R14 | P11 |
| DDATA[3:0] | — | — | — | O | P10, N10, P11, N11 | M7, N7, P8, L9 |
| PST[3:0] | — | — | — | O | T10, R10, T11, R11 | P7, L8, M8, N8 |
| **Test** | | | | | | |

**Table 2. MCF5274 and MCF5275 Signal Information and Muxing (continued)**

| Signal Name | GPIO | Alternate1 | Alternate2 | Dir.[1] | MCF5274 MCF5275 256 MAPBGA | MCF5274L MCF5275L 196 MAPBGA |
|---|---|---|---|---|---|---|
| TEST | — | — | — | I | N9 | N6 |
| PLL_TEST | — | — | — | I | M14 | — |
| **Power Supplies** | | | | | | |
| VDDPLL | — | — | — | I | M15 | M13 |
| VSSPLL | — | — | — | I | K16 | L13 |
| VSS | — | — | — | I | A1, A10, A16, E5, E12, F6, F11, G7:10, H7:10, J1, J7:10, K7:10, L6, L11, M5, N16, R7, T1, T16 | F7, F8, G6:9, H6:9, J7, J8 |
| OVDD | — | — | — | I | E6:8, F5, F7, F8, G5, G6, H5, H6, J11, J12, K11, K12, L9, L10, L12, M9:11 | E5:7, F5, F6, H10, J9, J10, K8:10 |
| VDD | — | — | — | I | D8, H13, K4, N8 | D6, G5, G12, L7 |
| SD_VDD | — | — | — | I | E9:11, F9, F10, F12, G11, G12, H11, H12, J5, J6, K5, K6, L5, L7, L8, M6, M7, M8 | E8:10, F9, F10, G10, H5, J5, J6, K5:7 |

1 Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.

2 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

# 5 Design Recommendations

## 5.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk

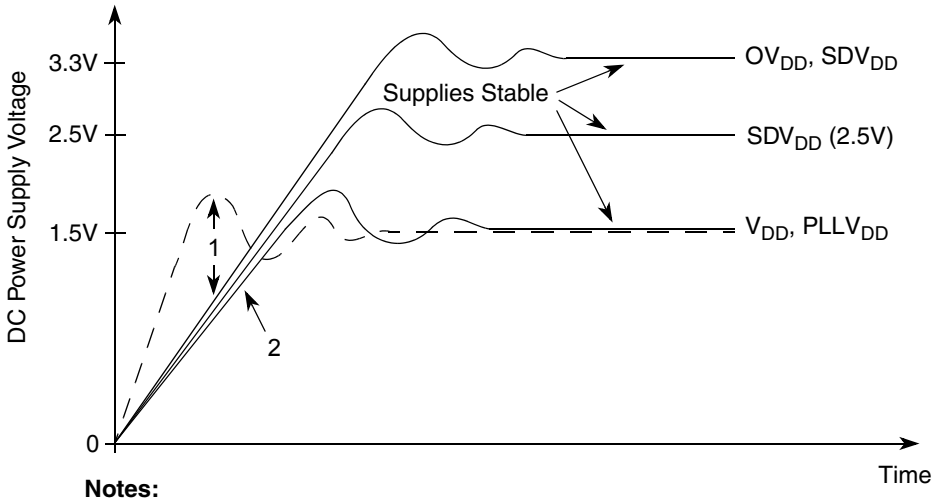
analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

## 5.2 Power Supply

- 33uF, 0.1 µF, and 0.01 µF across each power supply

### 5.2.1 Supply Voltage Sequencing and Separation Cautions

Figure 2 shows situations in sequencing the I/O $V_{DD}$ ($OV_{DD}$), SDRAM $V_{DD}$ ($SDV_{DD}$), PLL $V_{DD}$ ($PLLV_{DD}$), and Core $V_{DD}$ ($V_{DD}$).




**Notes:**
1. VDD should not exceed OVDD, SDVDD or PLLVDD by more than 0.4 V at any time, including power-up.
2. Recommended that VDD/PLLVDD should track OVDD/SDVDD up to 0.9 V, then separate for completion of ramps.
3. Input voltage must not be greater than the supply voltage (OVDD, SDVDD, VDD, or PLLVDD) by more than 0.5 V at any time, including during power-up.
4. Use 1 ms or slower rise time for all supplies.

**Figure 2. Supply Voltage Sequencing and Separation Cautions**

The relationship between $SDV_{DD}$ and $OV_{DD}$ is non-critical during power-up and power-down sequences. Both $SDV_{DD}$ (2.5V or 3.3V) and $OV_{DD}$ are specified relative to $V_{DD}$.

#### 5.2.1.1 Power Up Sequence

If $OV_{DD}$/$SDV_{DD}$ are powered up with $V_{DD}$ at 0 V, then the sense circuits in the I/O pads will cause all pad output drivers connected to the $OV_{DD}$/$SDV_{DD}$ to be in a high impedance state. There is no limit on how long after $OV_{DD}$/$SDV_{DD}$ powers up before $V_{DD}$ must powered up. $V_{DD}$ should not lead the $OV_{DD}$, $SDV_{DD}$ or $PLLV_{DD}$ by more than 0.4 V during power ramp-up, or there will be high current in the internal ESD protection diodes. The rise times on the power supplies should be slower than 1 µs to avoid turning on the internal ESD protection clamp diodes.

The recommended power up sequence is as follows:

1. Use 1 µs or slower rise time for all supplies.

2. $V_{DD}$/$PLLV_{DD}$ and $OV_{DD}$/$SDV_{DD}$ should track up to 0.9 V, then separate for the completion of ramps with $OV_{DD}$/SD $V_{DD}$ going to the higher external voltages. One way to accomplish this is to use a low drop-out voltage regulator.

#### 5.2.1.2 Power Down Sequence

If $V_{DD}$/$PLLV_{DD}$ are powered down first, then sense circuits in the I/O pads will cause all output drivers to be in a high impedance state. There is no limit on how long after $V_{DD}$ and $PLLV_{DD}$ power down before $OV_{DD}$ or $SDV_{DD}$ must power down. $V_{DD}$ should not lag $OV_{DD}$, $SDV_{DD}$, or $PLLV_{DD}$ going low by more than 0.4 V during power down or there will be undesired high current in the ESD protection diodes. There are no requirements for the fall times of the power supplies.

The recommended power down sequence is as follows:

1. Drop $V_{DD}$/$PLLV_{DD}$ to 0 V.
2. Drop $OV_{DD}$/$SDV_{DD}$ supplies.

## 5.3 Decoupling

- Place the decoupling capacitors as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1 µF and 0.01 µF at each supply input

## 5.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See electricals.

## 5.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

## 5.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

# 5.7 Interface Recommendations

## 5.7.1 DDR SDRAM Controller

### 5.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 3 shows the behavior of SDRAM signals in synchronous mode.

**Table 3. Synchronous DRAM Signal Connections**

| Signal | Description |
|---|---|
| $\overline{\text{SD\_SRAS}}$ | Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SDRAM\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals. |
| $\overline{\text{SD\_SCAS}}$ | Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM. |
| $\overline{\text{SD\_WE}}$ | DRAM read/write. Asserted for write operations and negated for read operations. |
| $\overline{\text{SD\_CS}}$[1:0] | Row address strobe. Select each memory block of SDRAMs connected to the MCF5275. One $\overline{\text{SDRAM\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals. |
| SD_CKE | Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality. |
| $\overline{\text{BS}}$[3:2] | Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:2] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs. |
| DDR_CLKOUT | Bus clock output. Connects to the CLK input of SDRAMs. |

### 5.7.1.2 Address Multiplexing

See the SDRAM controller module chapter in the *MCF5275 Reference Manual* for details on address multiplexing.

## 5.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 4.

**Table 4. MII Mode**

| Signal Description | MCF5275 Pin |
|---|---|
| Transmit clock | FEC*n*_TXCLK |
| Transmit enable | FEC*n*_TXEN |
| Transmit data | FEC*n*_TXD[3:0] |
| Transmit error | FEC*n*_TXER |

**Table 4. MII Mode (continued)**

| Signal Description | MCF5275 Pin |
|---|---|
| Collision | FEC*n*_COL |
| Carrier sense | FEC*n*_CRS |
| Receive clock | FEC*n*_RXCLK |
| Receive enable | FEC*n*_RXDV |
| Receive data | FEC*n*_RXD[3:0] |
| Receive error | FEC*n*_RXER |
| Management channel clock | FEC*n*_MDC |
| Management channel serial data | FEC*n*_MDIO |

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5275 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 5.

**Table 5. Seven-Wire Mode Configuration**

| Signal Description | MCF5275 Pin |
|---|---|
| Transmit clock | FEC*n*_TXCLK |
| Transmit enable | FEC*n*_TXEN |
| Transmit data | FEC*n*_TXD[0] |
| Collision | FEC*n*_COL |
| Receive clock | FEC*n*_RXCLK |
| Receive enable | FEC*n*_RXDV |
| Receive data | FEC*n*_RXD[0] |
| Unused, configure as PB14 | FEC*n*_RXER |
| Unused input, tie to ground | FEC*n*_CRS |
| Unused, configure as PB[13:11] | FEC*n*_RXD[3:1] |
| Unused output, ignore | FEC*n*_TXER |
| Unused, configure as PB[10:8] | FEC*n*_TXD[3:1] |
| Unused, configure as PB15 | FEC*n*_MDC |
| Input after reset, connect to ground | FEC*n*_MDIO |

Refer to the M5275EVBevaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5275 site by navigating to: http://www.freescale.com/coldfire.

### 5.7.3 BDM

Use the BDM interface as shown in the M5275EVB evaluation board user's manual. The schematics for this board are accessible at the MCF5275 site by navigating to: http://www.freescale.com/coldfire.

# 6 Mechanicals/Pinouts

## 6.1 256 MAPBGA Pinout

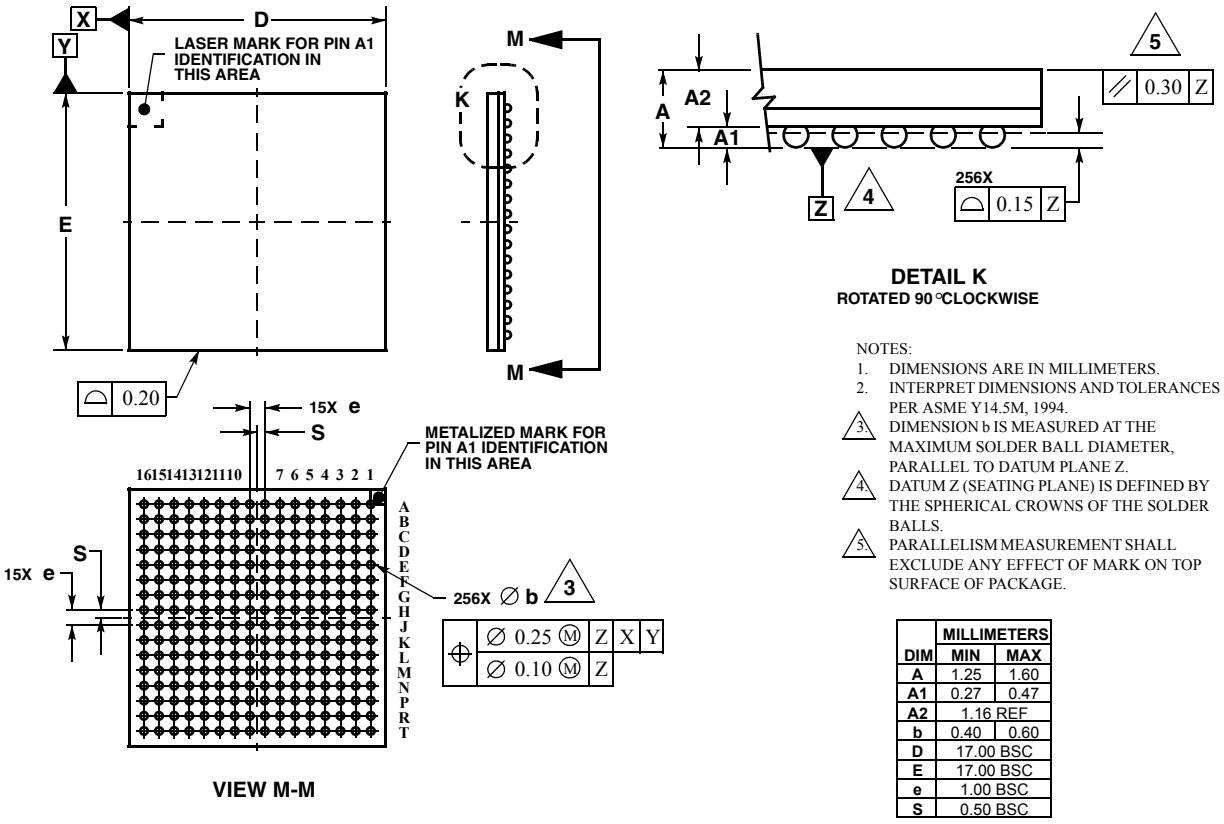
Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | FEC1_ RXD1 | FEC1_ RXDV | FEC1_ CRS | FEC1_ COL | FEC0_ COL | FEC0_ MDIO | U0RXD | U1RXD | VSS | A23 | A20 | A17 | A14 | SD_ VREF | VSS | A |
| B | FEC1_ RXD3 | FEC1_ RXD2 | FEC1_ RXD0 | FEC1_ RXCLK | FEC0_ RXDV | FEC0_ RXCLK | FEC0_ MDC | U0TXD | U1TXD | I2C_ SDA | A22 | A19 | A16 | A13 | A11 | A9 | B |
| C | FEC1_ TXCLK | FEC1_ RXER | FEC0_ TXCLK | FEC0_ RXER | FEC0_ RXD2 | FEC0_ RXD0 | FEC0_ CRS | $\overline{\text{U0CTS}}$ | $\overline{\text{U1CTS}}$ | I2C_ SCL | A21 | A18 | A15 | A12 | A10 | A8 | C |
| D | FEC1_ TXER | FEC1_ TXEN | FEC0_ TXER | FEC0_ TXEN | FEC0_ RXD3 | FEC0_ RXD1 | $\overline{\text{U0RTS}}$ | VDD | $\overline{\text{U1RTS}}$ | $\overline{\text{CS7}}$ | $\overline{\text{CS6}}$ | $\overline{\text{CS5}}$ | $\overline{\text{CS4}}$ | A7 | A6 | TSIZ1 | D |
| E | FEC1_ TXD3 | FEC1_ TXD2 | FEC0_ TXD3 | NC | VSS | OVDD | OVDD | OVDD | SD_VDD | SD_VDD | SD_VDD | VSS | $\overline{\text{CS3}}$ | A5 | A4 | A3 | E |
| F | FEC1_ TXD0 | FEC1_ TXD1 | FEC0_ TXD2 | FEC0_ TXD1 | OVDD | VSS | OVDD | OVDD | SD_VDD | SD_VDD | VSS | SD_VDD | $\overline{\text{CS2}}$ | A2 | A1 | A0 | F |
| G | FEC1_ MDIO | FEC1_ MDC | DT0OUT | FEC0_ TXD0 | OVDD | OVDD | VSS | VSS | VSS | VSS | SD_VDD | SD_VDD | $\overline{\text{IRQ7}}$ | USB_ SPEED | USB_ CLK | TSIZ0 | G |
| H | DT1IN | DT1OUT | DT0IN | NC | OVDD | OVDD | VSS | VSS | VSS | VSS | SD_VDD | SD_VDD | VDD | $\overline{\text{IRQ4}}$ | $\overline{\text{IRQ5}}$ | $\overline{\text{IRQ6}}$ | H |
| J | VSS | DT2IN | DT2OUT | DT3IN | SD_VDD | SD_VDD | VSS | VSS | VSS | VSS | OVDD | OVDD | $\overline{\text{IRQ2}}$ | $\overline{\text{IRQ3}}$ | USB_RP | USB_RN | J |
| K | $\overline{\text{OE}}$ | $\overline{\text{SD_WE}}$ | DT3OUT | VDD | SD_VDD | SD_VDD | VSS | VSS | VSS | VSS | OVDD | OVDD | $\overline{\text{IRQ1}}$ | USB_TN | USB_TP | VSSPLL | K |
| L | $\overline{\text{SD_ SCAS}}$ | $\overline{\text{SD_ SRAS}}$ | SD_CKE | $\overline{\text{TS}}$ | SD_VDD | VSS | SD_VDD | SD_VDD | OVDD | OVDD | VSS | OVDD | $\overline{\text{TA}}$ | USB_ TXEN | USB_ RXD | EXTAL | L |
| M | D31 | $\overline{\text{SD_CS1}}$ | $\overline{\text{BS3}}$ | SD_DQS3 | VSS | SD_VDD | SD_VDD | SD_VDD | OVDD | OVDD | OVDD | NC | USB_ SUSP | PLL_ TEST | VDDPLL | XTAL | M |
| N | D30 | D29 | D28 | D20 | D16 | SD_A10 | $\overline{\text{CS1}}$ | VDD | TEST | DDATA2 | DDATA0 | QSPI_ CS2 | CLK MOD1 | $\overline{\text{RSTOUT}}$ | $\overline{\text{RESET}}$ | VSS | N |
| P | D27 | D26 | D23 | D19 | SD_DQS2 | $\overline{\text{TIP}}$ | R/$\overline{\text{W}}$ | $\overline{\text{RCON}}$ | $\overline{\text{U2CTS}}$ | DDATA3 | DDATA1 | QSPI_ CS0 | CLK MOD0 | $\overline{\text{TRST}}$/ DSCLK | TDO/ DSO | TCLK/ PSTCLK | P |
| R | D25 | D24 | D22 | D18 | $\overline{\text{BS2}}$ | $\overline{\text{CS0}}$ | VSS | $\overline{\text{U2RTS}}$ | U2TXD | PST2 | PST0 | QSPI_ DOUT | QSPI_ CS3 | JTAG_ EN | TMS/ $\overline{\text{BKPT}}$ | TDI/DSI | R |
| T | VSS | SD_ VREF | D21 | D17 | $\overline{\text{SD_CS0}}$ | $\overline{\text{DDR_CLK OUT}}$ | DDR_CLK OUT | $\overline{\text{TEA}}$ | U2RXD | PST3 | PST1 | CLKOUT | QSPI_ DIN | QSPI_ CS1 | QSPI_ CLK | VSS | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

**Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)**

## 6.2 Package Dimensions - 256 MAPBGA

Figure 6 shows MCF5275 256 MAPBGA package dimensions.




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| DIM | MILLIMETERS MIN | MAX |
|---|---|---|
| A | 1.25 | 1.60 |
| A1 | 0.27 | 0.47 |
| A2 | 1.16 REF | |
| b | 0.40 | 0.60 |
| D | 17.00 BSC | |
| E | 17.00 BSC | |
| e | 1.00 BSC | |
| S | 0.50 BSC | |

**Figure 4. 256 MAPBGA Package Dimensions**

## 6.3 196 MAPBGA Pinout

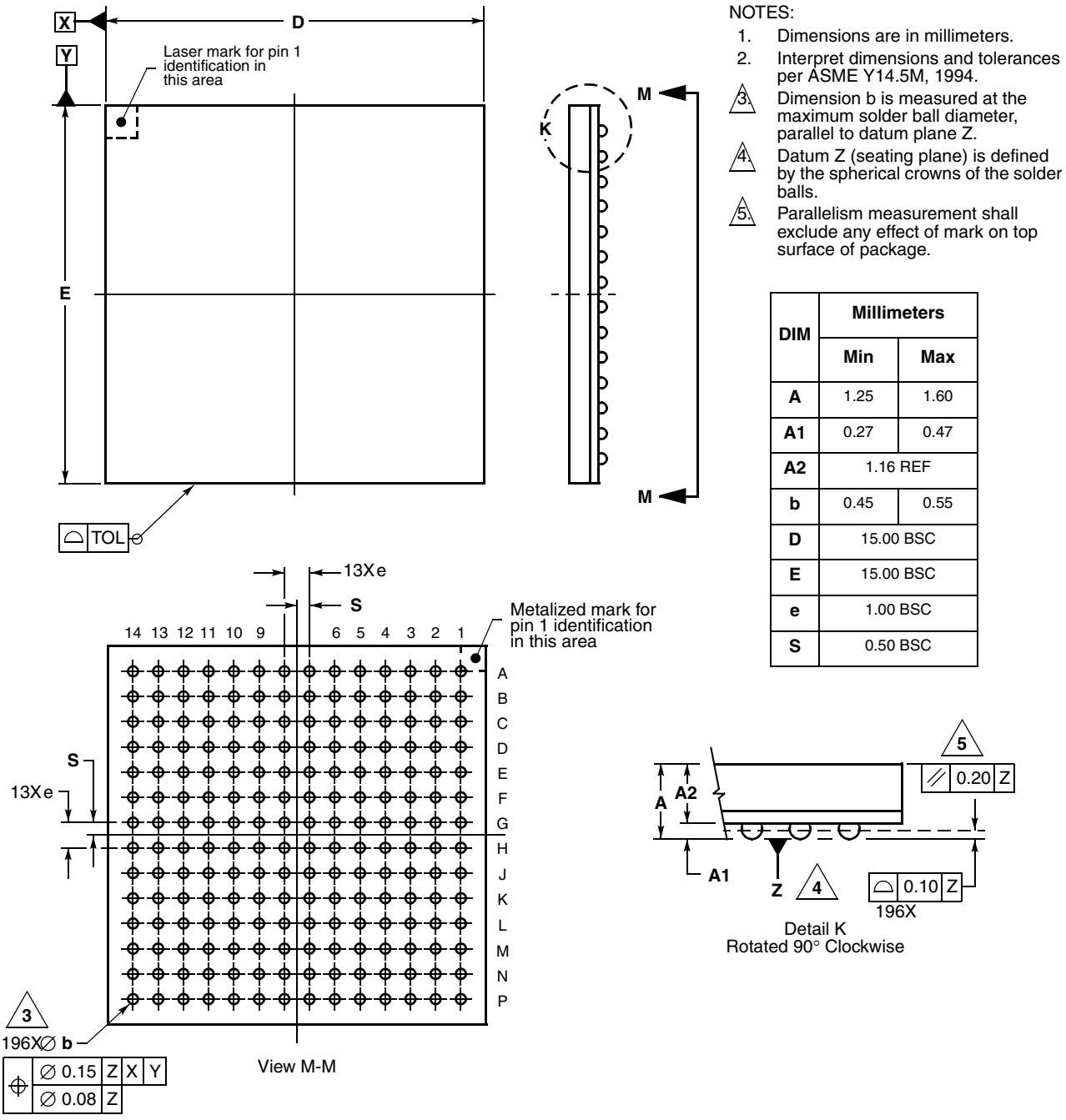
Figure 5 is a consolidated MCF5274L/75L pinout for the 196 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | NC | FEC0_ CRS | FEC0_ MDIO | U0RXD | U0TXD | U1RXD | I2C_SCL | A23 | $\overline{\text{CS6}}$ | $\overline{\text{CS5}}$ | A15 | A12 | SD_ VREF | NC | A |
| B | FEC0_ RXD2 | FEC0_ RXD1 | FEC0_ RXCLK | FEC0_ COL | $\overline{\text{U0RTS}}$ | $\overline{\text{U1RTS}}$ | I2C_SDA | A22 | A20 | A16 | A13 | $\overline{\text{CS3}}$ | A9 | TSIZ1 | B |
| C | FEC0_ TXCLK | FEC0_ TXER | FEC0_ TXEN | FEC0_ RXDV | FEC0_ MDC | $\overline{\text{U0CTS}}$ | $\overline{\text{U1CTS}}$ | A21 | A18 | A17 | A14 | A10 | A8 | $\overline{\text{CS2}}$ | C |
| D | FEC0_ TXD3 | FEC0_ TXD0 | FEC0_ TXD1 | FEC0_ RXD3 | FEC0_ RXD0 | VDD | U1TXD | $\overline{\text{CS7}}$ | A19 | $\overline{\text{CS4}}$ | A11 | A7 | A5 | A2 | D |
| E | DT0IN | DT0OUT | FEC0_ TXD2 | FEC0_ RXER | OVDD | OVDD | OVDD | SD_VDD2 | SD_VDD2 | SD_VDD2 | A6 | A4 | A1 | TSIZ0 | E |
| F | DT1IN | DT1OUT | DT2IN | DT2OUT | OVDD | OVDD | VSS | VSS | SD_VDD2 | SD_VDD2 | A3 | USB_CLK | A0 | $\overline{\text{IRQ7}}$ | F |
| G | DT3OUT | DT3IN | $\overline{\text{SD_CAS}}$ | $\overline{\text{SD_WE}}$ | VDD | VSS | VSS | VSS | VSS | SD_VDD2 | USB_ SPEED | VDD | $\overline{\text{IRQ6}}$ | $\overline{\text{IRQ5}}$ | G |
| H | $\overline{\text{SD_SRAS}}$ | $\overline{\text{TS}}$ | $\overline{\text{SD_CS1}}$ | $\overline{\text{OE}}$ | SD_VDD1 | VSS | VSS | VSS | VSS | OVDD | $\overline{\text{IRQ4}}$ | $\overline{\text{IRQ2}}$ | USB_RN | $\overline{\text{IRQ3}}$ | H |
| J | SD_CKE | SD_DQS3 | D31 | D22 | SD_VDD1 | SD_VDD1 | VSS | VSS | OVDD | OVDD | USB_RP | USB_TP | $\overline{\text{IRQ1}}$ | USB_TN | J |
| K | $\overline{\text{BS3}}$ | D29 | D28 | D23 | SD_VDD1 | SD_VDD1 | SD_VDD1 | OVDD | OVDD | OVDD | TDO/DSO | $\overline{\text{RESET}}$ | USB_ TXEN | $\overline{\text{TA}}$ | K |
| L | D30 | D26 | D25 | D24 | $\overline{\text{BS2}}$ | R/$\overline{\text{W}}$ | VDD | PST2 | DDATA0 | QSPI_ DOUT | QSPI_CLK | $\overline{\text{RSTOUT}}$ | VSSPLL | USB_RXD | L |
| M | D27 | D21 | D18 | D17 | $\overline{\text{SD_CS0}}$ | $\overline{\text{RCON}}$ | DDATA3 | PST1 | QSPI_ CS0 | QSPI_DIN | CLKMOD1 | TDI/DSI | VDDPLL | EXTAL | M |
| N | D20 | D19 | D16 | SD_A10 | $\overline{\text{CS0}}$ | TEST | DDATA2 | PST0 | QSPI_ CS2 | QSPI_ CS1 | CLKMOD0 | TMS/$\overline{\text{BKPT}}$ | USB_ SUSP | XTAL | N |
| P | NC | SD_ VREF | SD_DQS2 | $\overline{\text{CS1}}$ | $\overline{\text{DDR_CLK OUT}}$ | DDR_CLK OUT | PST3 | DDATA1 | CLKOUT | QSPI_ CS3 | JTAG_EN | TCLK/PST CLK | $\overline{\text{TRST}}$/DSC LK | NC | P |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

**Figure 5. MCF5274L and MCF5275L Pinout (196 MAPBGA)**

## 6.4 Package Dimensions - 196 MAPBGA

Figure 6 shows MCF5275 196 MAPBGA package dimensions.




NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension b is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

| DIM | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 1.25 | 1.60 |
| A1 | 0.27 | 0.47 |
| A2 | 1.16 REF | |
| b | 0.45 | 0.55 |
| D | 15.00 BSC | |
| E | 15.00 BSC | |
| e | 1.00 BSC | |
| S | 0.50 BSC | |

**Figure 6. 196 MAPBGA Package Dimensions**

# 7 Ordering Information

**Table 6. Orderable Part Numbers**

| Freescale Part Number | Description | Speed | Temperature |
|---|---|---|---|
| MCF5274LVM133 | MCF5274L RISC Microprocessor, 196 MAPBGA | 133MHz | 0° to +70° C |
| MCF5274LVM166 | MCF5274L RISC Microprocessor, 196 MAPBGA | 166MHz | 0° to +70° C |
| MCF5274VM133 | MCF5274 RISC Microprocessor, 256 MAPBGA | 133MHz | 0° to +70° C |
| MCF5274VM166 | MCF5274 RISC Microprocessor, 256 MAPBGA | 166MHz | 0° to +70° C |
| MCF5275LCVM133 | MCF5275L RISC Microprocessor, 196 MAPBGA | 133MHz | -40° to +85° C |
| MCF5275LCVM166 | MCF5275L RISC Microprocessor, 196 MAPBGA | 166MHz | -40° to +85° C |
| MCF5275CVM133 | MCF5275 RISC Microprocessor, 256 MAPBGA | 133MHz | -40° to +85° C |
| MCF5275CVM166 | MCF5275 RISC Microprocessor, 256 MAPBGA | 166MHz | -40° to +85° C |

# 8 Preliminary Electrical Characteristics

This appendix contains electrical specification tables and reference timing diagrams for the MCF5275 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5275.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

**NOTE**

The parameters specified in this appendix supersede any values found in the module specifications.

## 8.1 Maximum Ratings

**Table 7. Absolute Maximum Ratings[1, 2]**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | – 0.5 to +2.0 | V |
| I/O Pad Supply Voltage (3.3V) | $OV_{DD}$ | – 0.3 to +4.0 | V |
| Memory Interface SSTL 2.5V Pad Supply Voltage | $SDV_{DD}$ | – 0.3 to + 2.8 | V |
| Memory Interface SSTL 3.3V Pad Supply Voltage | $SDV_{DD}$ | – 0.3 to +4.0 | V |
| PLL Supply Voltage | $V_{DDPLL}$ | – 0.3 to +4.0 | V |
| Digital Input Voltage [3] | $V_{IN}$ | – 0.3 to + 4.0 | V |
| EXTAL pin voltage | $V_{EXTAL}$ | 0 to 3.3 | V |
| XTAL pin voltage | $V_{XTAL}$ | 0 to 3.3 | V |

**Table 7. Absolute Maximum Ratings[1, 2] (continued)**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Instantaneous Maximum Current<br>Single pin limit (applies to all pins) [4, 5] | $I_D$ | 25 | mA |
| Operating Temperature Range (Packaged) | $T_A$<br>($T_L$ - $T_H$) | – 40 to 85 | °C |
| Storage Temperature Range | $T_{stg}$ | – 65 to 150 | °C |

1 Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

2 This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or O $V_{DD}$).

3 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

4 All functional non-supply pins are internally clamped to $V_{SS}$ and O $V_{DD}$.

5 Power supply must maintain regulation within operating O $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in}$ > O $V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of O $V_{DD}$ and could result in external power supply going out of regulation. Insure external O $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock).Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions.

## 8.2 Thermal Characteristics

Table 8 lists thermal resistance values

**Table 8. Thermal characteristics**

| Characteristic | | Symbol | 256MBGA | 196MBGA | Unit |
|---|---|---|---|---|---|
| Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JMA}$ | 26[1,2] | 32[1,2] | °C/W |
| Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 23[1,2] | 29[1,2] | °C/W |
| Junction to board | | $\theta_{JB}$ | 15[3] | 20[3] | °C/W |
| Junction to case | | $\theta_{JC}$ | 10[4] | 10[4] | °C/W |
| Junction to top of package | Natural convection | $\Psi_{jt}$ | 2[1,5] | 2[1,5] | °C/W |
| Maximum operating junction temperature | | $T_j$ | 105 | 105 | °C |

1 $\theta_{JMA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JmA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-6 with the board horizontal.

3 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature ($T_J$) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

$T_A$ = Ambient Temperature, °C
$\Theta_{JMA}$ = Package Thermal Resistance, Junction-to-Ambient, °C/W
$P_D$ = $P_{INT} + P_{I/O}$
$P_{INT}$ = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between $P_D$ and $T_J$ (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K, the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## 8.3 ESD Protection

**Table 9. ESD Protection Characteristics[1, 2]**

| Characteristics | Symbol | Value | Units |
|---|---|---|---|
| ESD Target for Human Body Model | HBM | 2000 | V |
| ESD Target for Machine Model | MM | 200 | V |
| HBM Circuit Description | $R_{series}$ | 1500 | Ω |
| | C | 100 | pF |
| MM Circuit Description | $R_{series}$ | 0 | Ω |
| | C | 200 | pF |
| Number of pulses per pin (HBM)<br>positive pulses<br>negative pulses | <br>—<br>— | <br>1<br>1 | — |
| Number of pulses per pin (MM)<br>positive pulses<br>negative pulses | <br>—<br>— | <br>3<br>3 | — |
| Interval of Pulses | — | 1 | sec |

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 8.4 DC Electrical Specifications

**Table 10. DC Electrical Specifications[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | 1.4 | 1.6 | V |
| I/O Pad Supply Voltage | $OV_{DD}$ | 3.0 | 3.6 | V |
| SSTL I/O Pad Supply Voltage | $SDV_{DD}$ | 2.3 | 2.7 | V |
| SSTL I/O Pad Supply Voltage | $SDV_{DD}$ | 3.0 | 3.6 | V |
| SSTL Memory pads reference voltage (SD $V_{DD}$ = 2.5V) | $V_{REF}$ | 0.5 SD $V_{DD}$ | —[2] | V |
| SSTL Memory pads reference voltage (SD $V_{DD}$ = 3.3V) | $V_{REF}$ | 0.45 SD $V_{DD}$ | —[2] | V |
| Input High Voltage 3.3V I/O Pads | $V_{IH}$ | 0.7 x $OV_{DD}$ | 3.6 | V |
| Input Low Voltage 3.3V I/O Pads | $V_{IL}$ | $V_{SS}$ – 0.3 | 0.35 x $OV_{DD}$ | V |
| Output High Voltage 3.3V I/O Pads<br>$I_{OH}$ = –2.0 mA | $V_{OH}$ | $OV_{DD}$ - 0.5 | — | V |
| Output Low Voltage 3.3V I/O Pads<br>$I_{OL}$ = 2.0mA | $V_{OL}$ | — | 0.5 | V |
| Input Hysteresis 3.3V I/O Pads | $V_{HYS}$ | 0.06 x $V_{DD}$ | — | mV |
| Input High Voltage SSTL 3.3V/2.5V[3] | $V_{IH}$ | $V_{REF}$ + 0.3 | $SDV_{DD}$ + 0.3 | V |
| Input Low Voltage SSTL 3.3V/2.5V[3] | $V_{IL}$ | $V_{SS}$ - 0.3 | $V_{REF}$ - 0.3 | V |
| Output High Voltage SSTL 3.3V/2.5V[4]<br>$I_{OH}$ = –5.0 mA | $V_{OH}$ | $SDV_{DD}$ - 0.25V | — | V |
| Output Low Voltage SSTL 3.3V/2.5V[4]<br>$I_{OL}$ = 5.0 mA | $V_{OL}$ | — | 0.35 | V |
| Input Leakage Current<br>$V_{in}$ = $V_{DD}$ or $V_{SS}$, Input-only pins | $I_{in}$ | -1.0 | 1.0 | µA |
| High Impedance (Off-State) Leakage Current<br>$V_{in}$ = $V_{DD}$ or $V_{SS}$, All input/output and output pins | $I_{OZ}$ | -1.0 | 1.0 | µA |
| Weak Internal Pull Up Device Current, tested at $V_{IL}$ Max.[5] | $I_{APU}$ | -10 | -130 | µA |
| Input Capacitance [6]<br>All input-only pins<br>All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |
| Load Capacitance[7]<br>Low Drive Strength<br>High Drive Strength | $C_L$ | | <br>25<br>50 | pF |
| Core Operating Supply Current [8]<br>Master Mode<br>WAIT<br>DOZE<br>STOP | $I_{DD}$ | <br>—<br>—<br>—<br>— | <br>175<br>15<br>10<br>100 | <br>mA<br>mA<br>mA<br>µA |
| I/O Pad Operating Supply Current<br>Master Mode<br>Low Power Modes | $OI_{DD}$ | <br>—<br>— | <br>250<br>250 | <br>mA<br>µA |
| DC Injection Current [3, 9, 10, 11]<br>$V_{NEGCLAMP}$ =$V_{SS}$– 0.3 V, $V_{POSCLAMP}$ = $V_{DD}$ + 0.3<br>Single Pin Limit<br>Total MCU Limit, Includes sum of all stressed pins | $I_{IC}$ | <br><br>-1.0<br>-10 | <br><br>1.0<br>10 | mA |

1 Refer to Table 11 for additional PLL specifications.
2 $V_{REF}$ is specified as a nominal value only instead of a range, so no maximum value is listed.
3 This specification is guaranteed by design and is not 100% tested.

4 The actual $V_{OH}$ and $V_{OL}$ values for SSTL pads are dependent on the termination and drive strength used. The specifications numbers assume no parallel termination.

5 Refer to the MCF5274 signals chapter for pins having weak internal pull-up devices.

6 This parameter is characterized before qualification rather than 100% tested.

7 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.

8 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.

9 All functional non-supply pins are internally clamped to $V_{SS}$ and their respective $V_{DD}$.

10 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

11 Power supply must maintain regulation within operating $V_{DD}$ range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than $I_{DD}$, the injection current may flow out of $V_{DD}$ and could result in external power supply going out of regulation. Insure external $V_{DD}$ load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

## 8.5 Oscillator and Phase Lock Loop (PLLMRFM) Electrical Specifications

**Table 11. PLL Electrical Specifications[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| PLL Reference Frequency Range<br>Crystal reference<br>External reference<br>1:1 Mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$) | <br>$f_{ref\_crystal}$<br>$f_{ref\_ext}$<br>$f_{ref\_1:1}$ | <br>8<br>8<br>24 | <br>25<br>25<br>83 | MHz |
| Core frequency<br>CLKOUT Frequency [2]<br>External reference<br>On-Chip PLL Frequency | $f_{core}$<br><br><br>$f_{sys/2}$ | <br><br>0<br>$f_{ref}$ / 32 | 166<br><br>83<br>83 | MHz<br><br>MHz<br>MHz |
| Loss of Reference Frequency [3, 5] | $f_{LOR}$ | 100 | 1000 | kHz |
| Self Clocked Mode Frequency [4, 5] | $f_{SCM}$ | TBD | TBD | MHz |
| Crystal Start-up Time [5, 6] | $t_{cst}$ | — | 10 | ms |
| EXTAL Input High Voltage<br>Crystal Mode<br>All other modes (Dual Controller (1:1), Bypass, External) | $V_{IHEXT}$<br>$V_{IHEXT}$ | <br>TBD<br>TBD | <br>TBD<br>TBD | V |
| EXTAL Input Low Voltage<br>Crystal Mode<br>All other modes (Dual Controller (1:1), Bypass, External) | $V_{ILEXT}$<br>$V_{ILEXT}$ | <br>TBD<br>TBD | <br>TBD<br>TBD | V |
| XTAL Output High Voltage<br>$I_{OH}$ = 1.0 mA | $V_{OH}$ | <br>TBD | <br>— | V |
| XTAL Output Low Voltage<br>$I_{OL}$ = 1.0 mA | $V_{OL}$ | <br>— | <br>TBD | V |
| XTAL Load Capacitance[7] | | 5 | 30 | pF |
| PLL Lock Time [8] | $t_{lpll}$ | — | 750 | µs |
| Power-up To Lock Time [6, 9]<br>With Crystal Reference<br>Without Crystal Reference[10] | $t_{lplk}$ | <br>—<br>— | <br>11<br>750 | <br>ms<br>µs |

**Table 11. PLL Electrical Specifications[1] (continued)**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| 1:1 Mode Clock Skew (between CLKOUT and EXTAL) [11] | $t_{skew}$ | -1 | 1 | ns |
| Duty Cycle of reference [5] | $t_{dc}$ | 40 | 60 | % $f_{sys/2}$ |
| Frequency un-LOCK Range | $f_{UL}$ | -3.8 | 4.1 | % $f_{sys/2}$ |
| Frequency LOCK Range | $f_{LCK}$ | -1.7 | 2.0 | % $f_{sys/2}$ |
| CLKOUT Period Jitter, [5, 6, 9,12, 13] Measured at $f_{sys/2}$ Max<br>Peak-to-peak Jitter (Clock edge to clock edge)<br>Long Term Jitter (Averaged over 2 ms interval) | $C_{jitter}$ | <br>—<br>— | <br>5<br>.01 | % $f_{sys/2}$ |
| Frequency Modulation Range Limit[14, 15]<br>($f_{sys/2}$Max must not be exceeded) | $C_{mod}$ | 0.8 | 2.2 | % $f_{sys/2}$ |
| ICO Frequency. $f_{ico} = f_{ref} * 2 * (MFD+2)$[16] | $f_{ico}$ | 48 | 83 | MHz |

1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below $f_{LOR}$ with default MFD/RFD settings.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 Proper PC board layout procedures must be followed to achieve specifications.
7 Load Capacitance determined from crystal manufacturer specifications and will include circuit board parasitics.
8 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
9 Assuming a reference is available at power up, lock time is measured from the time $V_{DD}$ and $V_{DDPLL}$ are valid to $\overline{RSTOUT}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
10 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57 \times 10^{-6} \times 2(MFD + 2)$
11 PLL is operating in 1:1 PLL mode.
12 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DDPLL}$ and $V_{SSPLL}$ and variation in crystal oscillator frequency increase the jitter percentage for a given interval.
13 Based on slow system clock of 33MHz maximum frequency.
14 Modulation percentage applies over an interval of 10μs, or equivalently the modulation rate is 100KHz.
15 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
16 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

## 8.6 External Interface Timing Characteristics

Table 12 lists processor bus input timings.

**NOTE**

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

**Table 12. Processor Bus Input Timing Specifications**

| Name | Characteristic[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| B0 | CLKOUT | $t_{CYC}$ | 12 | — | ns |
| **Control Inputs** | | | | | |
| B1a | Control input valid to CLKOUT high[2] | $t_{CVCH}$ | 9 | — | ns |
| B1b | $\overline{BKPT}$ valid to CLKOUT high[3] | $t_{BKVCH}$ | 9 | — | ns |
| B2a | CLKOUT high to control inputs invalid[2] | $t_{CHCII}$ | 0 | — | ns |
| B2b | CLKOUT high to asynchronous control input $\overline{BKPT}$ invalid[3] | $t_{BKNCH}$ | 0 | — | ns |
| **Data Inputs** | | | | | |
| B4 | Data input (D[31:16]) valid to CLKOUT high | $t_{DIVCH}$ | 4 | — | ns |
| B5 | CLKOUT high to data input (D[31:16]) invalid | $t_{CHDII}$ | 0 | — | ns |

1 Timing specifications have been indicated taking into account the full drive strength for the pads.
2 $\overline{TEA}$ and $\overline{TA}$ pins are being referred to as control inputs.
3 Refer to figure A-19.

Timings listed in Table 12 are shown in Figure 7.

* The timings are also valid for inputs sampled on the negative clock edge.

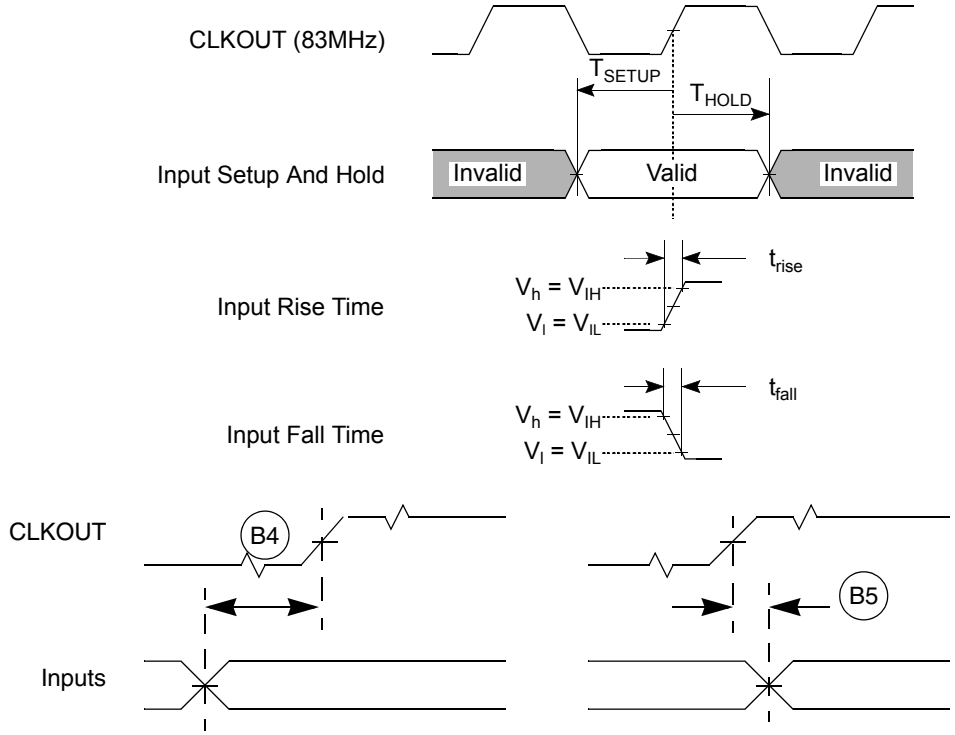



**Figure 7. General Input Timing Requirements**

## 8.7 Processor Bus Output Timing Specifications

Table 13 lists processor bus output timings.

**Table 13. External Bus Output Timing Specifications**

| Name | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **Control Outputs** | | | | | |
| B6a | CLKOUT high to chip selects ($\overline{CS}$[7:0]) valid [1] | $t_{CHCV}$ | — | $0.5t_{CYC}$ + 5.5 | ns |
| B6b | CLKOUT high to byte enables ($\overline{BS}$[3:2]) valid[2] | $t_{CHBV}$ | — | $0.5t_{CYC}$ + 5.5 | ns |
| B6c | CLKOUT high to output enable ($\overline{OE}$) valid[3] | $t_{CHOV}$ | — | $0.5t_{CYC}$ + 5.5 | ns |
| B7 | CLKOUT high to control output ($\overline{BS}$[3:2], $\overline{OE}$) invalid | $t_{CHCOI}$ | $0.5t_{CYC}$ + 1.0 | — | ns |
| B7a | CLKOUT high to chip selects invalid | $t_{CHCI}$ | $0.5t_{CYC}$ + 1.0 | — | ns |
| **Address and Attribute Outputs** | | | | | |
| B8 | CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, TSIZ[1:0], $\overline{TIP}$, R/$\overline{W}$) valid | $t_{CHAV}$ | — | 9 | ns |
| B9 | CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, TSIZ[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid | $t_{CHAI}$ | 1.0 | — | ns |
| **Data Outputs** | | | | | |
| B11 | CLKOUT high to data output (D[31:16]) valid | $t_{CHDOV}$ | — | 9 | ns |
| B12 | CLKOUT high to data output (D[31:16]) invalid | $t_{CHDOI}$ | 1.0 | — | ns |
| B13 | CLKOUT high to data output (D[31:16]) high impedance | $t_{CHDOZ}$ | — | 9 | ns |

1 $\overline{CS}$ transitions after the falling edge of CLKOUT.
2 $\overline{BS}$ transitions after the falling edge of CLKOUT.
3 $\overline{OE}$ transitions after the falling edge of CLKOUT.

Read/write bus timings listed in Table 13 are shown in Figure 8, Figure 9, and Figure 10.

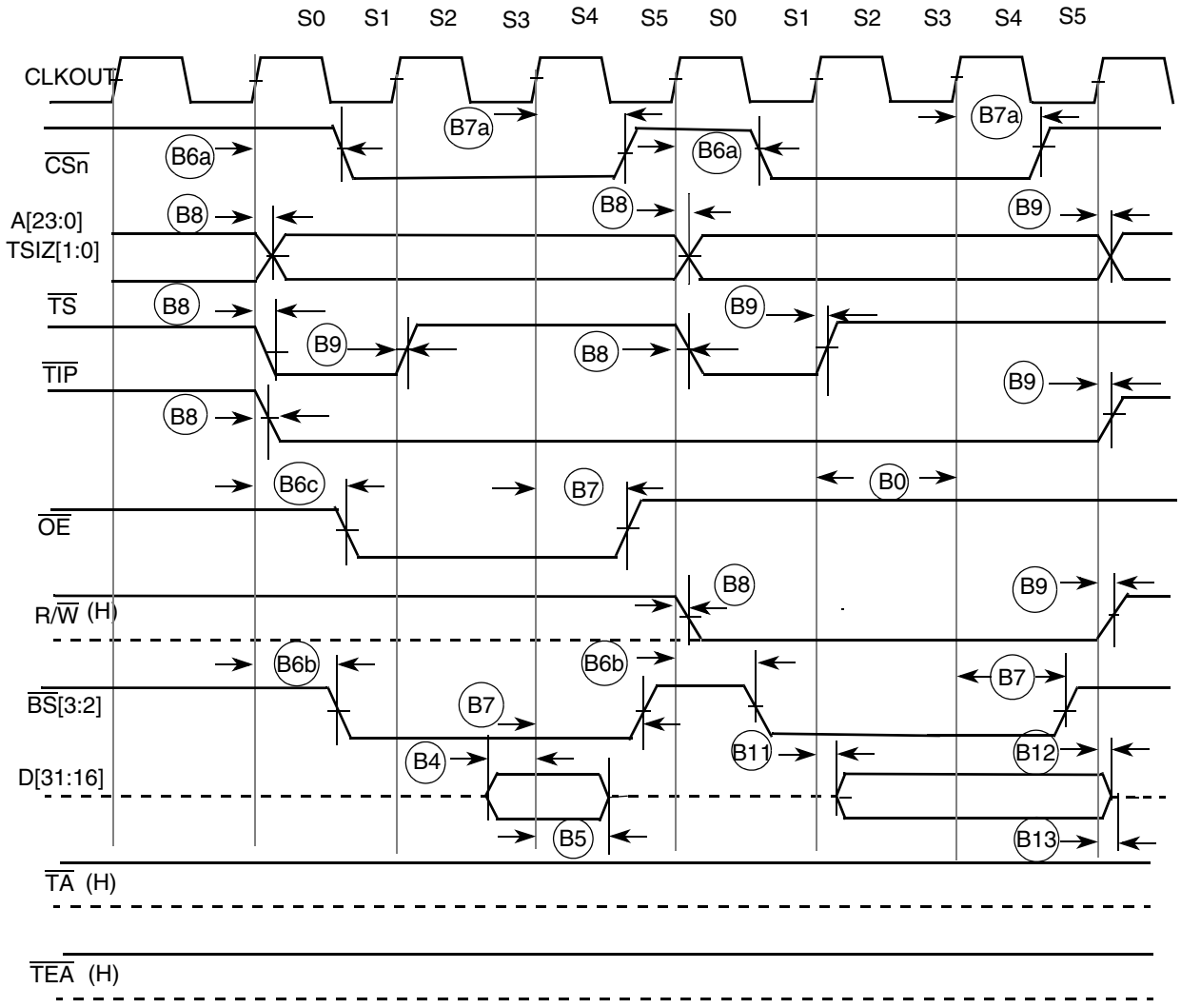



**Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing**

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 13.

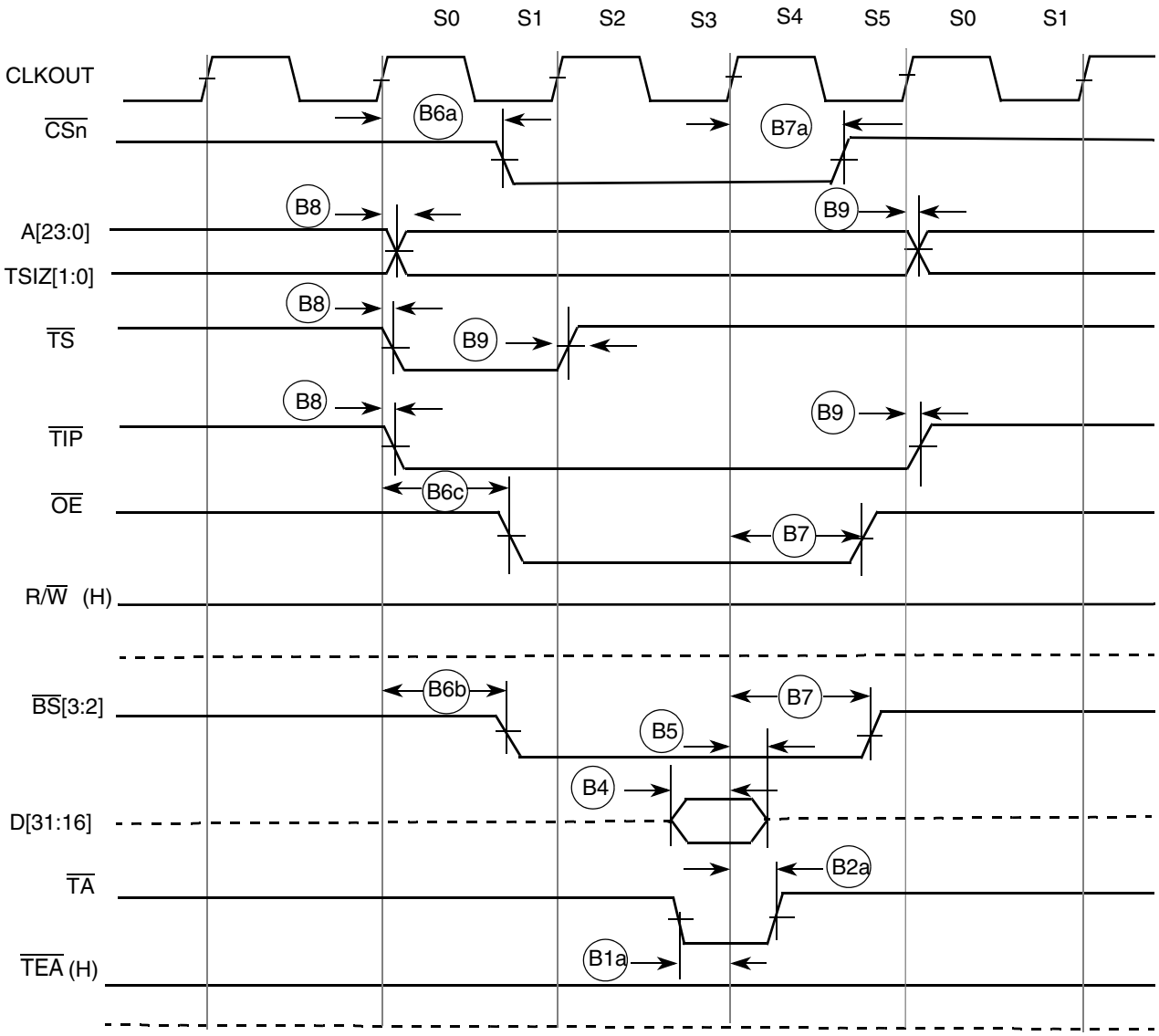



**Figure 9. SRAM Read Bus Cycle Terminated by TA**

Figure 10 shows an SRAM bus cycle terminated by TEA showing timings listed in Table 13.

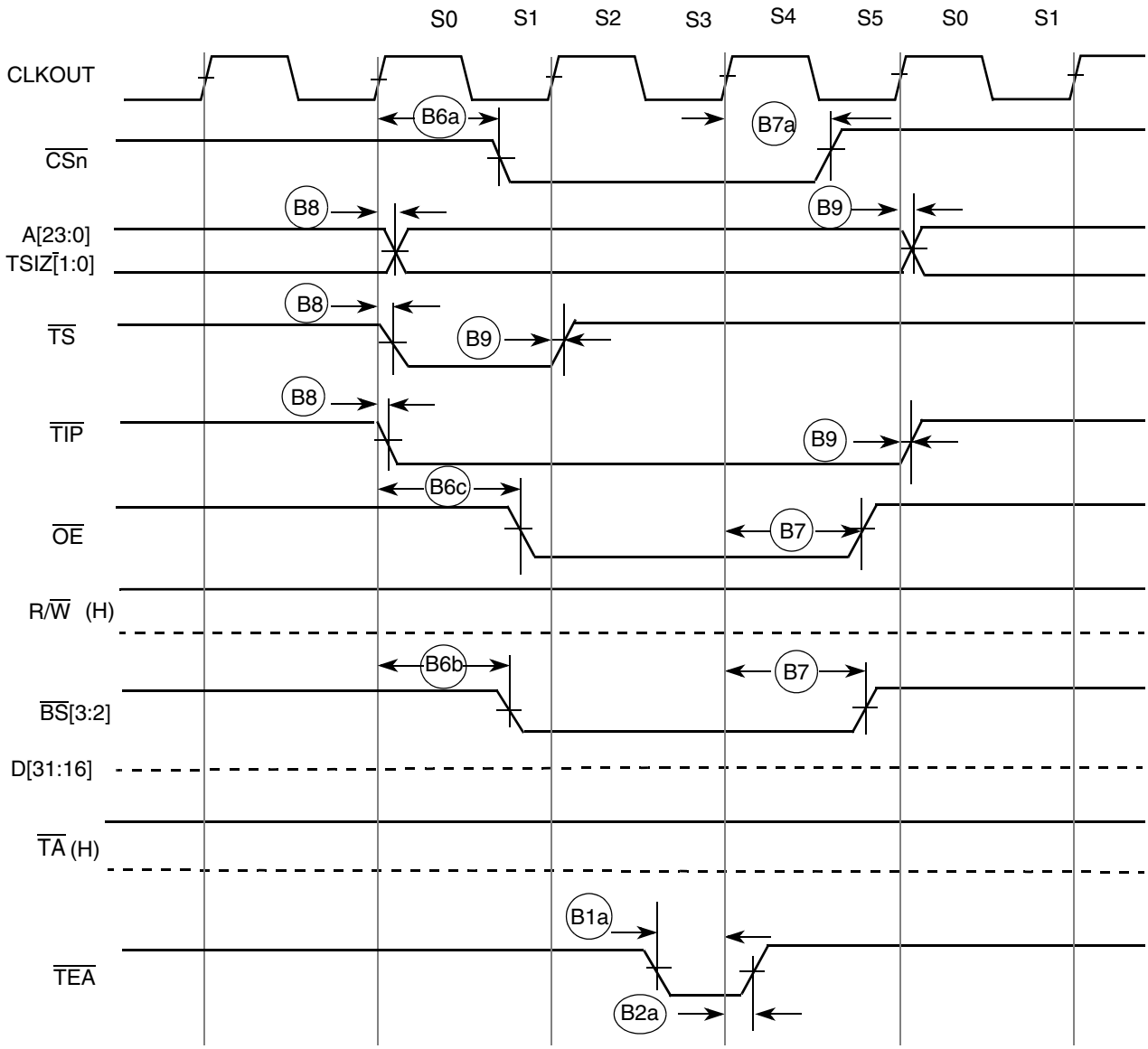



**Figure 10. SRAM Read Bus Cycle Terminated by TEA**

## 8.8 DDR SDRAM AC Timing Characteristics

The DDR SDRAM controller uses SSTL2 and I/O drivers. Either Class I or Class II drive strength is available and is user programmable. DDR Clock timing specifications are given in Table 14 and Figure 11.

**Table 14. DDR Clock Timing Specifications[1]**

| Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| $V_{MP}$ | Clock output mid-point voltage | 1.05 | 1.45 | V |
| $V_{OUT}$ | Clock output voltage level | -0.3 | $SDV_{DD}$ + 0.3 | V |
| $V_{ID}$ | Clock output differential voltage (peak to peak swing) | 0.7 | $SDV_{DD}$ + 0.6 | V |
| $V_{IX}$ | Clock crossing point voltage | 1.05 | 1.45 | V |

1 SD $V_{DD}$ is nominally 2.5V.

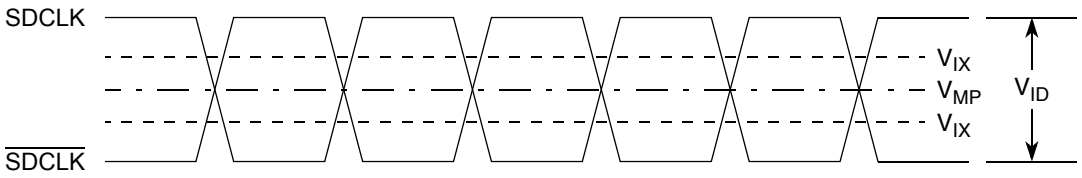



**Figure 11. DDR Clock Timing Diagram**

When using the DDR SDRAM controller the timing numbers in Table 15 must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

**Table 15. DDR Timing**

| NUM | Characteristic[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| | Frequency of operation[2] | | TBD | 83 | MHz |
| DD1 | Clock Period (DDR_CLKOUT) | $t_{CK}$ | 12 | TBD | ns |
| DD2 | Pulse Width High[3] | $t_{CKH}$ | 0.45 | 0.55 | $t_{CK}$ |
| DD3 | Pulse Width Low[3] | $t_{CKI}$ | 0.45 | 0.55 | $t_{CK}$ |
| DD4 | DDR_CLKOUT high to DDR address, SD_CKE, SD_CS[1:0], SD_SCAS, SD_SRAS, SD_WE valid | $t_{CMV}$ | — | 0.5 x $t_{CK}$ + 1 | ns |
| DD5 | DDR_CLKOUT high to DDR address, SD_CKE, $\overline{\text{SD\_CS}}$, $\overline{\text{SD\_SCAS}}$, $\overline{\text{SD\_SRAS}}$, $\overline{\text{SD\_WE}}$ invalid | $t_{CMH}$ | 2 | — | ns |
| DD6 | Write command to first $\overline{\text{SD\_DQS}}$ Latching Transition | $t_{DQSS}$ | — | 1.25 | $t_{CK}$ |
| DD7 | $\overline{\text{SD\_DQS}}$ high to Data and DM valid (write) - setup[4,5] | $t_{QS}$ | 1.5 | — | ns |
| DD8 | $\overline{\text{SD\_DQS}}$ high to Data and DM invalid (write) - hold[4] | $t_{QH}$ | 1 | — | ns |
| DD9 | $\overline{\text{SD\_DQS}}$ high to Data valid (read) - setup[6] | $t_{IS}$ | — | 1 | ns |
| DD10 | $\overline{\text{SD\_DQS}}$ high to Data invalid (read) - hold[7] | $t_{IH}$ | 0.25 x $t_{CK}$ + 1 | — | ns |
| DD11 | $\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - setup | $t_{DSS}$ | 0.5 | — | ns |
| DD12 | $\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - hold | $t_{DSH}$ | 0.5 | — | ns |
| DD13 | DQS input read preamble width ($t_{RPRE}$) | $t_{RPRE}$ | 0.9 | 1.1 | $t_{CK}$ |
| DD14 | DQS input read postamble width ($t_{RPST}$) | $t_{RPST}$ | 0.4 | 0.6 | $t_{CK}$ |
| DD15 | DQS output write preamble width ($t_{WPRE}$) | $t_{WPRE}$ | 0.25 | — | $t_{CK}$ |
| DD16 | DQS output write postamble width ($t_{WPST}$) | $t_{WPST}$ | 0.4 | 0.6 | $t_{CK}$ |

1 All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2 DDR_CLKOUT operates at half the frequency of the PLLMRFM output and the ColdFire core.
3 $t_{CKH}$ + $t_{CKL}$ must be less than or equal to $t_{CK}$.
4 D[31:24] is relative to $\overline{\text{SD\_DQS3}}$ and D[23:16] is relative to $\overline{\text{SD\_DQS2}}$.
5 The first data beat will be valid before the first rising edge of $\overline{\text{SD\_DQS}}$ and after the $\overline{\text{SD\_DQS}}$ write preamble. The remaining data beats will be valid for each subsequent $\overline{\text{SD\_DQS}}$ edge
6 Data input skew is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).
7 Data input hold is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the first data line becomes invalid.

Figure 13 shows a DDR SDRAM write cycle.

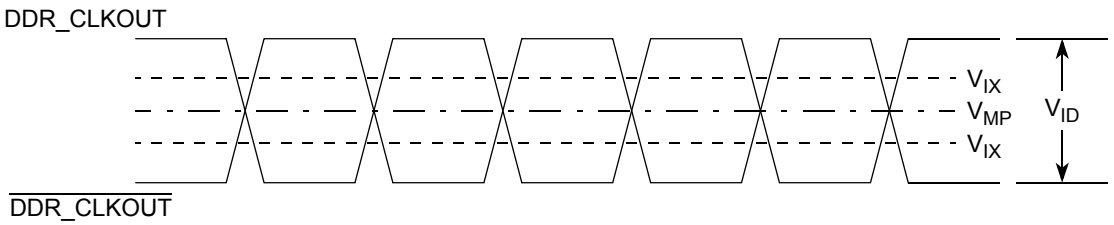



**Figure 12. DDR_CLKOUT and DDR_CLKOUT Crossover Timing**

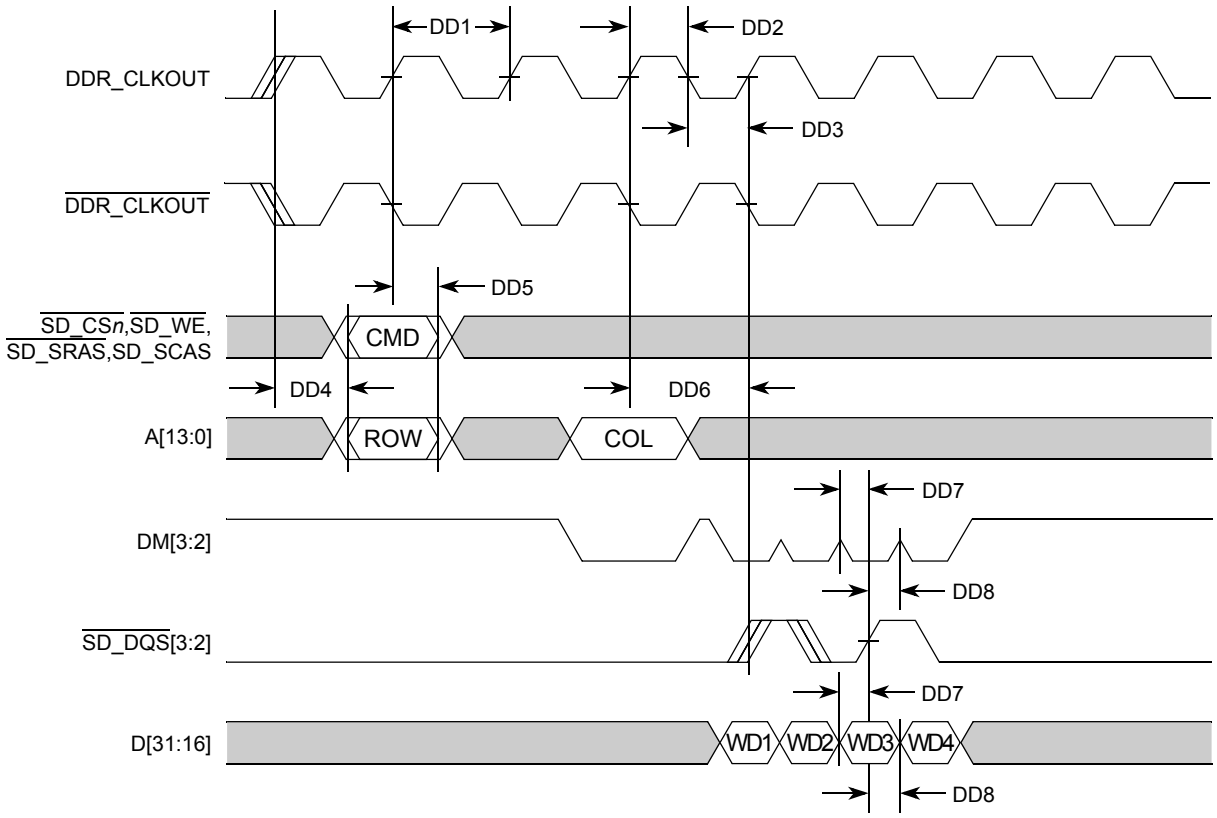



**Figure 13. DDR Write Timing**

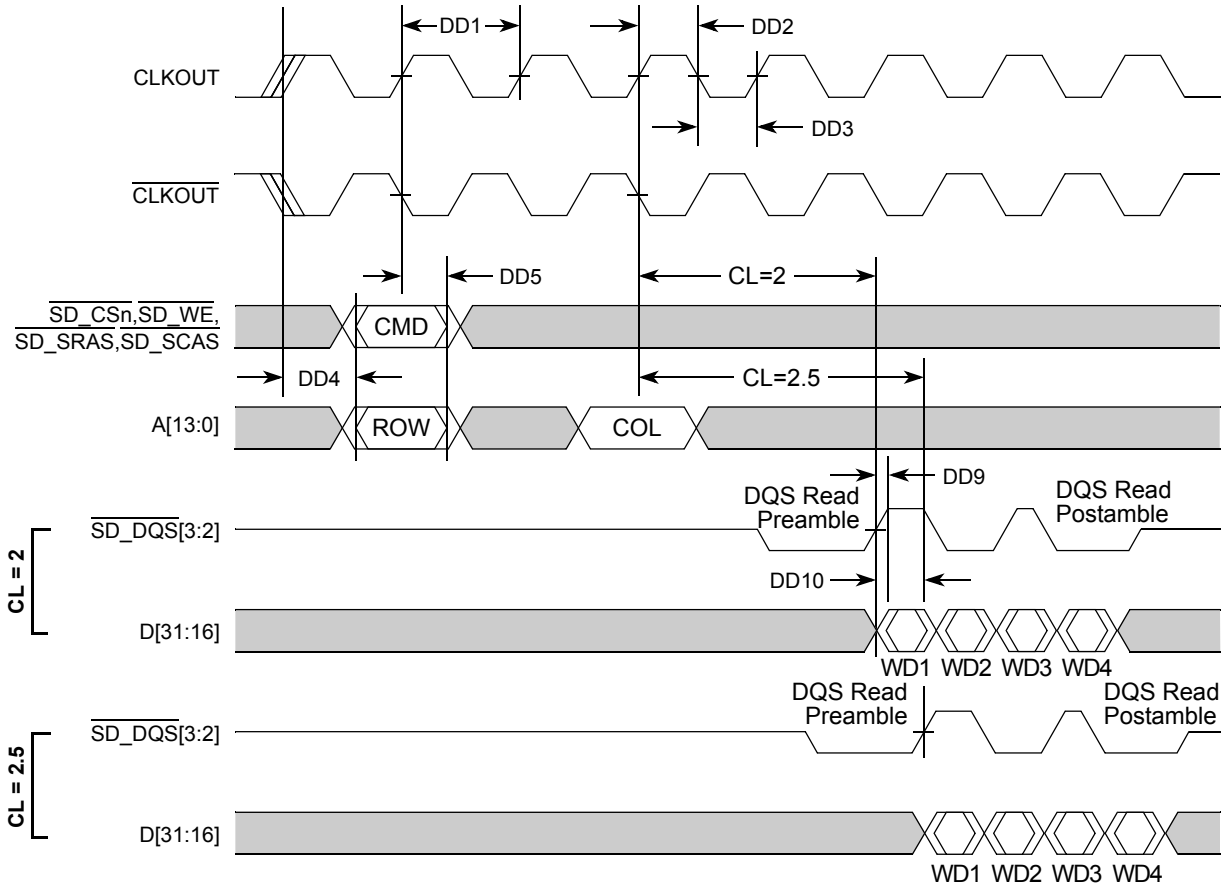



**Figure 14. DDR Read Timing**

## 8.9 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, TIMERS, UARTS, FEC0, FEC1, Interrupts and USB interfaces. When in GPIO mode the timing specification for these pins is given in Table 16 and Figure 15.

**Table 16. GPIO Timing**

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| G1 | CLKOUT High to GPIO Output Valid | $t_{CHPOV}$ | — | 10 | ns |
| G2 | CLKOUT High to GPIO Output Invalid | $t_{CHPOI}$ | 1.0 | — | ns |
| G3 | GPIO Input Valid to CLKOUT High | $t_{PVCH}$ | 9 | — | ns |
| G4 | CLKOUT High to GPIO Input Invalid | $t_{CHPI}$ | 1.5 | — | ns |

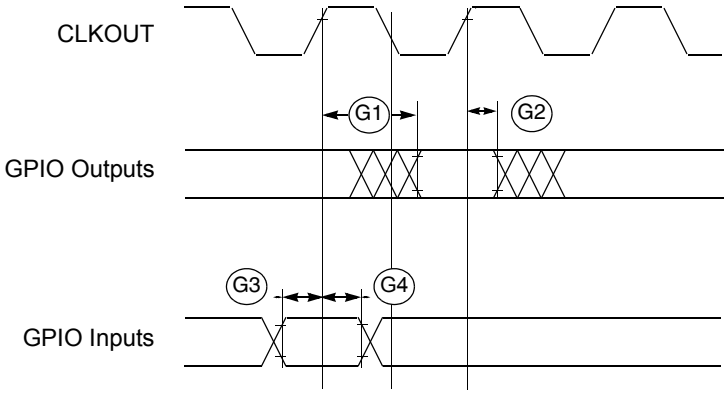


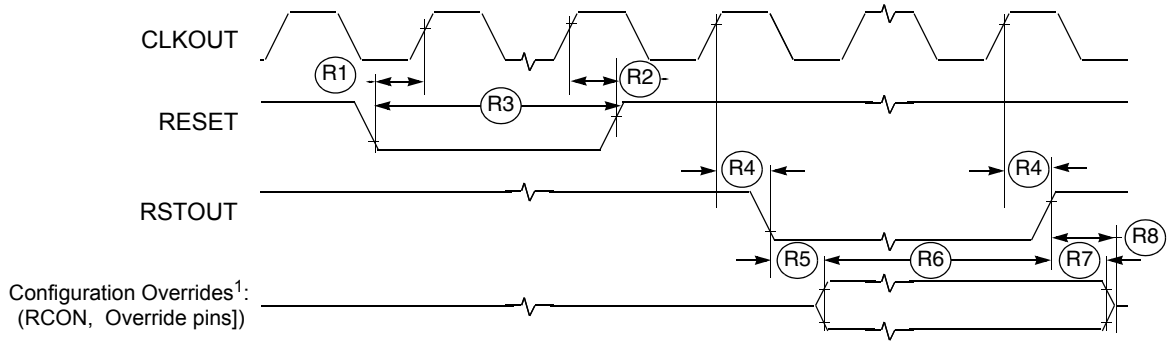

**Figure 15. GPIO Timing**

## 8.10 Reset and Configuration Override Timing

**Table 17. Reset and Configuration Override Timing**
**($V_{DD}$ = 2.7 to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = $T_L$ to $T_H$)[1]**

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| R1 | $\overline{\text{RESET}}$ Input valid to CLKOUT High | $t_{RVCH}$ | 9 | — | ns |
| R2 | CLKOUT High to $\overline{\text{RESET}}$ Input invalid | $t_{CHRI}$ | 1.5 | — | ns |
| R3 | $\overline{\text{RESET}}$ Input valid Time [2] | $t_{RIVT}$ | 5 | — | $t_{CYC}$ |
| R4 | CLKOUT High to $\overline{\text{RSTOUT}}$ Valid | $t_{CHROV}$ | — | 10 | ns |
| R5 | $\overline{\text{RSTOUT}}$ valid to Config. Overrides valid | $t_{ROVCV}$ | 0 | — | ns |
| R6 | Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid | $t_{COS}$ | 20 | — | $t_{CYC}$ |
| R7 | Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid | $t_{COH}$ | 0 | — | ns |
| R8 | $\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance | $t_{ROICZ}$ | — | 1 x $t_{CYC}$ | ns |

1 All AC timing is shown with respect to 50% $OV_{DD}$ levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.




1. Refer to the Coldfire Integration Module (CIM) section for more information.

RESET and Configuration Override Timing

## 8.11 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

### 8.11.1 MII Receive Signal Timing (FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER, and FEC*n*_RXCLK)

The receiver functions correctly up to a FEC*n*_RXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_RXCLK frequency.

Table 18 lists MII receive channel timings.

**Table 18. MII Receive Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M1 | FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER to FEC*n*_RXCLK setup | 5 | — | ns |
| M2 | FEC*n*_RXCLK to FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER hold | 5 | — | ns |
| M3 | FEC*n*_RXCLK pulse width high | 35% | 65% | FEC*n*_RXCLK period |
| M4 | FEC*n*_RXCLK pulse width low | 35% | 65% | FEC*n*_RXCLK period |

Figure 16 shows MII receive signal timings listed in Table 18.

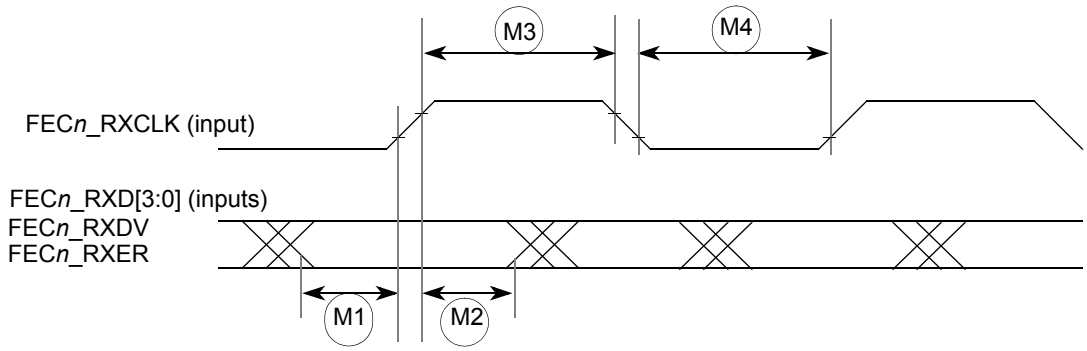



**Figure 16. MII Receive Signal Timing Diagram**

### 8.11.2 MII Transmit Signal Timing (FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER, FEC*n*_TXCLK)

Table 19 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC*n*_TXCLK maximum frequency of 25 MHz +1%. The processor clock frequency must exceed twice the FEC*n*_TXCLK frequency.

**Table 19. MII Transmit Channel Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M5 | FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER invalid | 5 | — | ns |
| M6 | FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER valid | — | 25 | ns |
| M7 | FEC*n*_TXCLK pulse width high | 35% | 65% | FEC*n*_TXCLK period |
| M8 | FEC*n*_TXCLK pulse width low | 35% | 65% | FEC*n*_TXCLK period |

Figure 17 shows MII transmit signal timings listed in Table 19.

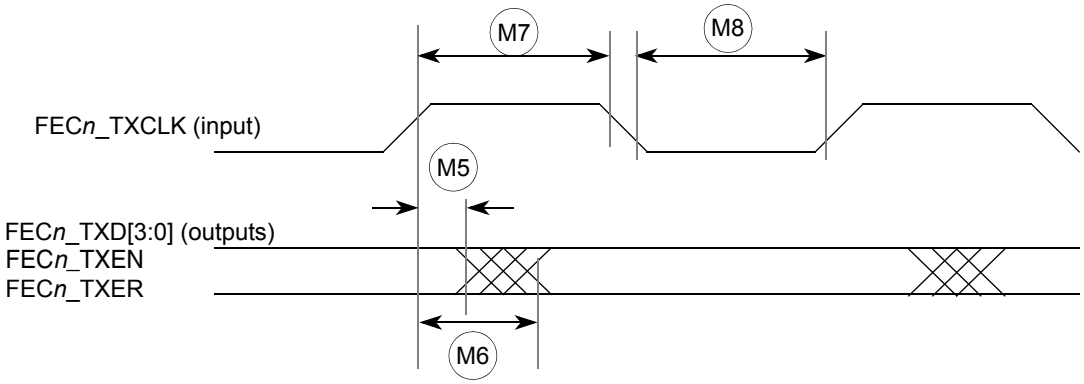



**Figure 17. MII Transmit Signal Timing Diagram**

## 8.11.3 MII Async Inputs Signal Timing (FEC*n*_CRS and FEC*n*_COL)

Table 20 lists MII asynchronous inputs signal timing.

**Table 20. MII Asynchronous Input Signal Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M9 | FEC*n*_CRS, FEC*n*_COL minimum pulse width | 1.5 | — | FEC*n*_TXCLK period |

Figure 18 shows MII asynchronous input timings listed in Table 20.


**Figure 18. MII Async Inputs Timing Diagram**

## 8.11.4 MII Serial Management Channel Timing (FEC*n*_MDIO and FEC*n*_MDC)

Table 21 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

**Table 21. MII Serial Management Channel Timing**

| Num | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| M10 | FEC*n*_MDC falling edge to FEC*n*_MDIO output invalid (minimum propagation delay) | 0 | — | ns |
| M11 | FEC*n*_MDC falling edge to FEC*n*_MDIO output valid (max prop delay) | — | 25 | ns |
| M12 | FEC*n*_MDIO (input) to FEC*n*_MDC rising edge setup | 10 | — | ns |
| M13 | FEC*n*_MDIO (input) to FEC*n*_MDC rising edge hold | 0 | — | ns |
| M14 | FEC*n*_MDC pulse width high | 40% | 60% | MDC period |
| M15 | FEC*n*_MDC pulse width low | 40% | 60% | MDC period |

Figure 19 shows MII serial management channel timings listed in Table 21.

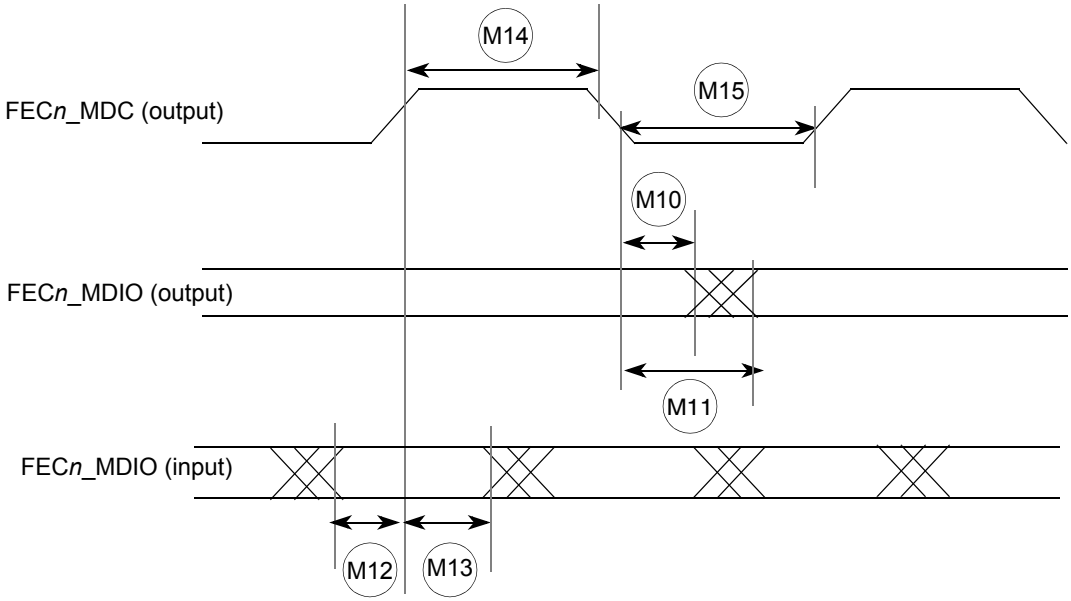



**Figure 19. MII Serial Management Channel Timing Diagram**

## 8.11.5 USB Interface AC Timing Specifications

Table 22 lists USB Interface timings.

**Table 22. USB Interface Timing**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| US1 | USB_CLK frequency of operation | 48 | 48 | MHz |
| US2 | USB_CLK fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 2 | ns |
| US3 | USB_CLK rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | 2 | ns |
| US4 | USB_CLK duty cycle (at 0.5 x O $V_{DD}$) | 45 | 55 | % |
| Data Inputs | | | | |
| US5 | USB_RP, USB_RN, USB_RXD valid to USB_CLK high | 6 | — | ns |

**Table 22. USB Interface Timing (continued)**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| US6 | USB_CLK high to USB_RP, USB_RN, USB_RXD invalid | 6 | — | ns |
| | Data Outputs | | | |
| US7 | USB_CLK high to USB_TP, USB_TN, USB_SUSP valid | — | 12 | ns |
| US8 | USB_CLK high to USB_TP, USB_TN, USB_SUSP invalid | 3 | — | ns |

Figure 20 shows USB interface timings listed in Table 22.

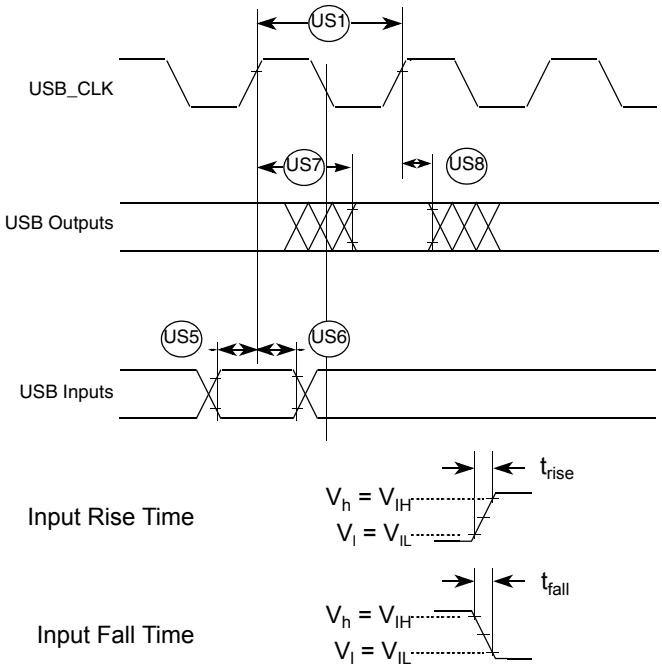



**Figure 20. USB Signals Timing Diagram**

## 8.12 I²C Input/Output Timing Specifications

Table 23 lists specifications for the I²C input timing parameters shown in Figure 21.

**Table 23. I²C Input Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1 | Start condition hold time | 2 x $t_{CYC}$ | — | ns |
| I2 | Clock low period | 8 x $t_{CYC}$ | — | ns |
| I3 | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | 1 | ms |
| I4 | Data hold time | 0 | — | ns |
| I5 | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 1 | ms |
| I6 | Clock high time | 4 x $t_{CYC}$ | — | ns |
| I7 | Data setup time | 0 | — | ns |

**Table 23. I²C Input Timing Specifications between I2C_SCL and I2C_SDA (continued)**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I8 | Start condition setup time (for repeated start condition only) | 2 x $t_{CYC}$ | — | ns |
| I9 | Stop condition setup time | 2 x $t_{CYC}$ | — | ns |

Table 24 lists specifications for the I²C output timing parameters shown in Figure 21.

**Table 24. I²C Output Timing Specifications between I2C_SCL and I2C_SDA**

| Num | Characteristic | Min | Max | Units |
|---|---|---|---|---|
| I1[1] | Start condition hold time | 6 x $t_{CYC}$ | — | ns |
| I2 [1] | Clock low period | 10 x $t_{CYC}$ | — | ns |
| I3 [2] | I2C_SCL/I2C_SDA rise time ($V_{IL}$ = 0.5 V to $V_{IH}$ = 2.4 V) | — | — | µs |
| I4 [1] | Data hold time | 7 x $t_{CYC}$ | — | ns |
| I5 [3] | I2C_SCL/I2C_SDA fall time ($V_{IH}$ = 2.4 V to $V_{IL}$ = 0.5 V) | — | 3 | ns |
| I6 [1] | Clock high time | 10 x $t_{CYC}$ | — | ns |
| I7 [1] | Data setup time | 2 x $t_{CYC}$ | — | ns |
| I8 [1] | Start condition setup time (for repeated start condition only) | 20 x $t_{CYC}$ | — | ns |
| I9 [1] | Stop condition setup time | 10 x $t_{CYC}$ | — | ns |

1 Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 24. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 24 are minimum values.

2 Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

3 Specified at a nominal 50-pF load.

Figure 21 shows timing for the values in Table 23 and Table 24.

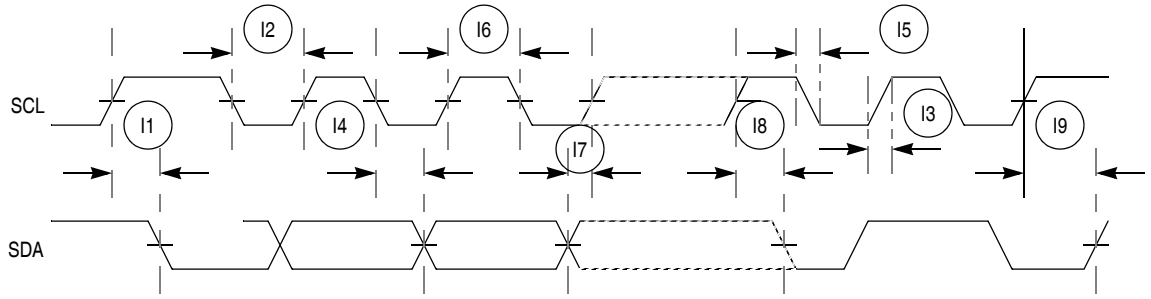



**Figure 21. I²C Input/Output Timings**

## 8.13 DMA Timers Timing Specifications

**Table 25. Timer Module AC Timing Specifications**

| Name | Characteristic [1] | Min | Max | Unit |
|---|---|---|---|---|
| T1 | T0IN / T1IN / T2IN / T3IN cycle time | 3 x $t_{CYC}$ | — | ns |
| T2 | T0IN / T1IN / T2IN / T3IN pulse width | 1 x $t_{CYC}$ | — | ns |

[1] All timing references to CLKOUT are given to its rising edge.

## 8.14 QSPI Electrical Specifications

**Table 26. QSPI Modules AC Timing Specifications**

| Name | Characteristic | Min | Max | Unit |
|---|---|---|---|---|
| QS1 | QSPI_CS[3:0] to QSPI_CLK | 1 | 510 | $t_{CYC}$ |
| QS2 | QSPI_CLK high to QSPI_DOUT valid. | — | 10 | ns |
| QS3 | QSPI_CLK high to QSPI_DOUT invalid (Output hold) | 2 | — | ns |
| QS4 | QSPI_DIN to QSPI_CLK (Input setup) | 9 | — | ns |
| QS5 | QSPI_DIN to QSPI_CLK (Input hold) | 9 | — | ns |

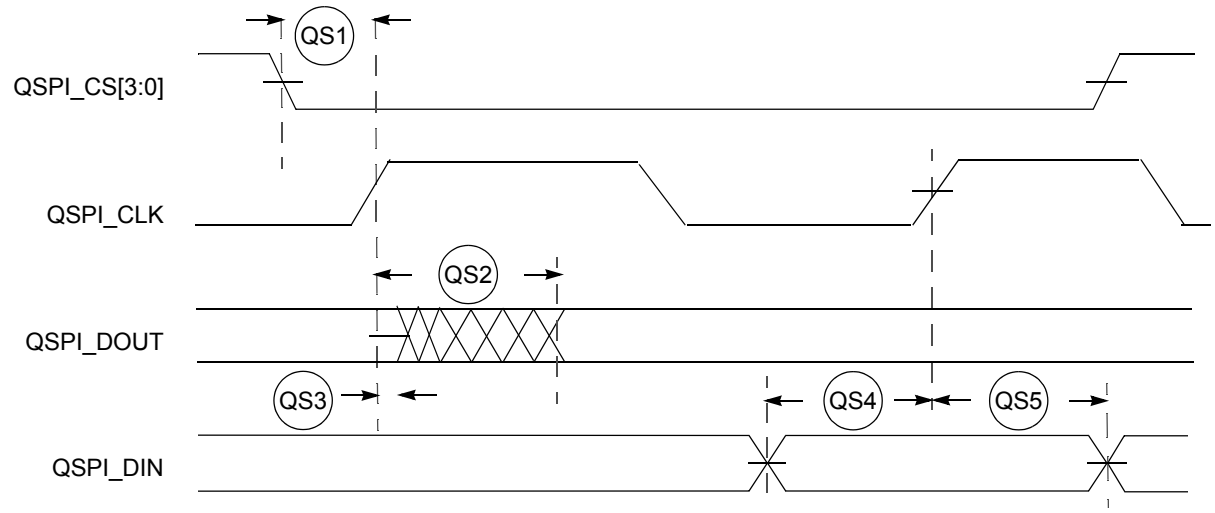



**Figure 22. QSPI Timing**

## 8.15 JTAG and Boundary Scan Timing

**Table 27. JTAG and Boundary Scan Timing**

| Num | Characteristics[1] | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| J1 | TCLK Frequency of Operation | $f_{JCYC}$ | DC | 1/4 | $f_{sys/2}$ |
| J2 | TCLK Cycle Period | $t_{JCYC}$ | 4 x $t_{CYC}$ | — | ns |
| J3 | TCLK Clock Pulse Width | $t_{JCW}$ | 26 | — | ns |
| J4 | TCLK Rise and Fall Times | $t_{JCRF}$ | 0 | 3 | ns |
| J5 | Boundary Scan Input Data Setup Time to TCLK Rise | $t_{BSDST}$ | 4 | — | ns |
| J6 | Boundary Scan Input Data Hold Time after TCLK Rise | $t_{BSDHT}$ | 26 | — | ns |
| J7 | TCLK Low to Boundary Scan Output Data Valid | $t_{BSDV}$ | 0 | 33 | ns |
| J8 | TCLK Low to Boundary Scan Output High Z | $t_{BSDZ}$ | 0 | 33 | ns |
| J9 | TMS, TDI Input Data Setup Time to TCLK Rise | $t_{TAPBST}$ | 4 | — | ns |
| J10 | TMS, TDI Input Data Hold Time after TCLK Rise | $t_{TAPBHT}$ | 10 | — | ns |
| J11 | TCLK Low to TDO Data Valid | $t_{TDODV}$ | 0 | 26 | ns |
| J12 | TCLK Low to TDO High Z | $t_{TDODZ}$ | 0 | 8 | ns |
| J13 | $\overline{\text{TRST}}$ Assert Time | $t_{TRSTAT}$ | 100 | — | ns |
| J14 | $\overline{\text{TRST}}$ Setup Time (Negation) to TCLK High | $t_{TRSTST}$ | 10 | — | ns |

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

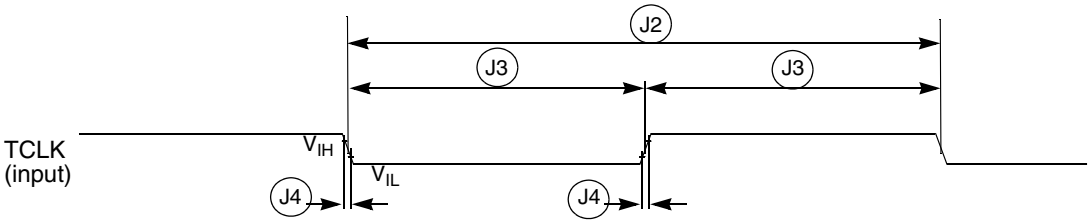



**Figure 23. Test Clock Input Timing**

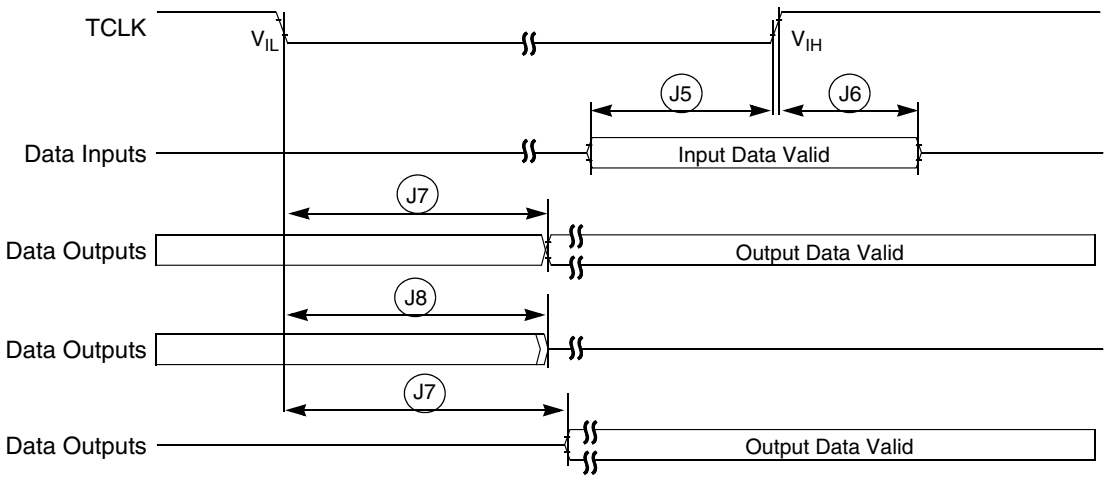



**Figure 24. Boundary Scan (JTAG) Timing**

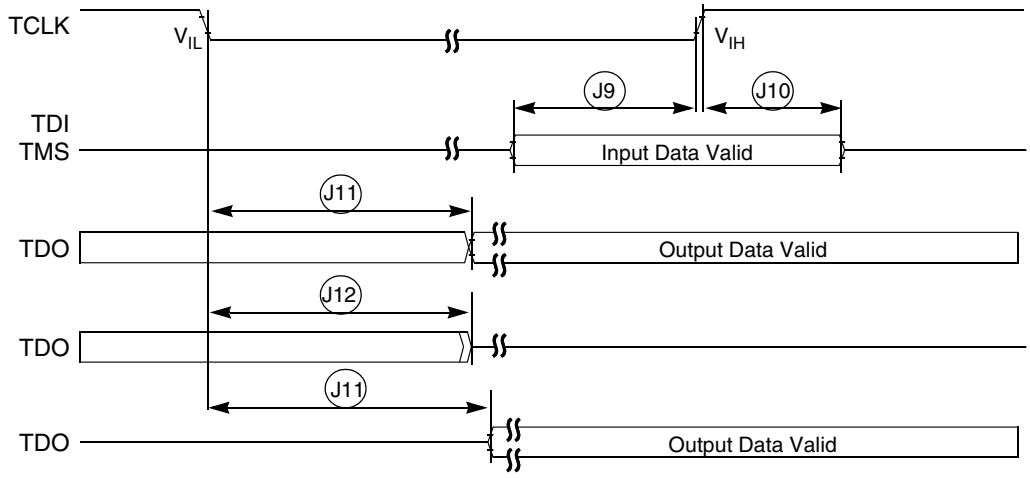



**Figure 25. Test Access Port Timing**

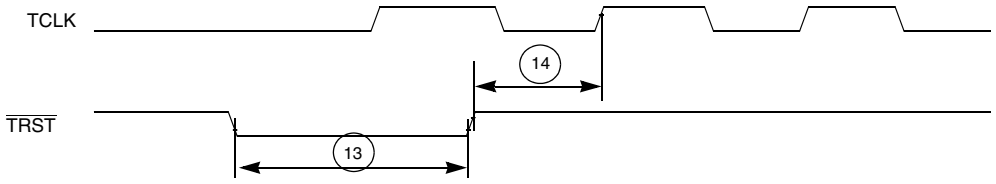



**Figure 26. TRST Timing**

## 8.16 Debug AC Timing Specifications

Table 28 lists specifications for the debug AC timing parameters shown in Figure 28.

**Table 28. Debug AC Timing Specification**

| Num | Characteristic | 166 MHz | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| D0 | PSTCLK cycle time | — | 0.5 | $t_{CYC}$ |
| D1 | PST, DDATA to PSTCLK setup | 4 | — | ns |
| D2 | CLKOUT to PST, DDATA hold | 1.0 | — | ns |
| D3 | DSI-to-DSCLK setup | 1 x $t_{CYC}$ | — | ns |
| D4 [1] | DSCLK-to-DSO hold | 4 x $t_{CYC}$ | — | ns |
| D5 | DSCLK cycle time | 5 x $t_{CYC}$ | — | ns |
| D6 | $\overline{BKPT}$ input data setup time to PSTCLK Rise | 4 | — | ns |
| D7 | $\overline{BKPT}$ input data hold time to PSTCLK Rise | 1.5 | — | ns |
| D8 | PSTCLK high to $\overline{BKPT}$ high Z | 0.0 | 10.0 | ns |

[1] DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of PSTCLK.

Figure 27 shows real-time trace timing for the values in Table 28.

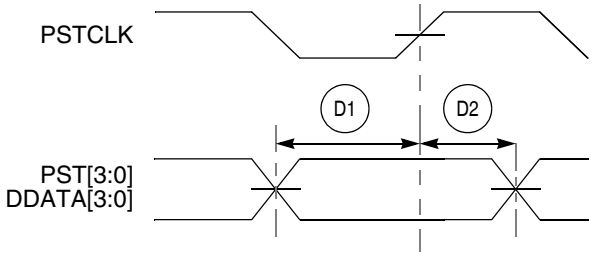



**Figure 27. Real-Time Trace AC Timing**

Figure 28 shows BDM serial port AC timing for the values in Table 28.

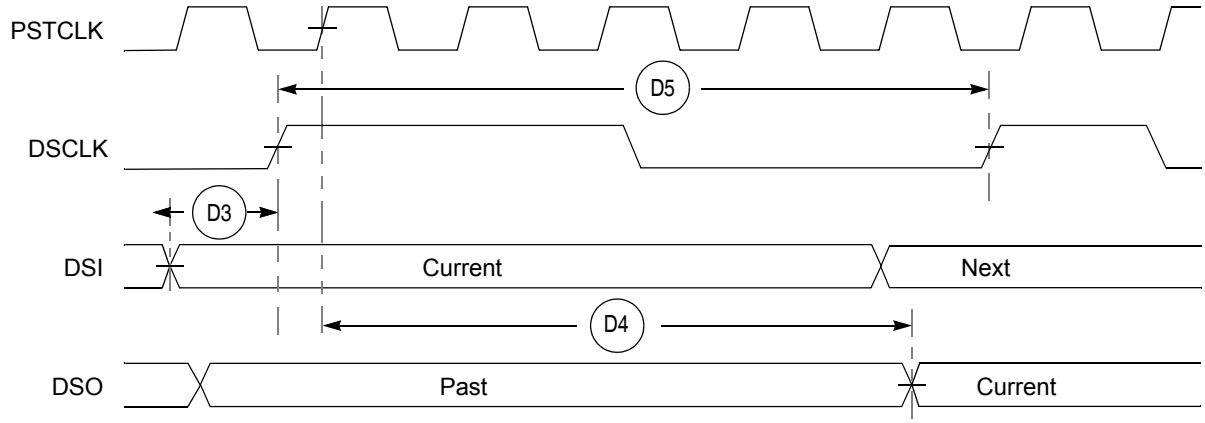



**Figure 28. BDM Serial Port AC Timing**

# 9 Documentation

Documentation regarding the MCF5275 and their development support tools is available from a local Freescale distributor, a Freescale semiconductor sales office, the Freescale Literature Distribution Center, or through the Freescale web address at http://www.freescale.com/coldfire.

# 10 Revision History

Table 29 provides a revision history for this hardware specification.

**Table 29. Document Revision History**

| Rev. No. | Substantive Change(s) |
|---|---|
| 0 | • Initial release. |
| 1 | • Added Figure 6. |
| 1.1 | • Removed duplicate information in the module description sections. The information is all in the Signals Description Table. |
| 1.2 | • Removed Overview, Features, Signal Descriptions, Modes of Operation, and Address Multiplexing sections. This information can be found in the MCF5275 Reference Manual.<br>• Removed list of documentation in Section 9, "Documentation.". An up-to-date list is always available on our web site.<br>• Changed CLKOUT -> PSTCLK in Section 8.16, "Debug AC Timing Specifications."<br>• Table 10: Update $V_{DD}$ spec from 1.35-1.65 to 1.4-1.6.<br>• Table 13: Timings B6a, B6b, B6c, B7, B7a, B9, B12 updated:<br>B6a, B6b, B6c maximum changed from "$0.5t_{CYC}$ + 5" to "$0.5t_{CYC}$ + 5.5"<br>B7, B7a minimum changed from "$0.5t_{CYC}$ + 1.5" to "$0.5t_{CYC}$ + 1.0"<br>B9, B11 minimum changed from "1.5" to "1.0" |
| 1.3 | • Added Section 5.2.1, "Supply Voltage Sequencing and Separation Cautions."<br>• Added thermal characteristics for 196 MAPBGA in Table 8.<br>• Updated package dimensions drawing, Figure 6. |
| 2 | • Removed second sentence from Section 8.11.1, "MII Receive Signal Timing (FECn_RXD[3:0], FECn_RXDV, FECn_RXER, and FECn_RXCLK)," and Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," regarding no minimum frequency requirement for TXCLK.<br>• Removed third and fourth paragraphs from Section 8.11.2, "MII Transmit Signal Timing (FECn_TXD[3:0], FECn_TXEN, FECn_TXER, FECn_TXCLK)," as this feature is not supported on this device. |

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