


Synchronous 400mA Buck-Boost and 200mA Buck Converters

FEATURES

- **Dual High Efficiency DC/DC Converters:**
Buck-Boost (V_{OUT} : 2.2V to 5.25V, I_{OUT} : 400mA for $V_{IN} > 3V$, $V_{OUT} = 3.3V$)
Buck (V_{OUT} : 0.6V to V_{IN} , I_{OUT} : 200mA)
- **2.4V to 5.5V Input Voltage Range**
- **Pin Selectable Burst Mode[®] Operation**
- **25 μ A Total Quiescent Current for Both Converters in Burst Mode Operation**
- Independent Power Good Indicator Outputs
- Integrated Soft-Start
- Thermal and Overcurrent Protection
- <1 μ A Quiescent Current in Shutdown
- Small 0.75mm \times 3mm \times 3mm QFN Package

APPLICATIONS

- Flash-Based MP3 Players
- Medical Instruments
- Digital Cameras
- PDAs, Handheld PCs
- Personal Navigation Devices

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DESCRIPTION

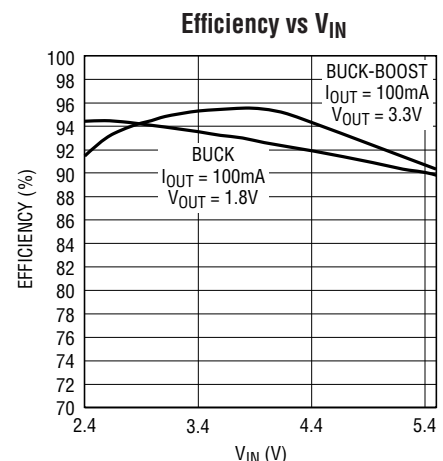
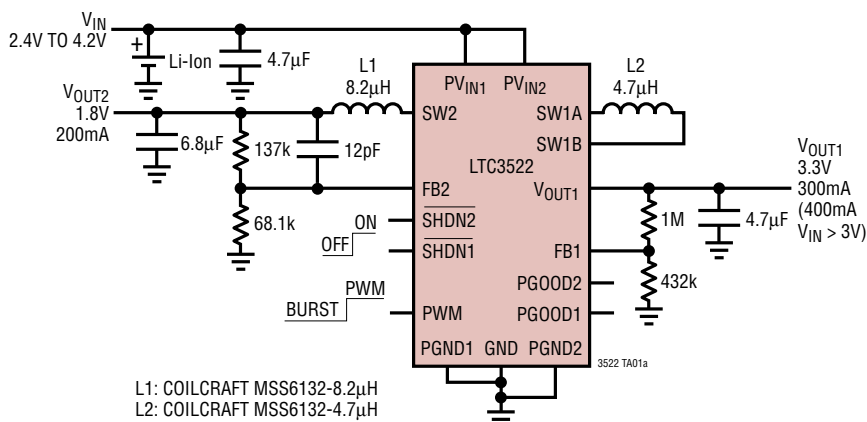
The LTC[®]3522 combines a 400mA buck-boost DC/DC converter with a 200mA synchronous buck DC/DC converter in a tiny 3mm \times 3mm package. The 1MHz switching frequency minimizes the solution footprint while maintaining high efficiency. Both converters feature internal soft-start and compensation, simplifying the design process.

The buck converter is current mode controlled and utilizes an internal synchronous rectifier for high efficiency. The buck converter supports 100% duty cycle operation to extend battery life. If the PWM pin is held low, the buck converter automatically transitions from Burst Mode operation to PWM mode. With the PWM pin held high, the buck converter remains in low noise, 1MHz PWM mode.

The buck-boost converter provides continuous conduction operation to maximize efficiency and minimize noise. At light loads, the buck-boost converter can be placed in Burst Mode operation to improve efficiency and reduce no-load standby current.

The LTC3522 provides a 1 μ A shutdown mode, overtemperature shutdown and current limit protection on both converters. The LTC3522 is available in a 16-pin low profile 3mm \times 3mm QFN package.

TYPICAL APPLICATION



3522 TA01b

3522f

ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV _{IN1} , PV _{IN2} Voltage	-0.3V to 6V
SW1A, SW1B, SW2 Voltage DC	-0.3V to 6V
Pulsed < 100ns	-1V to 7V
Voltage, All Other Pins	-0.3V to 6V
Operating Temperature Range (Note 2) ...	-40°C to 85°C
Maximum Junction Temperature (Note 5)	125°C
Storage Temperature Range	-65°C to 125°C

PACKAGE/ORDER INFORMATION

UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN 17) IS GND AND MUST BE SOLDERED TO PCB GROUND

ORDER PART NUMBER	UD PART MARKING
LTC3522EUD	LCRQ

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. PV_{IN1} = PV_{IN2} = 3.6V, V_{OUT1} = 3.3V unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage		● 2.4		5.5	V
Quiescent Current—Shutdown	V _{SHDN1} = V _{SHDN2} = 0V	●	0.01	1	μA
Burst Mode Quiescent Current	V _{FB1} = 1.1V, V _{FB2} = 0.66V, V _{PWM} = 0V		25		μA
Oscillator Frequency		● 0.8	1.07	1.33	MHz
SHDN1, SHDN2, PWM Input High Voltage		1.4			V
SHDN1, SHDN2, PWM Input Low Voltage				0.4	V
Power Good Outputs Low Voltage	I _{PGOOD1} = I _{PGOOD2} = 1mA		0.02	0.1	V
Power Good Outputs Leakage	V _{PGOOD1} = V _{PGOOD2} = 5.5V		0.1	10	μA
Buck Converter					
PMOS Switch Resistance			0.41		Ω
NMOS Switch Resistance			0.34		Ω
NMOS Switch Leakage	V _{SW2} = 5V, PV _{IN1} = PV _{IN2} = 5V		0.1	5	μA
PMOS Switch Leakage	V _{SW2} = 0V, PV _{IN1} = PV _{IN2} = 5V		0.1	10	μA
Feedback Voltage	(Note 4)	● 0.582	0.594	0.606	V
Feedback Input Current			1	50	nA
Peak Current Limit	(Note 3)	300	400		mA
Maximum Duty Cycle	V _{FB2} = 0.54V	● 100			%
Minimum Duty Cycle	V _{FB2} = 0.66V	●		0	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $PV_{IN1} = PV_{IN2} = 3.6\text{V}$, $V_{OUT1} = 3.3\text{V}$ unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Threshold	V_{FB2} Falling		-11.3	-7.7	-4.1	%
Power Good Hysteresis				2.5		%
Buck-Boost Converter						
Output Voltage		●	2.2		5.25	V
PMOS Switch Resistance				0.29		Ω
NMOS Switch Resistance				0.22		Ω
NMOS Switch Leakage	$V_{SW1A} = V_{SW1B} = 5\text{V}$, $PV_{IN1} = PV_{IN2} = 5\text{V}$			0.1	5	μA
PMOS Switch Leakage	$V_{SW1A} = V_{SW1B} = 0\text{V}$, $PV_{IN1} = PV_{IN2} = 5\text{V}$			0.1	10	μA
Feedback Voltage	(Note 4)	●	0.97	1	1.03	V
Feedback Input Current				1	50	nA
Average Current Limit	(Note 3)		0.65	0.85		A
Burst Mode Current Limit			230	340		mA
Reverse Current Limit	(Note 3)			250		mA
Maximum Duty Cycle	$V_{FB1} = 0.9\text{V}$	●	70	80		%
Minimum Duty Cycle	$V_{FB1} = 1.1\text{V}$	●		0		%
PGOOD Threshold	V_{FB1} Falling		-12	-10	-8	%
Power Good Hysteresis				2.5		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3522 is guaranteed to meet performance specifications from 0°C to 85°C . Specifications over the -40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

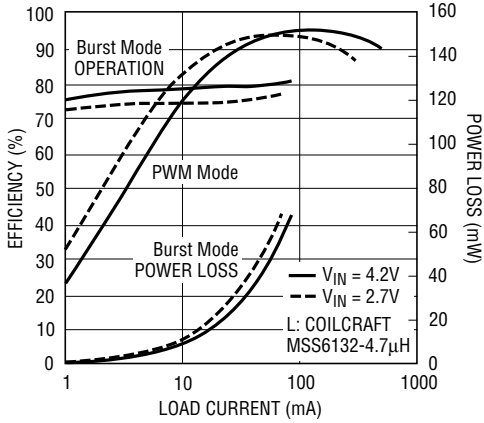
Note 3: Current measurements are performed when the LTC3522 is not switching. The current limit values in operation will be somewhat higher due to the propagation delay of the comparators.

Note 4: The LTC3522 is tested in a proprietary non-switching test mode that connects each FB pin to the output of the respective error amplifier.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

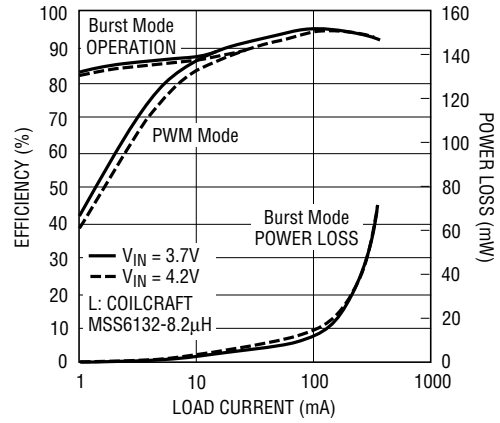
TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Buck-Boost Efficiency, Li-Ion to 3.3V



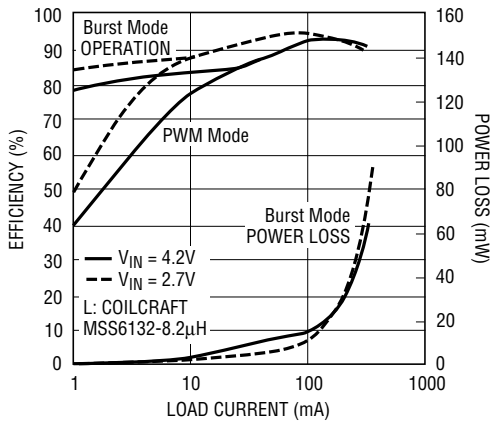
3522 G01

Buck Efficiency, Li-Ion to 2.5V



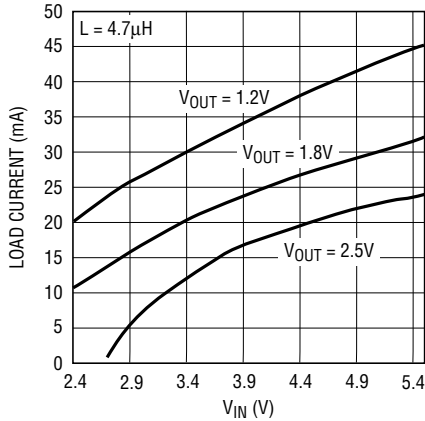
3522 G02

Buck Efficiency, Li-Ion to 1.8V



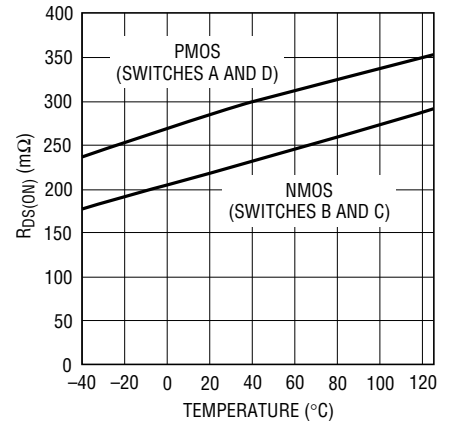
3522 G03

Buck Burst Mode Threshold



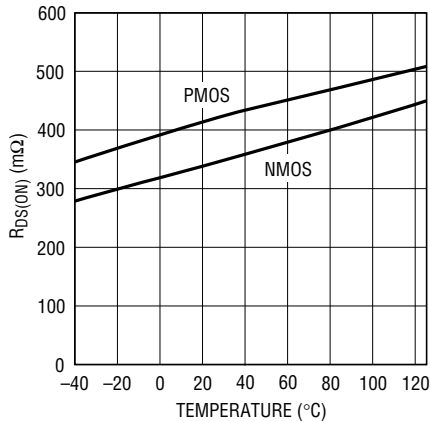
3522 G04

Buck-Boost Switch $R_{DS(ON)}$



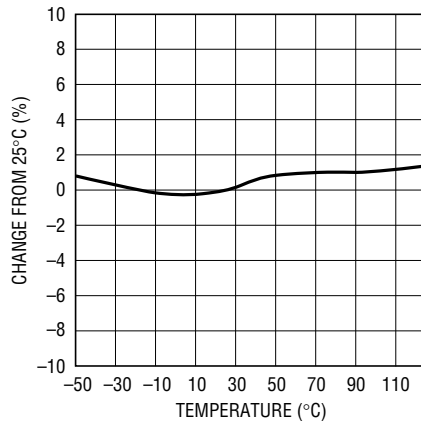
3522 G05

Buck Switch $R_{DS(ON)}$



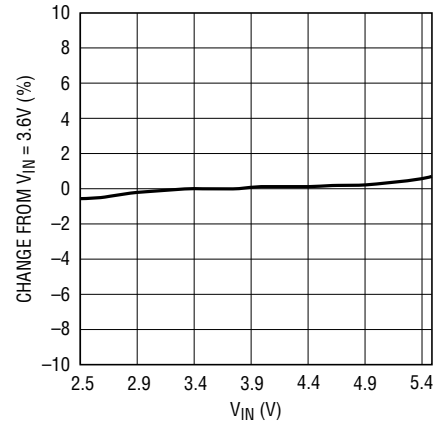
3522 G06

Switching Frequency vs Temperature



3522 G07

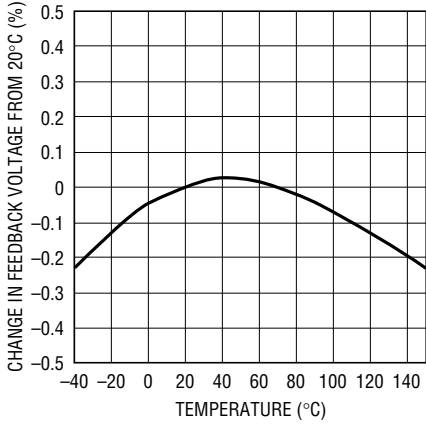
Switching Frequency vs V_{IN}



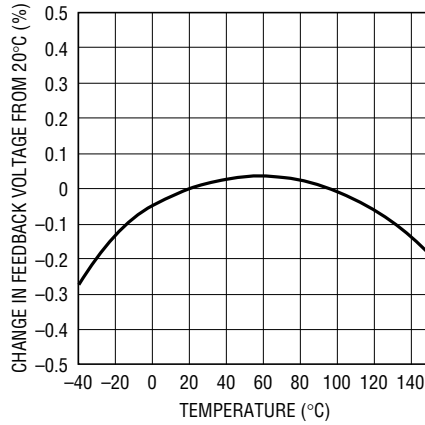
3522 G08

TYPICAL PERFORMANCE CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

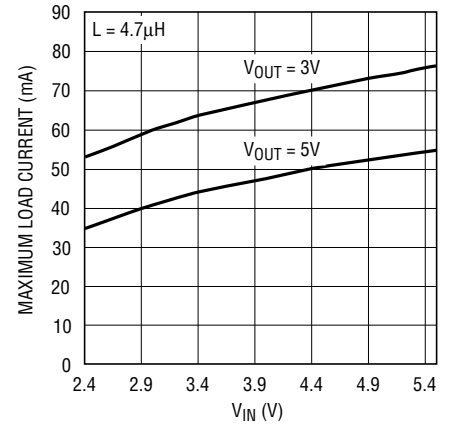
Buck-Boost Feedback Voltage vs Temperature



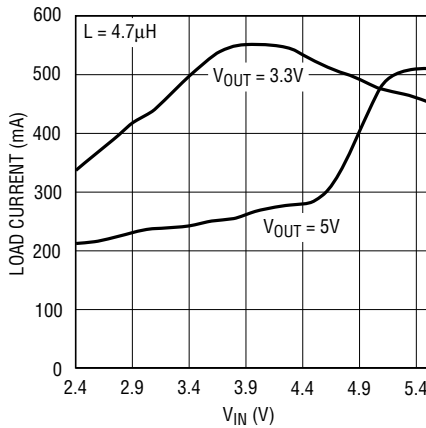
Buck Feedback Voltage vs Temperature



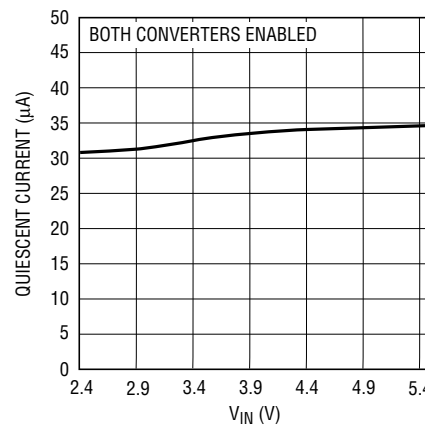
Buck-Boost Maximum Load Current, Burst Mode Operation



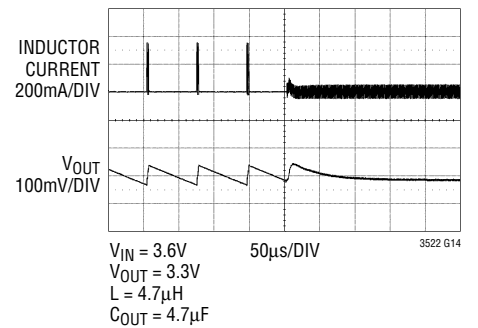
Buck-Boost Maximum Load Current, PWM Mode



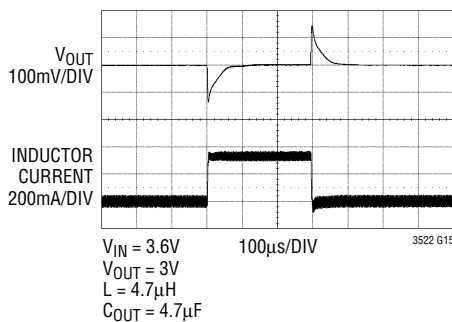
No Load Quiescent Current vs VIN



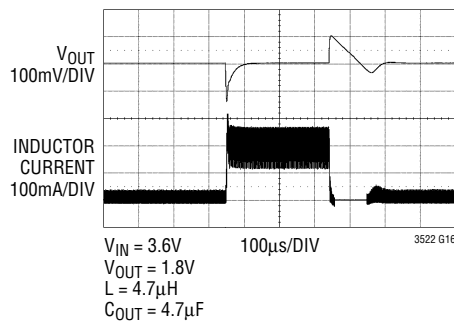
Buck-Boost Burst to PWM Transition



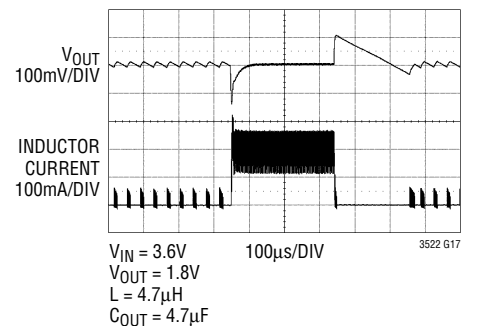
Buck-Boost Load Step, 0mA to 300mA



Buck Load Step, PWM Mode, 5mA to 200mA



Buck Load Step, Burst Mode Operation, 5mA to 200mA



PIN FUNCTIONS

FB2 (Pin 1): Feedback Voltage for the Buck Converter Derived from a Resistor Divider on the Buck Output Voltage. The buck output voltage is given by the following equation where R1 is a resistor between FB2 and ground and R2 is a resistor between FB2 and the buck output voltage:

$$V_{\text{OUT}} = 0.594V \left(1 + \frac{R2}{R1} \right)$$

PWM (Pin 2): Logic Input Used to Choose Between Burst and PWM Mode Operation for Both Converters. This pin cannot be left floating.

PWM = Low: Burst Mode operation is enabled on both converters. The buck converter will operate in Burst Mode operation at light current but will automatically transition to PWM operation at higher currents. The buck converter can supply its maximum output current (200mA) in this mode. The buck-boost converter will operate in variable frequency mode and can only supply a reduced load current (typically 50mA).

PWM = High: Both converters are forced into low noise 1MHz PWM mode operation. The buck converter will remain at constant frequency operation until its minimum on-time is reached. The buck-boost converter will remain in PWM mode at all load currents.

GND (Pin 3): Small-Signal Ground Used as a Ground Reference for the Internal Circuitry of the LTC3522.

PGOOD2 (Pin 4): This pin is an open-drain output which will only pull low if the buck converter is enabled and one or more of the following conditions occurs: the buck output voltage is out of regulation, the part is in overtemperature shutdown or the part is in undervoltage lockout.

FB1 (Pin 5): Feedback Voltage for the Buck-Boost Converter Derived from a Resistor Divider on the Buck-Boost Output Voltage. The buck-boost output voltage is given by the following equation where R1 is a resistor between FB1 and ground and R2 is a resistor between FB1 and the buck-boost output voltage:

$$V_{\text{OUT}} = 1V \left(1 + \frac{R2}{R1} \right)$$

PGOOD1 (Pin 6): This pin is an open-drain output which will only pull low if the buck-boost converter is enabled and one or more of the following conditions occurs: the buck-boost output voltage is out of regulation, the part is in overtemperature shutdown, the part is in undervoltage lockout or the buck-boost converter is in current limit. See the Operation section of this data sheet for details on the functionality of this pin in PWM mode.

SHDN1 (Pin 7): Buck-Boost Active-Low Shutdown Pin. Forcing this pin above 1.4V enables the buck-boost converter. Forcing this pin below 0.4V disables the buck-boost converter. This pin cannot be left floating.

PV_{IN1} (Pin 8): High Current Power Supply Connection Used to Supply Switch A of the Buck-Boost Converter. This pin should be bypassed by a 4.7µF or larger ceramic capacitor. The bypass capacitor should be placed as close to the pin as possible and should have a short return path to ground. **Pins PV_{IN1} and PV_{IN2} must be connected together in the application circuit.**

PGND2 (Pin 9): High Current Ground Connection for the Buck-Boost Switch C. The PCB trace connecting this pin to ground should be made as short and wide as possible.

PIN FUNCTIONS

SW1B (Pin 10): Buck-Boost Switch Node That Must be Connected to One Side of the Buck-Boost Inductor.

SW1A (Pin 11): Buck-Boost Switch Node That Must be Connected to One Side of the Buck-Boost Inductor.

V_{OUT1} (Pin 12): Buck-Boost Output Voltage Node. This pin should be connected to a low ESR output capacitor. The capacitor should be placed as close to the IC as possible and should have a short return to ground.

PGND1 (Pin 13): High Current Ground Connection for Buck-Boost Switch B and the Buck Converter Synchronous Rectifier. The PCB trace connecting this pin to ground should be made as short and wide as possible.

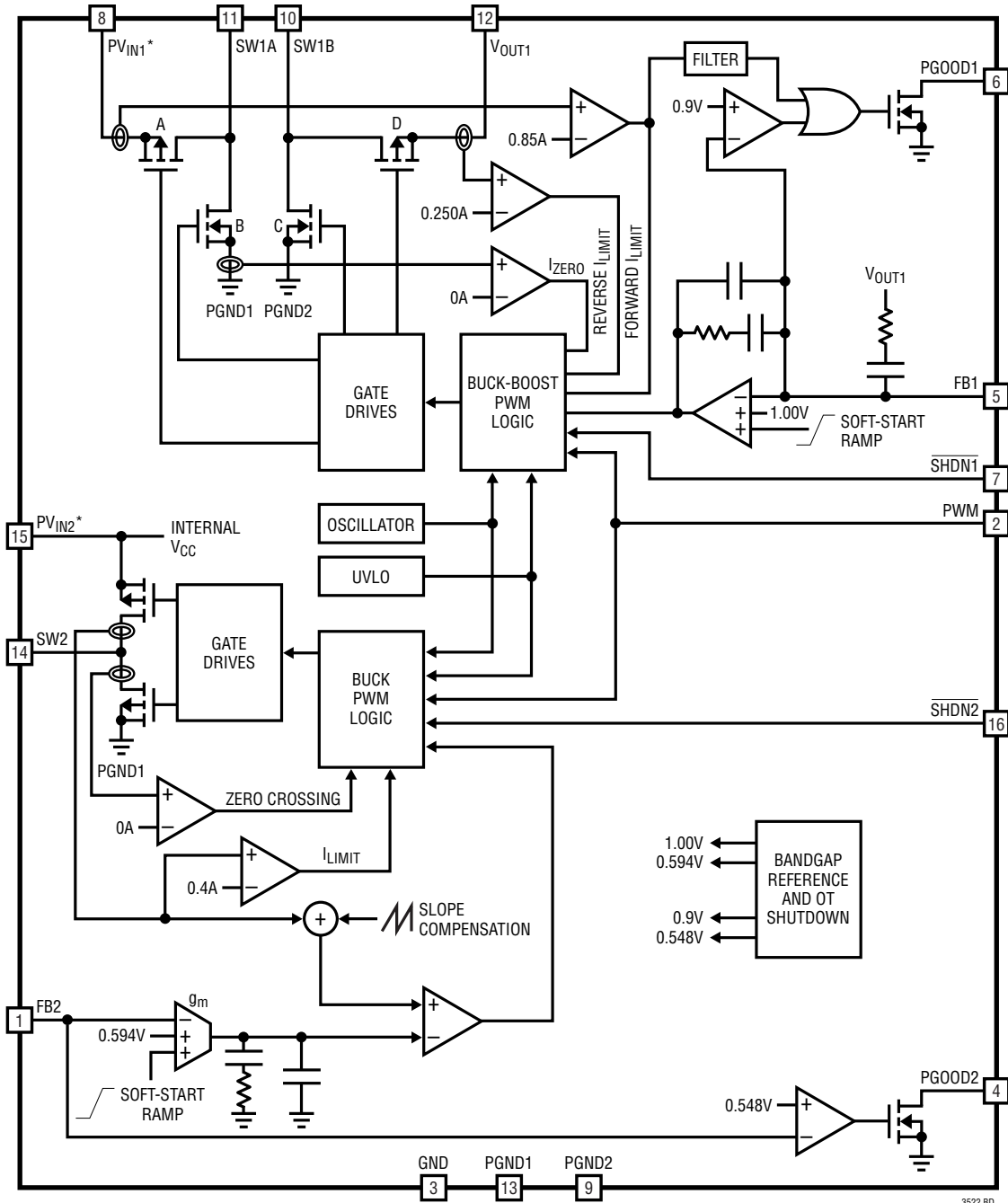
SW2 (Pin 14): Buck Converter Switch Node That Must be Connected to the Buck Inductor.

PV_{IN2} (Pin 15): High Current Power Supply Connection Used to Supply the Buck Converter Power Switch. In addition this pin is the supply pin for the internal circuitry of the LTC3522. This pin should be bypassed by a 4.7 μ F or larger ceramic capacitor. The bypass capacitor should be placed as close to the pin as possible and should have a short return path to ground. **Pins PV_{IN1} and PV_{IN2} must be connected together in the application circuit.**

SHDN2 (Pin 16): Buck Active-Low Shutdown Pin. Forcing this pin above 1.4V enables the buck converter. Forcing this pin below 0.4V disables the buck converter. This pin cannot be left floating.

Exposed Pad (Pin 17): The Exposed Pad must be electrically connected to ground. Pins PGND1, PGND2, GND, and the Exposed Pad must be connected together in the application circuit.

BLOCK DIAGRAM



*PV_{IN1} AND PV_{IN2} MUST BE CONNECTED TOGETHER IN THE APPLICATION.

3522f BD

OPERATION

The LTC3522 combines a synchronous buck DC/DC converter and a 4-switch buck-boost DC/DC converter in a single 3mm × 3mm QFN package. The buck-boost converter utilizes a proprietary switching algorithm which allows its output voltage to be regulated above, below or equal to the input voltage. The buck converter provides a high efficiency lower voltage output and supports 100% duty cycle operation to extend battery life. In Burst Mode operation, the combined quiescent current for both converters is reduced to 25 μ A. Both converters operate from the same internal 1MHz oscillator.

BUCK CONVERTER OPERATION

PWM Mode Operation

When the PWM pin is held high, the LTC3522 buck converter uses a constant frequency, current mode control architecture. Both the main (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) switches are internal. At the start of each oscillator cycle, the P-channel switch is turned on and remains on until the current waveform with superimposed slope compensation ramp exceeds the error amplifier output. At this point, the synchronous rectifier is turned on and remains on until the inductor current falls to zero or a new switching cycle is initiated. As a result, the buck converter operates with discontinuous inductor current at light loads which improves efficiency. At extremely light loads, the minimum on-time of the main switch will be reached and the buck converter will begin turning off for multiple cycles in order to maintain regulation.

Burst Mode Operation

When the PWM pin is forced low, the buck converter will automatically transition between Burst Mode operation at sufficiently light loads (below approximately 10mA) and PWM mode at heavier loads. Burst Mode entry is determined by the peak inductor current and therefore the load current at which Burst Mode operation will be entered depends on the input voltage, the output voltage and the inductor value. Typical curves for Burst Mode entry threshold are provided in the Typical Performance

Characteristics section of this data sheet. Under dropout and near dropout conditions, Burst Mode operation will not be entered.

Dropout Operation

As the input voltage decreases to a value approaching the output regulation voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage will force the main switch to remain on for more than one cycle until 100% duty cycle operation is reached where the main switch remains on continuously. In this dropout state, the output voltage will be determined by the input voltage less the resistive voltage drop across the main switch and series resistance of the inductor.

Slope Compensation

Current mode control requires the use of slope compensation to prevent sub-harmonic oscillations in the inductor current waveform at high duty cycle operation. This is accomplished internally on the LTC3522 through the addition of a compensating ramp to the current sense signal. In some current mode ICs, current limiting is performed by clamping the error amplifier voltage to a fixed maximum. This leads to a reduced output current capability at low step-down ratios. In contrast, the LTC3522 performs current limiting prior to addition of the slope compensation ramp and therefore achieves a peak inductor current limit that is independent of duty cycle.

Short-Circuit Protection

When the output is shorted to ground, the error amplifier will saturate high and the P-channel MOSFET switch will turn on at the start of each cycle and remain on until the current limit trips. During this minimum on-time, the inductor current will increase rapidly and will decrease very slowly during the remainder of the period due to the very small reverse voltage produced by a hard output short. To eliminate the possibility of inductor current runaway in this situation, the buck converter switching frequency is reduced to approximately 250kHz when the voltage on FB2 falls below 0.3V.

OPERATION

Soft-Start

The buck converter has an internal voltage mode soft-start circuit with a nominal duration of 600 μ s. The converter remains in regulation during soft-start and will therefore respond to output load transients which occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load current.

Error Amplifier and Compensation

The LT3522 buck converter utilizes an internal transconductance error amplifier. Compensation of the feedback loop is performed internally to reduce the size of the application circuit and simplify the design process. The compensation network has been designed to allow use of a wide range of output capacitors while simultaneously ensuring rapid response to load transients.

PGOOD2 Comparator

The PGOOD2 pin is an open-drain output which indicates the status of the buck converter. If the buck output voltage falls 7.7% below the regulation voltage, the PGOOD2 open-drain output will pull low. The output voltage must rise 2.5% above the falling threshold before the pull-down will turn off. In addition, there is a 60 μ s typical deglitching delay in the flag in order to prevent false trips due to voltage transients on load steps. The PGOOD2 output will also pull low during overtemperature shutdown and undervoltage lockout to indicate these fault conditions. The PGOOD2 output is only active if the buck converter is enabled.

BUCK-BOOST CONVERTER OPERATION

PWM Mode Operation

When the PWM pin is held high, the LTC3522 buck-boost converter operates in a constant frequency PWM mode with voltage mode control. A proprietary switching algorithm allows the converter to switch between buck, buck-boost and boost modes without discontinuity in inductor current or loop characteristics. The switch topology for the buck-boost converter is shown in Figure 1.

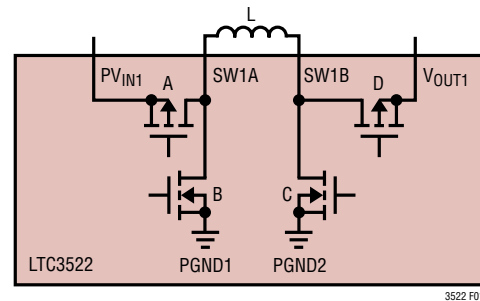


Figure 1. Buck-Boost Switch Topology

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A and B are pulse width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 85%, the switch pair AC begins turning on for a small fraction of the switching period. As the input voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionally. As the input voltage drops below the output voltage, the AC phase will eventually increase to the point that there is no longer any BD phase. At this point, switch A remains on continuously while switch pair CD is pulse width modulated to obtain the desired output voltage. At this point, the converter is operating solely in boost mode.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple, and loop transfer function throughout all three operational modes. These advantages result in increased efficiency and stability in comparison to the traditional 4-switch buck-boost converter.

Error Amplifier and Compensation

The buck-boost converter utilizes a voltage mode error amplifier with an internal compensation network as shown in Figure 2.

Notice that resistor R2 of the external resistor divider network plays an integral role in determining the frequency

OPERATION

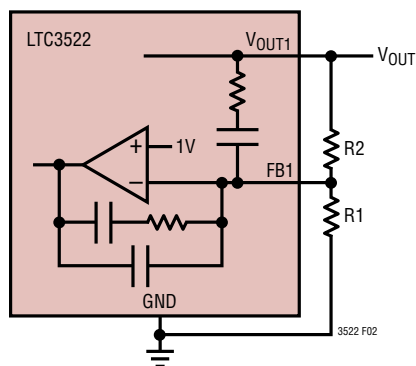


Figure 2. Buck-Boost Error Amplifier and Compensation

response of the compensation network. The ratio of R2 to R1 must be set to program the desired output voltage but this still allows the value of R2 to be adjusted to optimize the transient response of the converter. Increasing the value of R2 generally leads to greater stability at the expense of reduced transient response speed. Increasing the value of R2 can yield substantial transient response improvement in cases where the phase margin has been reduced due to the use of a small value output capacitor or a large inductance (particularly with large boost step-up ratios). Conversely, decreasing the value of R2 increases the loop bandwidth which can improve the speed of the converter's transient response. This can be useful in improving the transient response if a large valued output capacitor is utilized. In this case, the increased bandwidth created by decreasing R2 is used to counteract the reduced converter bandwidth caused by the large output capacitor.

Current Limit Operation

The buck-boost converter has two current limit circuits. The primary current limit is an average current limit circuit which injects an amount of current into the feedback node which is proportional to the extent that the switch A current exceeds the current limit value. Due to the high gain of this loop, the injected current forces the error amplifier output to decrease until the average current through switch A decreases approximately to the current limit value. The average current limit utilizes the error amplifier in an active state and thereby provides a smooth recovery with little overshoot once the current limit fault condition is removed. Since the current limit is based on the average current through switch A, the peak inductor current in

current limit will have a dependency on the duty cycle (i.e., on the input and output voltages in the overcurrent condition).

The speed of the average current limit circuit is limited by the dynamics of the error amplifier. On a hard output short, it would be possible for the inductor current to increase substantially beyond current limit before the average current limit circuit would react. For this reason, there is a second current limit circuit which turns off switch A if the current ever exceeds approximately 165% of the average current limit value. This provides additional protection in the case of an instantaneous hard output short.

Reverse Current Limit

The reverse current comparator on switch D monitors the inductor current entering V_{OUT1} . When this current exceeds 250mA (typical) switch D will be turned off for the remainder of the switching cycle.

Burst Mode Operation

With the PWM pin held low, the buck-boost converter operates utilizing a variable frequency switching algorithm designed to improve efficiency at light load and reduce the standby current at zero load. In Burst Mode operation, the inductor is charged with fixed peak amplitude current pulses. These current pulses are repeated as often as necessary to maintain the output regulation voltage. The typical output current which can be supplied in Burst Mode operation is dependent upon the input and output voltage as given by the following formula:

$$I_{OUT(MAX),BURST} = \frac{0.11 \cdot V_{IN}}{V_{IN} + V_{OUT}} \text{ (A)}$$

In Burst Mode operation, the error amplifier is not used but is instead placed in a low current standby mode to reduce supply current and improve light load efficiency.

Soft-Start

The buck-boost converter has an internal voltage mode soft-start circuit with a nominal duration of 600 μ s. The converter remains in regulation during soft-start and will therefore respond to output load transients that occur during this time. In addition, the output voltage rise time

OPERATION

has minimal dependency on the size of the output capacitor or load. During soft-start, the buck-boost converter is forced into PWM operation regardless of the state of the PWM pin.

PGOOD1 Comparator

The PGOOD1 pin is an open-drain output which indicates the status of the buck-boost converter. In Burst Mode operation (PWM = Low), the PGOOD1 open-drain output will pull low when the output voltage falls 10% below the regulation voltage. There is approximately 2.5% hysteresis in this threshold when the output voltage is returning good. In addition, there is a 60 μ s typical deglitching delay to prevent false trips due to short duration voltage transients in response to load steps.

In PWM mode, operation of the PGOOD1 comparator is complicated by the fact that the feedback pin voltage is driven to the reference voltage independent of the output voltage through the action of the voltage mode error amplifier. Since the soft-start is voltage mode, the feedback voltage will track the output voltage correctly during soft-start, and the PGOOD1 output will correctly indicate the point at which the buck-boost attains regulation at the end of soft-start. Therefore, the PGOOD1 output can be utilized for sequencing purposes. Once in regulation, the feedback voltage will no longer track the output voltage and the PGOOD1 pin will not directly respond to a loss of regulation in the output. However, the only means by which a loss of regulation can occur is if the current limit has been reached thereby preventing the buck-boost converter from delivering the required output current.

In such cases, the occurrence of current limit will cause the PGOOD1 flag to fall indicating a fault state. There can be cases, however, when the buck-boost converter is continuously in current limit, causing the PGOOD1 output to pull low, but the output voltage still remains slightly above the PGOOD1 comparator trip point.

The PGOOD1 output also pulls low during overtemperature shutdown and undervoltage lockout. The PGOOD1 output is only active if the buck-boost converter is enabled.

COMMON FUNCTIONS

Thermal Shutdown

If the die temperature exceeds 150°C (typical) both converters will be disabled. All power devices will be turned off and all switch nodes will be high impedance. The soft-start circuits for both converters are reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. Both converters will restart (if enabled) when the die temperature drops to approximately 140°C.

Undervoltage Lockout

If the supply voltage decreases below 2.3V (typical) then both converters will be disabled and all power devices will be turned off. The soft-start circuits for both converters are reset during undervoltage lockout to provide a smooth restart once the input voltage rises above the undervoltage lockout threshold.

APPLICATIONS INFORMATION

The basic LTC3522 application circuit is shown as the typical application on the front page of this data sheet. The external component selection is determined by the desired output voltages, output currents and ripple voltage requirements of each particular application. However, basic guidelines and considerations for the design process are provided in this section.

Buck Inductor Selection

The choice of buck inductor value influences both the efficiency and the magnitude of the output voltage ripple. Larger inductance values will reduce inductor current ripple and will therefore lead to lower output voltage ripple. For a fixed DC resistance, a larger value inductor will yield higher efficiency by lowering the peak current to be closer to the average. However, a larger value inductor within the same family will generally have a greater series resistance, thereby offsetting this efficiency advantage.

Given a desired peak to peak current ripple, ΔI_L , the required inductance can be calculated via the following expression, where f represents the switching frequency in MHz:

$$L = \frac{1}{f\Delta I_L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) (\mu H)$$

A reasonable choice for ripple current is $\Delta I_L = 80\text{mA}$ which represents 40% of the maximum 200mA load current. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current in order to prevent core saturation and loss of efficiency during operation. To optimize efficiency the inductor should have a low series resistance.

In particularly space restricted applications it may be advantageous to use a much smaller value inductor at the expense of larger ripple current. In such cases, the converter will operate in discontinuous conduction for a wider range of output loads and efficiency will be reduced. In addition, there is a minimum inductor value required to maintain stability of the current loop (given the fixed internal slope compensation). Specifically, if the buck converter is going to be utilized at duty cycles over 40%,

the inductance value must be at least L_{MIN} as given by the following equation:

$$L_{MIN} = 2.5 \cdot V_{OUT} (\mu H)$$

Table 1 depicts the minimum required inductance for several common output voltages.

Table 1. Buck Minimum Inductance

OUTPUT VOLTAGE	MINIMUM INDUCTANCE
0.6V	1.5 μ H
0.8V	2.0 μ H
1.2V	3.0 μ H
2.0V	5.0 μ H
2.7V	6.8 μ H
3.3V	8.3 μ H

Buck Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck output in order to minimize voltage ripple. Multi-layer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. In addition to controlling the ripple magnitude, the value of the output capacitor also sets the loop crossover frequency and therefore can impact loop stability. There is both a minimum and maximum capacitance value required to ensure stability of the loop. If the output capacitance is too small, the loop cross-over frequency will increase to the point where switching delay and the high frequency parasitic poles of the error amplifier will degrade the phase margin. In addition, the wider bandwidth produced by a small output capacitor will make the loop more susceptible to switching noise. At the other extreme, if the output capacitor is too large, the cross-over frequency can decrease too far below the compensation zero and also lead to degraded phase margin. Table 2 provides a guideline for the range of allowable values of low ESR output capacitors. Larger value output capacitors can be accommodated provided they have sufficient ESR to stabilize the loop or by increasing the value of the feedforward capacitor in parallel with the upper resistor divider resistor.

APPLICATIONS INFORMATION

Table 2. Buck Output Capacitor Range

V _{OUT}	C _{MIN}	C _{MAX}
0.6V	15μF	300μF
0.8V	15μF	230μF
1.2V	10μF	150μF
1.8V	6.8μF	90μF
2.7V	6.8μF	70μF
3.3V	6.8μF	50μF

Buck Input Capacitor Selection

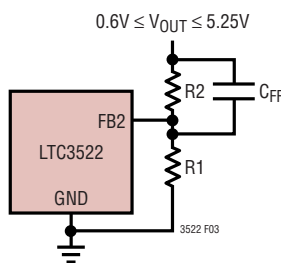
The PV_{IN2} pin provides current to the buck converter power switch and is also the supply pin for the IC's internal circuitry. It is recommended that a low ESR ceramic capacitor with a value of at least 4.7μF be used to bypass this pin. The capacitor should be placed as close to the pin as possible and have a short return to ground.

Buck Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.594V \left(1 + \frac{R2}{R1} \right)$$

The external divider is connected to the output as shown in Figure 3. It is recommended that a feedforward capacitor, C_{FF}, be placed in parallel with resistor R2 in order to improve the noise immunity of the feedback node. Table 3 provides the recommended resistor and feedforward capacitor combinations for common output voltage options.


Figure 3. Setting the Buck Output Voltage
Table 3. Buck Resistor Divider Values

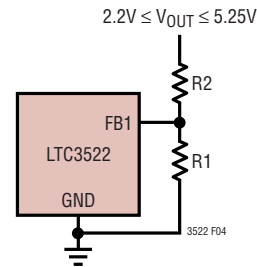
V _{OUT}	R1	R2	C _{FF}
0.6V	–	0	–
0.8V	200k	69.8k	12pF
1.0V	118k	80.6k	12pF
1.2V	100k	102k	12pF
1.5V	78.7k	121k	12pF
1.8V	68.1k	137k	12pF
2.7V	63.4k	226k	18pF
3.3V	60.4k	274k	20pF

Buck-Boost Output Voltage Programming

The buck-boost output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 1V \left(1 + \frac{R2}{R1} \right)$$

The external divider is connected to the output as shown in Figure 4. The buck-boost converter utilizes voltage mode control and the value of R2 plays an integral role in the dynamics of the feedback loop. In general, a larger value for R2 will increase stability and reduce the speed of the transient response. A smaller value of R2 will reduce stability but increase the transient response speed. A good starting point is to choose R2 = 1M, and then calculate the required value of R1 to set the desired output voltage according to the formula given above. If a large output capacitor is used, the bandwidth of the converter is reduced. In such cases R2 can be reduced to improve the transient


Figure 4. Setting the Buck-Boost Output Voltage

APPLICATIONS INFORMATION

response. If a large inductor or small output capacitor is utilized the loop will be less stable and the phase margin can be improved by increasing the value of R2.

Buck-Boost Inductor Selection

To achieve high efficiency, a low ESR inductor should be utilized for the buck-boost converter. The inductor must have a saturation rating greater than the worst case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple will be larger in buck and boost mode than in the buck-boost region. The peak-to-peak inductor current ripple for each mode can be calculated from the following formulas, where f is the frequency in MHz and L is the inductance in μH :

$$\Delta I_{L,P-P,BUCK} = \frac{1}{fL} \cdot \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}$$

$$\Delta I_{L,P-P,BOOST} = \frac{1}{fL} \cdot \frac{V_{IN}(V_{OUT} - V_{IN})}{V_{OUT}}$$

In addition to affecting output current ripple, the size of the inductor can also affect the stability of the feedback loop. In boost mode, the converter transfer function has a right half plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductor can move this zero to a frequency that is low enough to degrade the phase margin of the feedback loop. It is recommended that the inductor value be chosen less than $10\mu\text{H}$ if the buck-boost converter is to be used in the boost region.

Buck-Boost Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multi-layer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. The capacitor should be chosen large enough to reduce the output voltage ripple to acceptable levels.

Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f is the frequency in MHz, C_{OUT} is the capacitance in μF , L is the inductance in μH and I_{LOAD} is the output current in Amps:

$$\Delta V_{P-P(BOOST)} = \frac{I_{LOAD}(V_{OUT} - V_{IN})}{C_{OUT} \cdot V_{OUT} \cdot f}$$

$$\Delta V_{P-P(BUCK)} = \frac{1}{8 \cdot L \cdot C_{OUT} \cdot f^2} \cdot \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN}}$$

Since the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode. In addition to controlling the ripple magnitude, the value of the output capacitor also affects the location of the resonant frequency in the open loop converter transfer function. If the output capacitor is too small, the bandwidth of the converter will extend high enough to degrade the phase margin. To prevent this from happening, it is recommended that a minimum value of $4.7\mu\text{F}$ be used for the buck-boost output capacitor.

Buck-Boost Input Capacitor Selection

The supply current to the buck-boost converter is provided by the PV_{IN1} pin. It is recommended that a low ESR ceramic capacitor with a value of at least $4.7\mu\text{F}$ be located as close to this pin as possible.

Inductor Style and Core Material

Different inductor core materials and styles have an impact on the size and price of an inductor at any given peak current rating. Toroid or shielded pot cores in ferrite or permalloy materials are small and reduce emissions, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 4 provides a sampling

APPLICATIONS INFORMATION

of inductors that are well suited to many LTC3522 buck converter applications.

Table 4. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE	MAX CURRENT	DCR	HEIGHT
Taiyo Yuden	NP035B-4R7M	4.7 μ H	1.2A	0.047 Ω	1.8mm
	NP035B-6R8M	6.8 μ H	1.0A	0.084 Ω	1.8mm
Coilcraft	MSS6132-472ML	4.7 μ H	1.8A	0.056 Ω	3.2mm
	MSS6132-822ML	8.2 μ H	1.35A	0.070 Ω	3.2mm
Sumida	CDRH2D14NP-4R7N	4.7 μ H	1.0A	0.135 Ω	1.55mm
	CDRH2D18/HPNP-4R7N	4.7 μ H	1.2A	0.110 Ω	2.0mm
	CDRH3D16NP-4R7N	4.7 μ H	0.9A	0.08 Ω	1.8mm
Cooper-Bussmann	SD18-4R7	4.7 μ H	1.54A	0.082 Ω	1.8mm
	SD10-4R7	4.7 μ H	1.08A	0.153 Ω	1.0mm

Capacitor Vendor Information

Both the input and output capacitors used with the LTC3522 must be low ESR and designed to handle the large AC currents generated by switching converters. The vendors in Table 5 provide capacitors that are well suited to LTC3522 application circuits.

Table 5. Capacitor Vendor Information

MANUFACTURER	WEB SITE	REPRESENTATIVE PART NUMBERS
Taiyo Yuden	www.t-yuden.com	JMK107BJ105MA 4.7 μ F, 6.3V
TDK	www.component.tdk.com	C2012X5R0J475K 4.7 μ F, 6.3V
Murata	www.murata.com	GRM219R61A475K 4.7 μ F
AVX	www.avxcorp.com	SM055C475KHN480 4.7 μ F

PCB Layout Considerations

The LTC3522 switches large currents at high frequencies. Special care should be given to the PCB layout to ensure stable, noise-free operation. Figure 5 depicts the recommended PCB layout to be utilized for the LTC3522. A few key guidelines follow:

1. All circulating high current paths should be kept as short as possible. This can be accomplished by keeping the routes to all bold components in Figure 5 as short and as wide as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on PV_{IN1} and PV_{IN2} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The small-signal ground pad (GND) should have a single point connection to the power ground. A convenient way to achieve this is to short the pin directly to the Exposed Pad as shown in Figure 5.
3. The components shown in bold and their connections should all be placed over a complete ground plane.
4. To prevent large circulating currents from disrupting the output voltage sensing, the ground for each resistor divider should be returned directly to the small signal ground pin (GND).
5. Use of vias in the die attach pad will enhance the thermal environment of the converter especially if the vias extend to a ground plane region on the exposed bottom surface of the PCB.
6. Keep the connection from the resistor dividers to the feedback pins FB1 and FB2 as short as possible and away from the switch pin connections.

APPLICATIONS INFORMATION

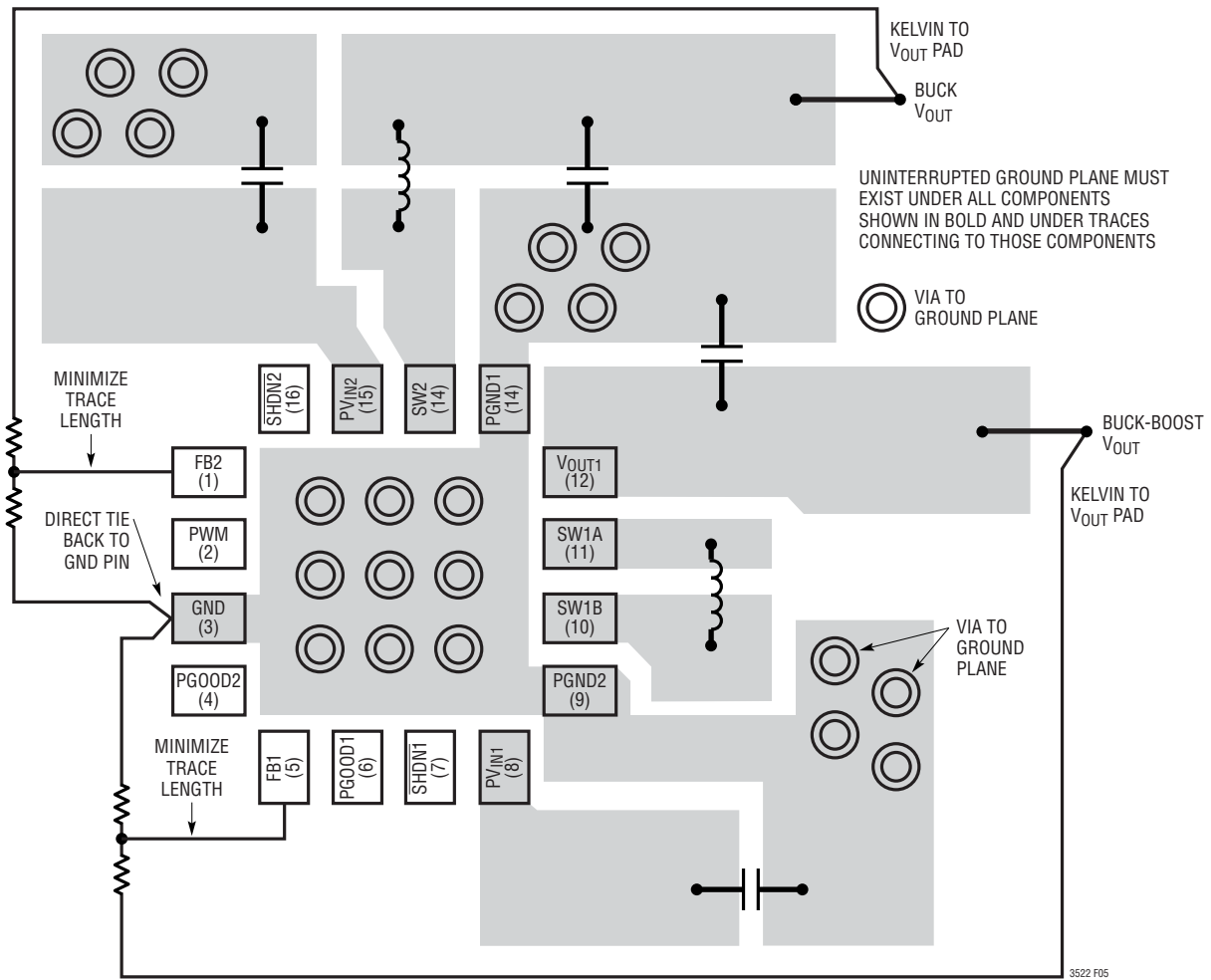
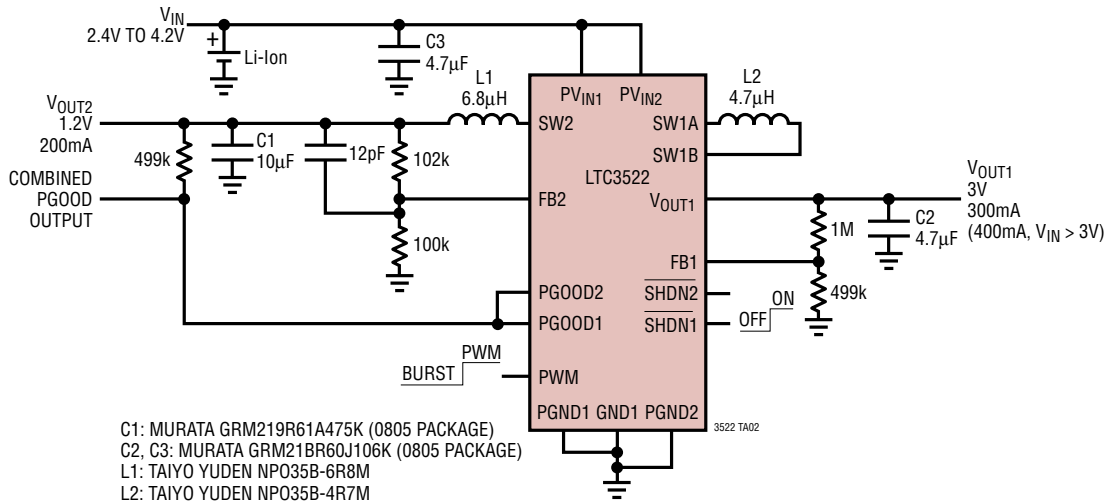


Figure 5. LTC3522 Recommended PCB Layout

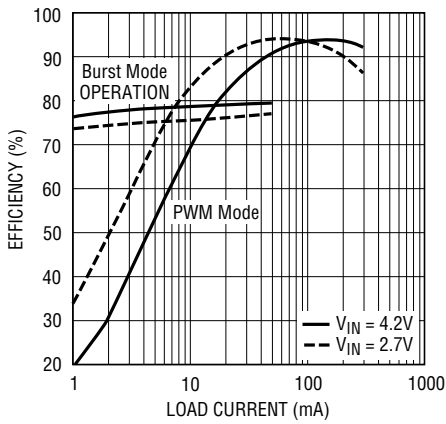
3522 F05

TYPICAL APPLICATION

Li-Ion to 3V at 400mA and 1.2V at 200mA

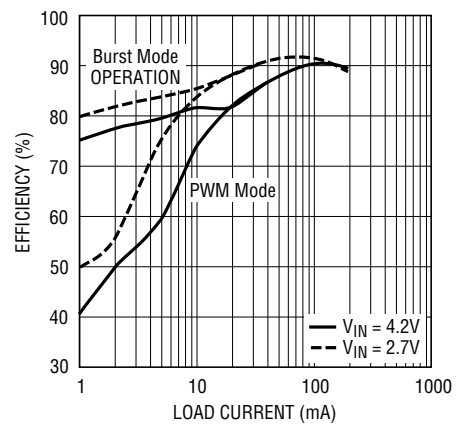


Buck-Boost Converter Efficiency vs Load Current



3522 TA02b

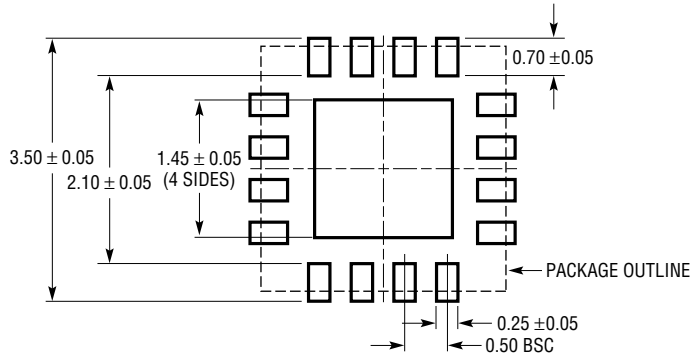
Buck Converter Efficiency vs Load Current



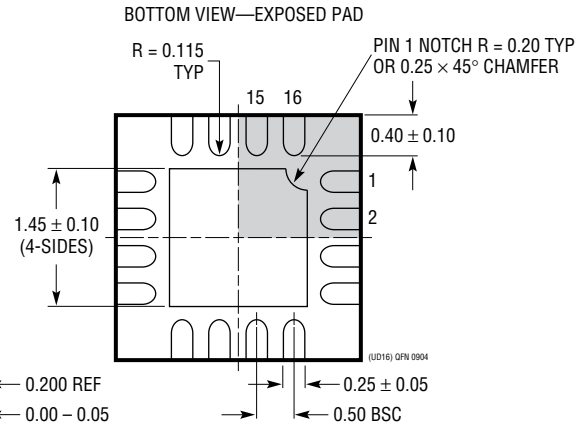
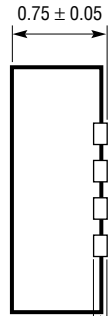
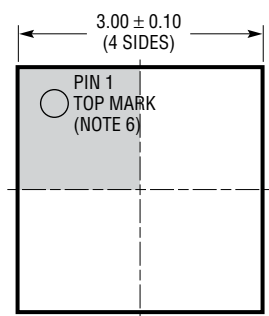
3522 TA02c

PACKAGE DESCRIPTION

UD Package 16-Lead Plastic QFN (3mm × 3mm) (Reference LTC DWG # 05-08-1691)



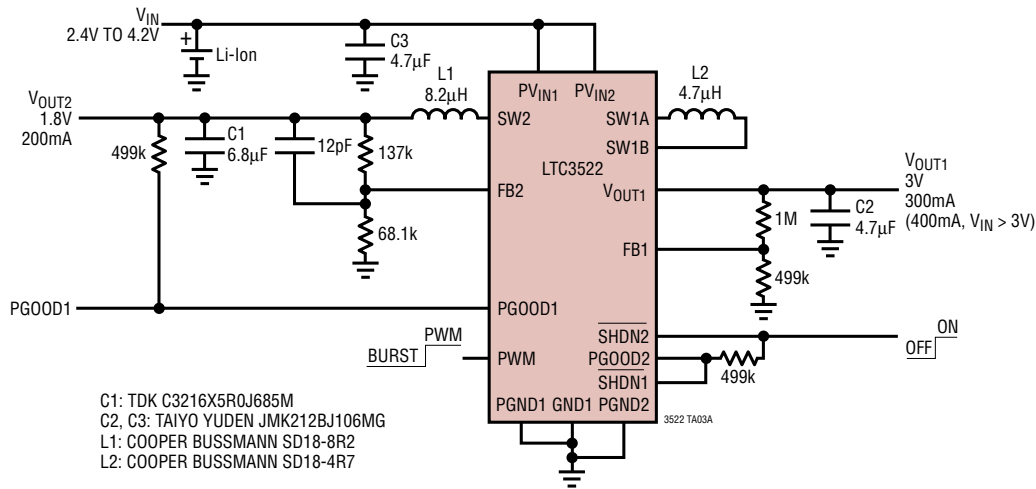
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



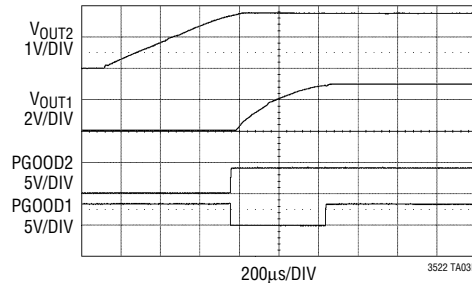
- NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

3V at 400mA and 1.8V at 200mA with Sequenced Start-Up



Sequenced Start-Up Waveforms



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3410/LTC3410B	300mA (I _{OUT}), 2.25MHz Synchronous Buck DC/DC Converter	V _{IN} : 2.5V to 5.5V, V _{OUT(RANGE)} = 0.8V to V _{IN} , I _Q = 26µA, I _{SD} < 1µA, SC70 Package
LTC3440	600mA (I _{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V _{IN} : 2.5V to 5.5V, V _{OUT(RANGE)} = 2.5V to 5.5V, I _Q = 25µA, I _{SD} < 1µA, MS, DFN Packages
LTC3441	600mA (I _{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V _{IN} : 2.5V to 5.5V, V _{OUT(RANGE)} = 2.4V to 5.25V, I _Q = 25µA, I _{SD} < 1µA, DFN Package
LTC3442	1.2A (I _{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V _{IN} : 2.4V to 5.5V, V _{OUT(RANGE)} = 2.4V to 5.25V, I _Q = 35µA, I _{SD} < 1µA, DFN Package
LTC3455	Dual DC/DC Converter with USB Power Manager and Li-Ion Battery Charger	96% Efficiency, Seamless Transition Between Inputs, I _Q = 110µA, I _{SD} < 2µA, QFN Package
LTC3456	2-Cell Multi-Output DC/DC Converter with USB Power Manager	92% Efficiency, Seamless Transition Between Inputs, I _Q = 180µA, I _{SD} < 1µA, QFN Package
LTC3530	600mA (I _{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V _{IN} : 1.8V to 5.5V, V _{OUT(RANGE)} = 1.8V to 5.5V, I _Q = 40µA, I _{SD} < 1µA, DFN, MSOP Packages
LTC3532	500mA (I _{OUT}), 2MHz Synchronous Buck-Boost DC/DC Converter	V _{IN} : 2.4V to 5.5V, V _{OUT(RANGE)} = 2.4V to 5.25V, I _Q = 35µA, I _{SD} < 1µA, DFN, MSOP Packages
LTC3544/LTC3544B	300mA, 200mA ×2, 100mA, 2.25MHz Quad Output Synchronous Step-Down DC/DC Converter	V _{IN} : 2.25V to 5.5V, V _{OUT(MIN)} = 0.8V, I _Q = 70µA, I _{SD} < 1µA, 3mm × 3mm QFN Packages

3522f