PD-93816D

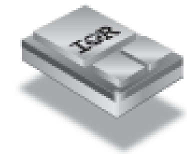
International
IOR Rectifier

IRHNA57264SE
JANSR2N7474U2
250V, N-CHANNEL
REF: MIL-PRF-19500/684
R5™ TECHNOLOGY

RADIATION HARDENED POWER MOSFET SURFACE MOUNT (SMD-2)

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number
IRHNA57264SE	100K Rads (Si)	0.06Ω	45A	JANSR2N7474U2



SMD-2

International Rectifier's R5™ technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm^2)). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Ultra Low $R_{DS(on)}$
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Surface Mount
- Ceramic Package
- Light Weight

Absolute Maximum Ratings **Pre-Irradiation**

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	45	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	28	
I_{DM}	Pulsed Drain Current ①	180	
P_D @ T_C = 25°C	Max. Power Dissipation	250	W
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	222	mJ
I_{AR}	Avalanche Current ①	45	A
E_{AR}	Repetitive Avalanche Energy ①	250	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Pckg. Mounting Surface Temp.	300 (for 5s)	
	Weight	3.3 (Typical)	g

For footnotes refer to the last page

04/25/06

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.28	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.06	Ω	V_{GS} = 12V, I_D = 28A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	V_{DS} = V_{GS}, I_D = 1.0mA
g_{fs}	Forward Transconductance	27	—	—	S (℧)	V_{DS} ≥ 15V, I_{DS} = 28A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 200V ,V_{GS}=0V
		—	—	25		V_{DS} = 200V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	165	nC	V_{GS} =12V, I_D = 45A
Q_{gs}	Gate-to-Source Charge	—	—	45		V_{DS} = 125V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	75		
$t_{d(on)}$	Turn-On Delay Time	—	—	35	ns	V_{DD} = 125V, I_D = 45A,
t_r	Rise Time	—	—	125		V_{GS} =12V, R_G = 2.35Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	80		
t_f	Fall Time	—	—	65		
$L_S + L_D$	Total Inductance	—	4.0	—	nH	Measured from the center of drain pad to center of source pad
C_{iss}	Input Capacitance	—	5045	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	781	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	70	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	45	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_j = 25°C, I_S = 45A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	560	nS	T_j = 25°C, I_F = 45A, di/dt ≤ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	8.6	µC	V_{DD} ≤ 50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	0.5	°C/W	
$R_{thJ-PCB}$	Junction-to-PC board	—	1.6	—		soldered to a 2" square copper-clad board

Note: Corresponding Spice and Saber models are available on International Rectifier web site.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si)		Units	Test Conditions
		Min	Max		
BV_{DSS}	Drain-to-Source Breakdown Voltage	250	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5		$V_{GS} = V_{DS}$, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	µA	V_{DS}= 200V, V_{GS}=0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.061	Ω	V_{GS} = 12V, I_D = 31A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (SMD-2)	—	0.060	Ω	V_{GS} = 12V, I_D = 31A
V_{SD}	Diode Forward Voltage ④	—	1.2	V	V_{GS} = 0V, I_D = 45A

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET	Energy	Range	V_{DS} (V)				
	(MeV/(mg/cm²))	(MeV)	(µm)	@VGS=0V	@VGS=-5V	@VGS=-10V	@VGS=-15V	@VGS=-20V
Br	36.7	309	39.5	250	250	250	250	250
I	59.8	341	32.5	250	250	250	250	240
Au	82.3	350	28.4	250	250	225	175	50

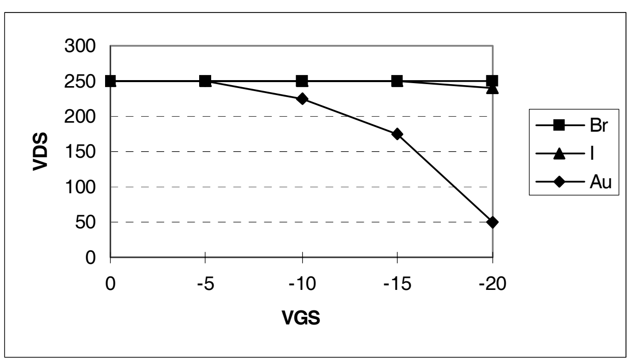


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

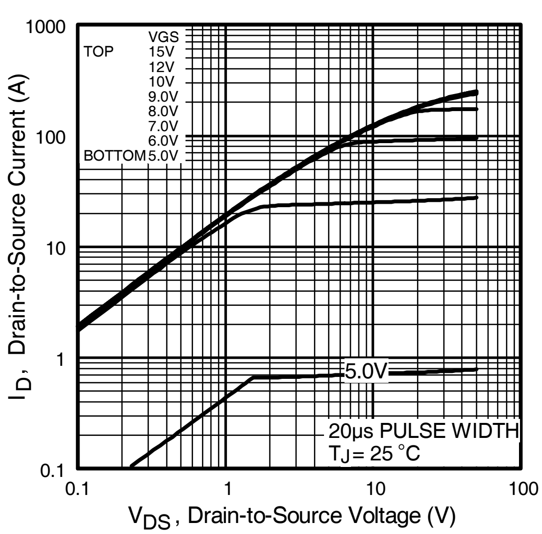


Fig 1. Typical Output Characteristics

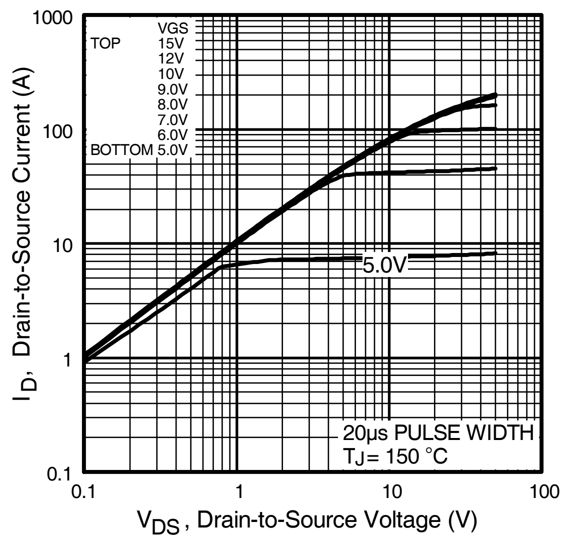


Fig 2. Typical Output Characteristics

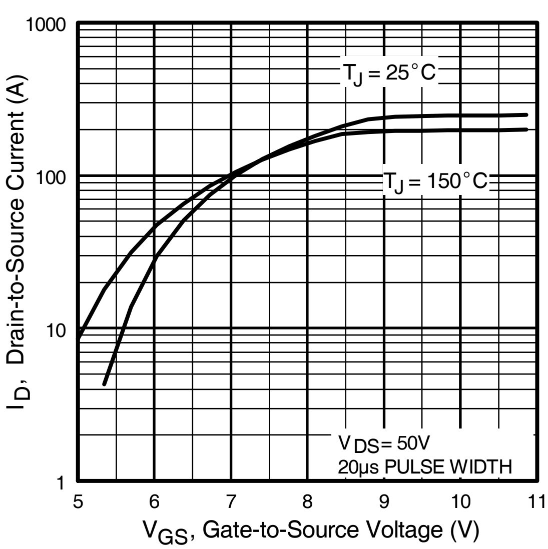


Fig 3. Typical Transfer Characteristics

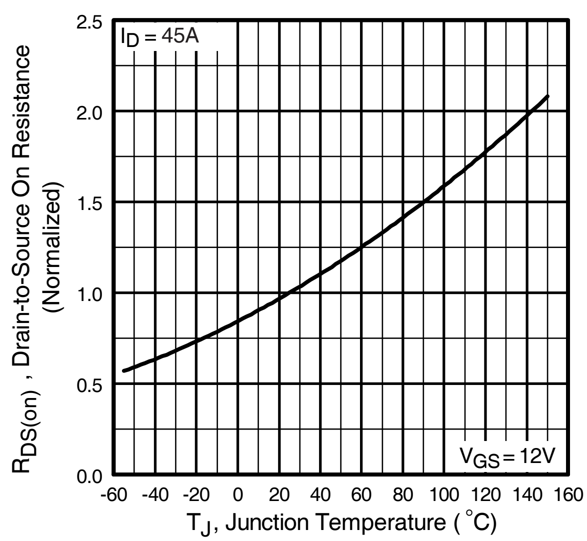


Fig 4. Normalized On-Resistance Vs. Temperature

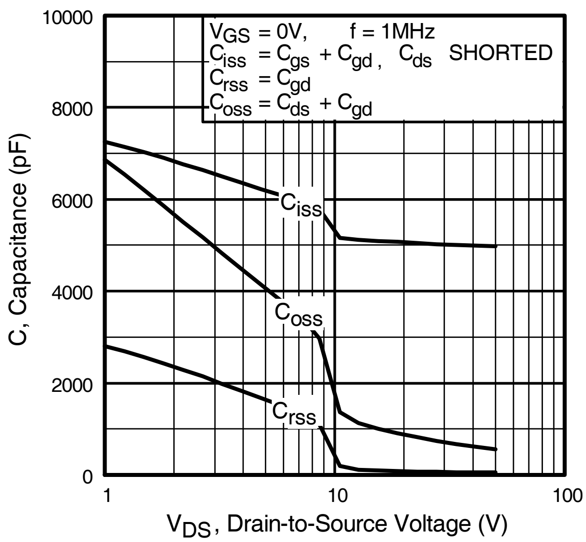


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

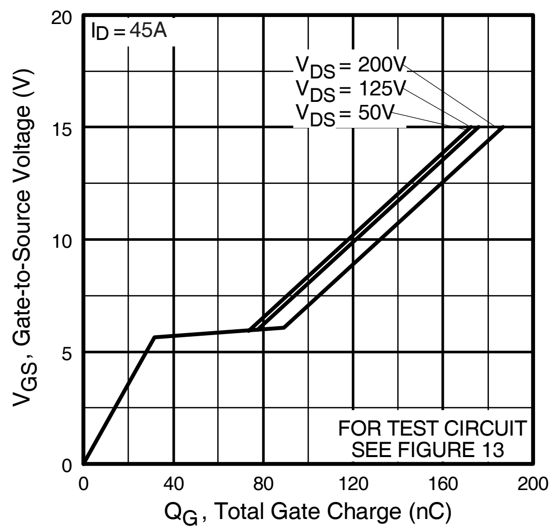


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

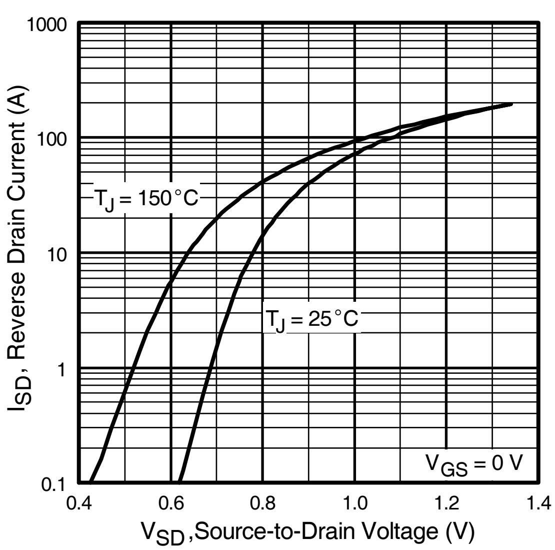


Fig 7. Typical Source-Drain Diode Forward Voltage

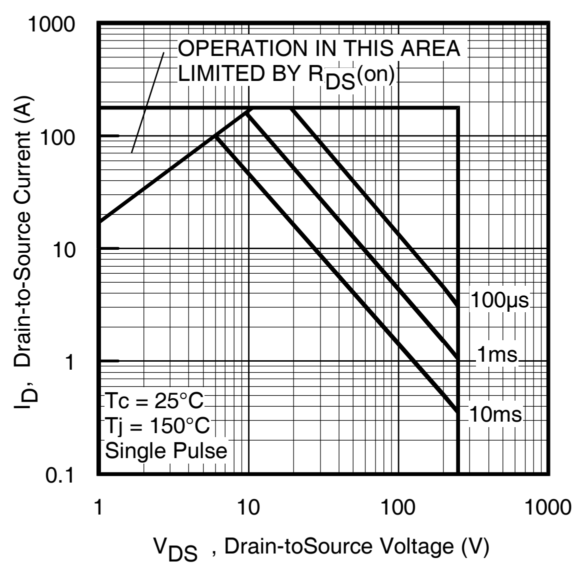


Fig 8. Maximum Safe Operating Area

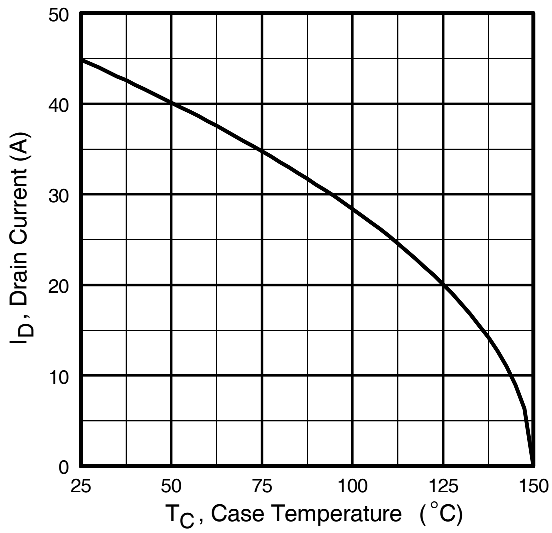


Fig 9. Maximum Drain Current Vs. Case Temperature

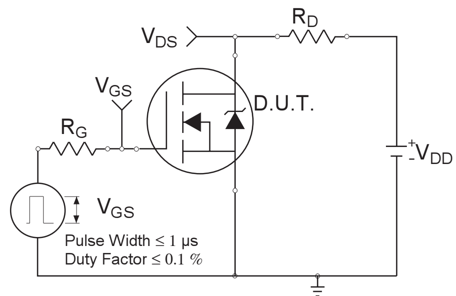


Fig 10a. Switching Time Test Circuit

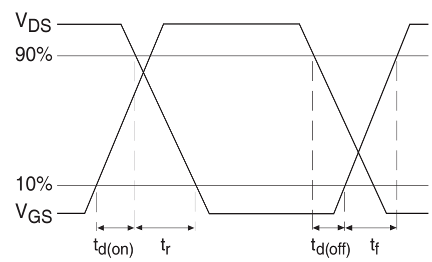


Fig 10b. Switching Time Waveforms

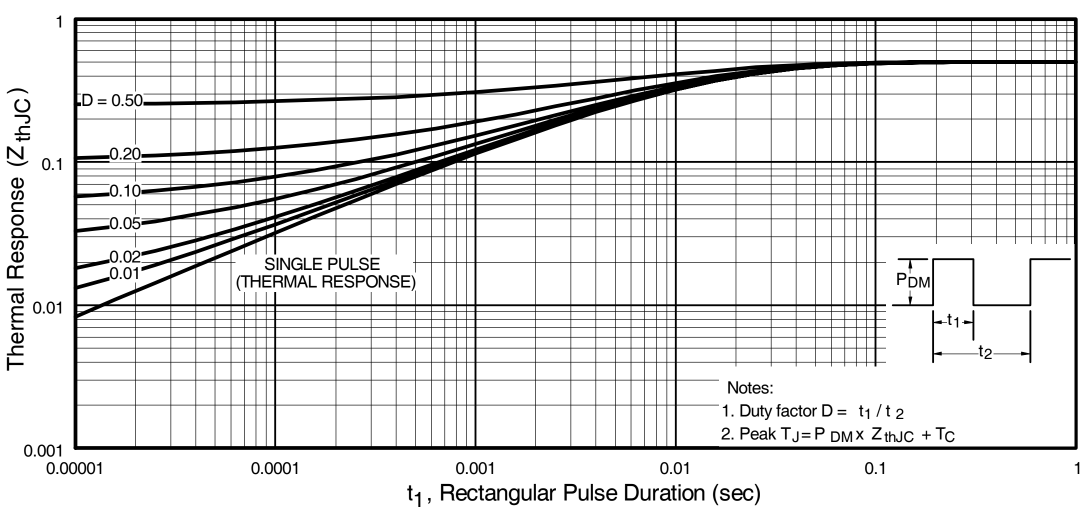


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

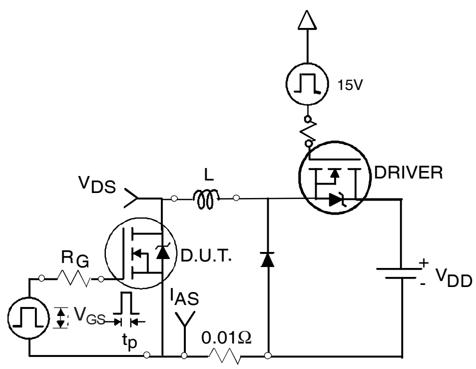


Fig 12a. Unclamped Inductive Test Circuit

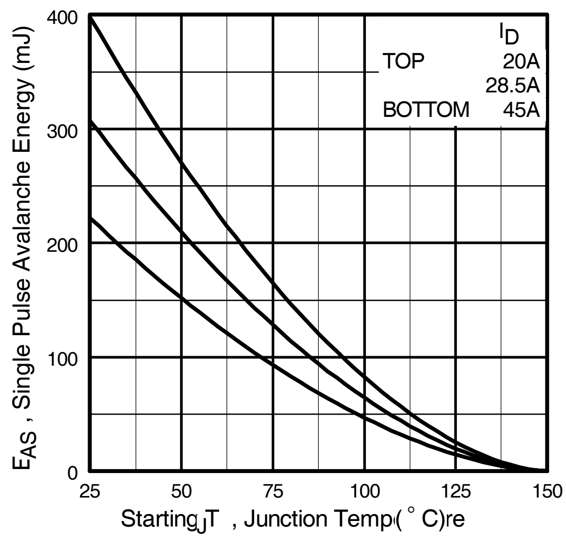


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

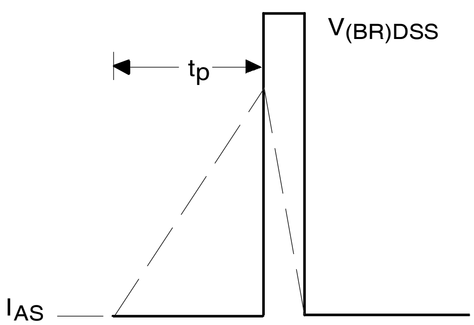


Fig 12b. Unclamped Inductive Waveforms

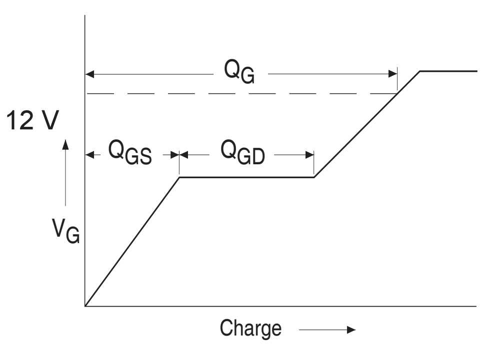


Fig 13a. Basic Gate Charge Waveform

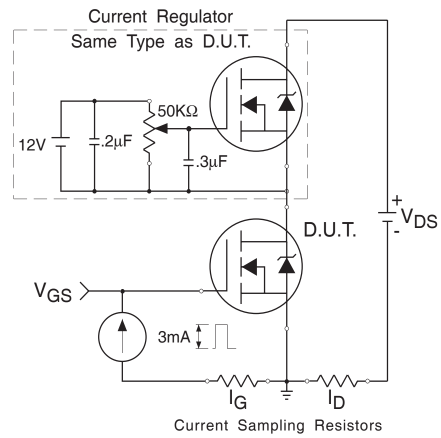


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L= 0.22mH Peak I_L = 45A, V_{GS} = 12V

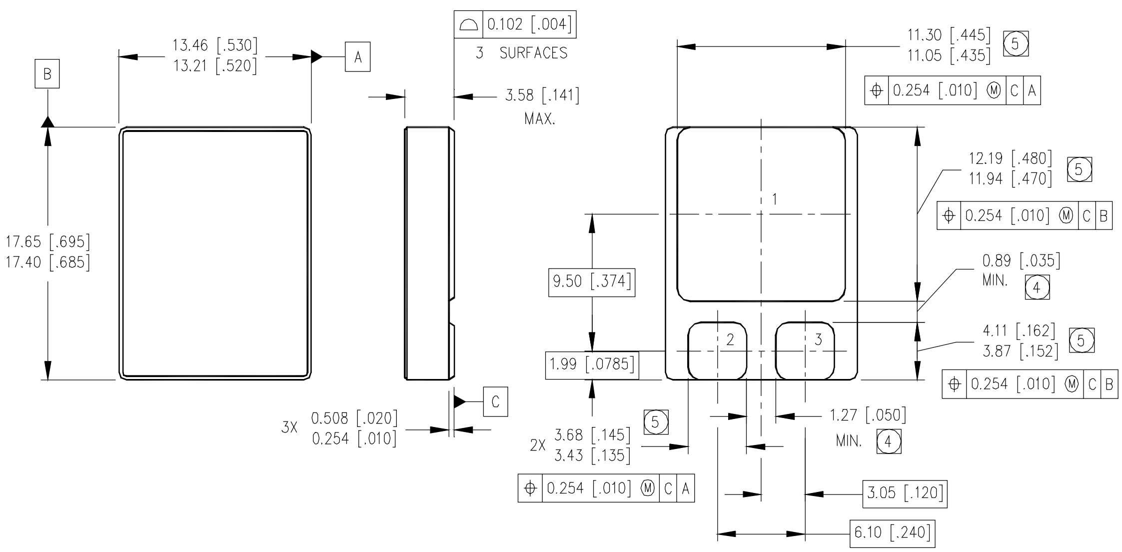
③ I_{SD} ≤ 45A, di/dt ≤ 274A/μs, V_{DD} ≤ 250V, T_J ≤ 150°C

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 200 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — SMD-2



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M−1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. DIMENSION INCLUDES METALLIZATION FLASH.
5. DIMENSION DOES NOT INCLUDE METALLIZATION FLASH.

PAD ASSIGNMENTS

1 = DRAIN
2 = GATE
3 = SOURCE

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