ANALOG DEVICES

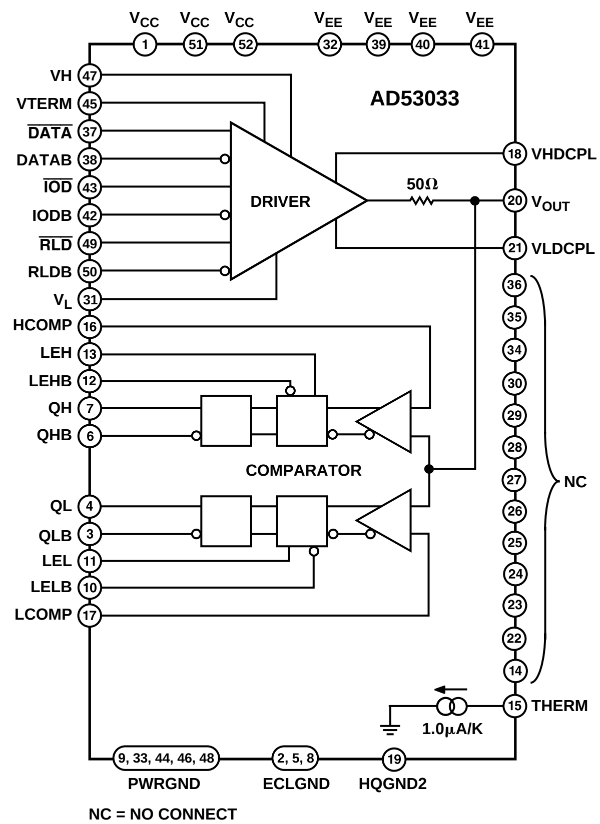
High Performance Driver/Comparator on a Single Chip

AD53033

FEATURES
250 MHz Operation
Driver/Comparator Included
52-Lead LQFP Package with Built-in Heat Sink

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation and Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD53033 is a single chip that performs the pin electronics functions of driver and comparator (D-C) in ATE VLSI and memory testers.

The driver is a proprietary design that features three active states: Data High Mode, Data Low Mode and Term Mode as well as an Inhibit State. This facilitates the implementation of high speed active termination. The output voltage range is –3 V to +8 V to accommodate a wide variety of test devices. The output leakage is typically less than 250 nA over the entire signal range.

The dual comparator, with an input range equal to the driver output range, features built-in latches and ECL-compatible outputs. The outputs are capable of driving 50 Ω signal lines terminated to –2 V. Signal tracking capability is upwards of 5 V/ns.

Also included on the chip is an onboard temperature sensor whose purpose is to give an indication of the surface temperature of the D-C. This information can be used to measure θ_{JC} and θ_{JA} or flag an alarm if proper cooling is lost. Output from the sensor is a current sink that is proportional to absolute temperature. The gain is trimmed to a nominal value of 1.0 μA/K. As an example, the output current can be sensed by using a 10 kΩ resistor connected from +10 V to the THERM (IOUT) pin. A voltage drop across the resistor will be developed that equals: $10K \times 1\ \mu A/K = 10\ mV/K = 2.98\ V$ at room temperature.

REV. 0

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AD53033–SPECIFICATIONS

DRIVER SPECIFICATIONS

(All specifications are at T_J = +85°C ± 5°C, +V_S = +12 V ± 3%, –V_S = –7 V = ±3% unless otherwise noted. All temperature coefficients are measured at T_J = +75°C to +95°C). CHDCPL = CLDCPL = 39 nF.

Parameter	Min	Typ	Max	Units	Test Conditions
DIFFERENTIAL INPUT CHARACTERISTICS					
(DATA to $\overline{\text{DATA}}$, IOD to $\overline{\text{IOD}}$, RLD to $\overline{\text{RLD}}$)					
Input Voltage	–2		0	V	
Differential Input Range		ECL			
Bias Current	–250		+250	µA	V_{IN} = –2 V, 0.0 V
REFERENCE INPUTS					
Bias Currents	–50		+50	µA	V_L, V_H, V_T = 5 V
OUTPUT CHARACTERISTICS					
Logic High Range	–2		8	V	DATA = H, V_H = –2 V to +8 V V_L = –3 V (V_H = –2 V to +6 V) V_L = –1 V (V_H = +6 V to +8 V)
Logic Low Range	–3		5	V	DATA = L, V_L = –3 V to +5 V, V_H = +6 V
Amplitude (V_H and V_L)	0.1		9	V	V_L = 0.0 V, V_H = +0.1 V, V_T = 0 V
Absolute Accuracy					V_L = –2 V, V_H = +7 V, V_T = 0 V
V_H Offset	–50		+50	mV	DATA = H, V_H = 0 V, V_L = –3 V, V_T = +3 V
V_H Gain + Linearity Error	0.3 – 5		+0.3 + 5	% of V_H + mV	DATA = H, V_H = –2 V to +8 V, V_L = –3 V, V_T = +3 V
V_L Offset	–50		+50	mV	DATA = L, V_L = –3 V, V_H = +6 V, V_T = +7.5 V
V_L Gain + Linearity Error	–0.3 – 5		+0.3 + 5	% of V_L + mV	DATA = L, V_L = 0 V , V_H = +6 V, V_T = +7.5 V
Offset TC		0.5		mV/°C	V_L = 0 V, V_H = +5 V, V_T = 0 V
Output Resistance					
V_H = –2 V	44	46	48	Ω	V_L = –3 V, V_T = 0 V, I_{OUT} = 0, +1, +30 mA
V_H = +8 V	44	46	48	Ω	V_L = –1 V, V_T = 0 V, I_{OUT} = 0, –1, –30 mA
V_L = –3 V	44	46	48	Ω	V_H = +6 V, V_T = 0 V, I_{OUT} = 0, +1, +30 mA
V_L = +5 V	44	46	48	Ω	V_H = +6 V, V_T = 0 V, I_{OUT} = 0, –1, –30 mA
V_H = +3 V		46		Ω	V_L = 0 V, V_T = 0 V, I_{OUT} = –30 mA (Trim Point)
Dynamic Current Limit	100			mA	C_{BYP} = 39 nF, V_H = +7 V, V_L = –2 V, V_T = 0 V
Static Current Limit	–85		+85	mA	Output to –3 V, V_H = +8 V, V_L = –1 V, V_T = 0 V DATA = H and Output to +8 V, V_H = +6 V, V_L = –3 V, V_T = 0 V, DATA = L
V_{TERM}					
Voltage Range	–3		8.0	V	TERM MODE, V_T = –3 V to +8 V, V_L = 0 V, V_H = 3 V
V_{TERM} Offset	–50		+50	mV	TERM MODE, V_T = 0 V, V_L = 0 V, V_H = 3 V
V_{TERM} Gain + Linearity Error	–0.3 + 5		+0.3 + 5	% of V_{SET} + mV	TERM MODE, V_T = –3 V to +8 V, V_L = 0 V, V_H = 3 V
Offset TC		0.5		mV/°C	V_T = 0 V, V_L = 0 V, V_H = 3 V
Output Resistance	44	46	49	Ω	I_{OUT} = +30 mA, +1.0 mA, V_T = –3.0 V, V_H = 3 V, V_L = 0 V I_{OUT} = –30 mA, –1.0 mA, V_T = +8.0 V, V_H = 3 V, V_L = 0 V I_{OUT} = ±30 mA, ±1.0 mA, V_T = 0 V, V_H = 3 V, V_L = 0 V
DYNAMIC PERFORMANCE, (V_H AND V_L)					
Propagation Delay Time	1.1	1.6	2.1	ns	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Propagation Delay TC		2		ps/°C	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Delay Matching, Edge to Edge		<100		ps	Measured at 50%, V_H = +400 mV, V_L = –400 mV
Rise and Fall Times					
1 V Swing		0.6		ns	Measured 20%–80%, V_L = 0 V, V_H = 1 V
3 V Swing		1.0		ns	Measured 20%–80%, V_L = 0 V, V_H = 3 V
5 V Swing		1.7		ns	Measured 10%–90%, V_L = 0 V, V_H = 5 V
9 V Swing		3.0		ns	Measured 10%–90%, V_L = –2 V, V_H = 7 V
Rise and Fall Time Temperature Coefficient					
1 V Swing		±1		ps/°C	Measured 20%–80%, V_L = 0 V, V_H = 1 V
3 V Swing		±2		ps/°C	Measured 20%–80%, V_L = 0 V, V_H = 3 V
5 V Swing		±4		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 5 V
Overshoot and Preshoot	–3.0 – 50		+3.0 + 50	% of Step + mV	V_L, V_H = –0.1 V, 0.1 V, V_L, V_H = 0.0 V, 1.0 V V_L, V_H = 0.0 V, 3.0 V, V_L, V_H = 0.0 V, 5.0 V V_L, V_H = –2.0 V, 7.0 V
Settling Time					
to 15 mV		<50		ns	V_L = 0 V, V_H = 0.5 V
to 4 mV		<10		µs	V_L = 0 V, V_H = 0.5 V

Parameter	Min	Typ	Max	Units	Test Conditions
Delay Change vs. Pulsewidth		<50		ps	V_L = 0 V, V_H = 2 V
Minimum Pulsewidth					
3 V Swing		2		ns	V_L = 0 V, V_H = 3 V, 90% Reached, Measure @ 50%
5 V Swing		3		ns	V_L = 0 V, V_H = 5 V, 90% Reached, Measure @ 50%
Toggle Rate		250		MHz	V_L = 0 V, V_H = 5 V, VDUT > 3.0 V p-p
DYNAMIC PERFORMANCE, INHIBIT					
Delay Time, Active to Inhibit	1.5		4.0	ns	Measured at 50%, V_H = +2 V, V_L = –2 V
Delay Time, Inhibit to Active	1.5		3.5	ns	Measured at 50%, V_H = +2 V, V_L = –2 V
Delay Time Matching (Z)			±2.2	ns	Z = Delay Time Active to Inhibit Test (Above)—Delay Time Inhibit to Active Test (Above) (Of Worst Two Edges)
I/O Spike		<200		mV, p-p	V_H = 0 V, V_L = 0 V
Rise, Fall Time, Active to Inhibit			3.5	ns	V_H = +2 V, V_L = –2 V (Measured 20%/80% of 1 V Output)
Rise, Fall Time, Inhibit to Active			2.2	ns	V_H = +2 V, V_L = –2 V (Measured 20%/80% of 1 V Output)
DYNAMIC PERFORMANCE , V_{TERM}					
Delay Time, V_H to V_{TERM}			3.0	ns	Measured at 50%, V_L = V_H = +0.4 V, V_{TERM} = –0.4 V
Delay Time, V_L to V_{TERM}			5.0	ns	Measured at 50%, V_L = V_H = +0.4 V, V_{TERM} = –0.4 V
Delay Time, V_{TERM} to V_H and V_{TERM} to V_L			4.0	ns	Measured at 50%, V_L = V_H = +0.4 V, V_{TERM} = –0.4 V
Overshoot and Preshoot	–3.0 + 75		+3.0 + 75	% of Step + mV	V_H/V_L, V_{TERM} = (+0.4 V, –0.4 V), (0.0 V, –2.0 V), (0.0 V, +7.0 V)
V_{TERM} Mode Rise Time			4.0	ns	V_L, V_H = 0 V, V_{TERM} = –2 V, 20%–80%
V_{TERM} Mode Fall Time			5.5	ns	V_L, V_H = 0 V, V_{TERM} = –2 V, 20%–80%
PSRR, DRIVE or TERM Mode		35		dB	V_S = V_S ± 3%

Specifications subject to change without notice.

COMPARATOR SPECIFICATIONS

(All specifications are at T_J = +85°C ± 5°C, +V_S = +12 V ± 3%, –V_S = –7 V = ±3% unless otherwise noted. All temperature coefficients are measured at T_J = +75°C to +95°C).

Parameter	Min	Typ	Max	Units	Test Conditions
DC INPUT CHARACTERISTICS					
Offset Voltage (V_{OS})	–25		25	mV	CMV = 0 V
Offset Voltage (Drift)		50		µV/°C	CMV = 0 V
HCOMP, LCOMP Bias Current	–50		50	µA	V_{IN} = 0 V
Voltage Range (V_{CM})	–3		8.0	V	
Differential Voltage (V_{DIFF})			9.0	V	
Gain and Linearity	–0.05		0.05	% FSR	V_{IN} = –3 V to +8 V
LATCH ENABLE INPUTS					
Logic "1" Current (I_{IH})			250	µA	LE, $\overline{LE}$ = –0.8 V
Logic "0" Current (I_{IL})	–250			µA	LE, $\overline{LE}$ = –1.8 V
DIGITAL OUTPUTS					
Logic "1" Voltage (V_{OH})	–0.98			V	Q or $\overline{Q}$, 50 Ω to –2 V
Logic "0" Voltage (V_{OL})			–1.5	V	Q or $\overline{Q}$, 50 Ω to –2 V
Slew Rate		1		V/ns	
SWITCHING PERFORMANCE					
Propagation Delay					
Input to Output	0.9		2.5	ns	V_{IN} = 2 V p-p,
Latch Enable to Output		2		ns	HCOMP = +1 V, LCOMP = +1 V
Propagation Delay Temperature Coefficient		2		ps/°C	
Propagation Delay Change with Respect to					
Slew Rate: 0.5 V, 1.0 V, 3.0 V/ns		<±100		ps	V_{IN} = 0 V to 5 V
Slew Rate: 5.0 V/ns		<±350		ps	V_{IN} = 0 V to 5 V
Amplitude: 1.0 V, 3.0 V, 5.0 V		<±200		ps	V_{IN} = 1.0 V/ns
Equivalent Input Rise Time		450		ps	V_{IN} = 0 V to 3 V, 3 V/ns
Pulsewidth Linearity		<±200		ps	V_{IN} = 0 V to 3 V, 3 V/ns, PW = 3 ns–8 ns
Settling Time		<25		ns	Settling to ±8 mV, V_{IN} = 1 V to 0 V
Latch Timing					
Input Pulsewidth		<1.5		ns	
Setup Time		<1.0		ns	
Hold Time		<1.0		ns	

Specifications subject to change without notice.

AD53033–SPECIFICATIONS

TOTAL FUNCTION SPECIFICATIONS

(All specifications are at T_J = +85°C ± 5°C, $+V_S$ = +12 V ± 3%, $–V_S$ = –7 V = ±3% unless otherwise noted. All temperature coefficients are measured at T_J = +75°C to +95°C).

Parameter	Min	Typ	Max	Units	Test Conditions
OUTPUT CHARACTERISTICS					
Output Leakage Current, V_{OUT} = –2 V to +7 V	–500		+500	nA	
Output Leakage Current, V_{OUT} = –3 V to +8 V	–2		+2	µA	
Output Capacitance		6		pF	Driver INHIBITED
POWER SUPPLIES					
Total Supply Range		19		V	
Positive Supply		12		V	
Negative Supply		–7		V	
Positive Supply Current			178	mA	Driver = Active
Negative Supply Current			195	mA	Driver = Active
Total Power Dissipation			3.5	W	Driver = Active
Temperature Sensor Gain Factor	0.7	1	1.4	µA/K	R_{LOAD} = 10 kΩ, V_{SOURCE} = +10 V

NOTES
Connecting or shorting the decoupling pins to ground will result in the destruction of the device.

Specifications subject to change without notice.

Table I. Driver Truth Table

DATA	$\overline{\text{DATA}}$	IOD	$\overline{\text{IOD}}$	RLD	$\overline{\text{RLD}}$	OUTPUT STATE
0	1	1	0	X	X	VL
1	0	1	0	X	X	VH
X	X	0	1	0	1	INH
X	X	0	1	1	0	VTERM

Table II. Comparator Truth Table

V_{OUT}		LEH	$\overline{\text{LEH}}$	LEL	$\overline{\text{LEL}}$	OUTPUT STATES QH	$\overline{\text{QH}}$	QL	$\overline{\text{QL}}$
>HCOMP	>LCOMP	1	0	1	0	1	0	1	0
>HCOMP	<LCOMP	1	0	1	0	1	0	0	1
<HCOMP	>LCOMP	1	0	1	0	0	1	1	0
<HCOMP	<LCOMP	1	0	1	0	0	1	0	1
X	X	0	1	0	1	QH (t-1)	$\overline{\text{QH}}$ (t-1)	QL (t-1)	$\overline{\text{QL}}$ (t-1)

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage
- $+V_S$ to GND . . . . +13 V
- $–V_S$ to GND . . . . –8 V
- $+V_S$ to $–V_S$ . . . . +20 V
- PWR GND to ECL GND or HQ GND . . . . ±0.4 V

Inputs
- DATA, $\overline{\text{DATA}}$, IOD, $\overline{\text{IOD}}$, RLD, $\overline{\text{RLD}}$ . . . . . . +5 V, –3 V
- DATA to $\overline{\text{DATA}}$, IOD to $\overline{\text{IOD}}$, RLD to $\overline{\text{RLD}}$ . . . . . . ±3 V
- LEL, $\overline{\text{LEL}}$, LEH, $\overline{\text{LEH}}$ . . . . +5 V, –3 V
- LEL to $\overline{\text{LEL}}$, LEH to $\overline{\text{LEH}}$ . . . . ±3 V
- VH, VL, VTERM to GND . . . . +9 V, –4 V
- VH to VL . . . . ±11 V
- (VH – VTERM) and (VTERM – VL) . . . . ±11 V
- HCOMP . . . . +9 V, –4 V
- LCOMP . . . . +9 V, –4 V
- HCOMP, LCOMP to V_{OUT} . . . . ±11 V

Outputs
- V_{OUT} Short Circuit Duration . . . . Indefinite[2]
- V_{OUT} Inhibit Mode . . . . +9 V, –4 V
- VHDCPL . . . . Do Not Connect Except for Cap to V_{CC}
- VLDCPL . . . . Do Not Connect Except for Cap to V_{EE}
- QH, $\overline{\text{QH}}$, QL, $\overline{\text{QL}}$ Maximum I_{OUT}
  - Continuous . . . . 50 mA
  - Surge . . . . 100 mA
- THERM . . . . +13 V, 0 V

Environmental
- Operating Temperature (Junction) . . . . +175°C
- Storage Temperature . . . . –65°C to +150°C
- Lead Temperature (Soldering, 10 sec)[3] . . . . +260°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Output short circuit protection to ground is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.

[3]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ±5°C (75°F ± 10°F) with relative humidity not to exceed 65%.

Table III. Package Thermal Characteristics

Air Flow, FM	θ_{JA}, °C/W
0	33
200	25
400	22

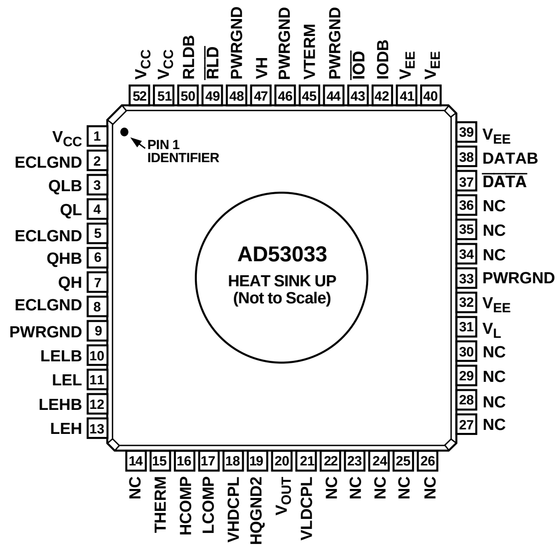
ORDERING GUIDE

Model	Package Description	Shipment Method Quantity per Shipping Container	Package Option
AD53033JSTP	52-Lead LQFP-EDQUAD	90	SQ-52

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD53033 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

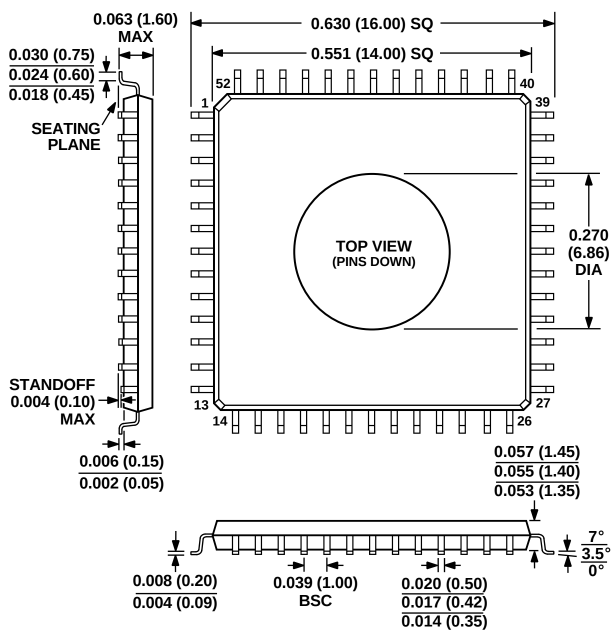


NC = NO CONNECT

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead LQFP–EDQUAD with Integral Heat Slug (SQ-52)



CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED

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