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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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2SJ574

Silicon P Channel MOS FET High Speed Switching

RENESAS

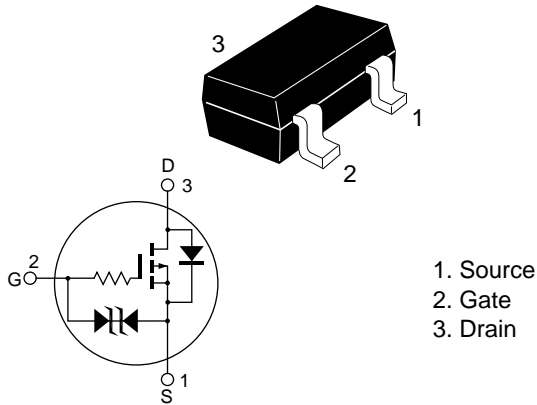
ADE-208-739B (Z)
3rd.Edition.
June 1999

Features

- Low on-resistance
 $R_{DS} = 1.1 \Omega$ typ. ($V_{GS} = -10 \text{ V}$, $I_D = -150 \text{ mA}$)
 $R_{DS} = 2.2 \Omega$ typ. ($V_{GS} = -4 \text{ V}$, $I_D = -150 \text{ mA}$)
- 4 V gate drive device.
- Small package (MPAK)

Outline

MPAK



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-300	mA
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-1.2	A
Body-drain diode reverse drain current	I_{DR}	-300	mA
Channel dissipation	Pch ^{Note 2}	400	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value on the alumina ceramic board (12.5x20x0.7mm)

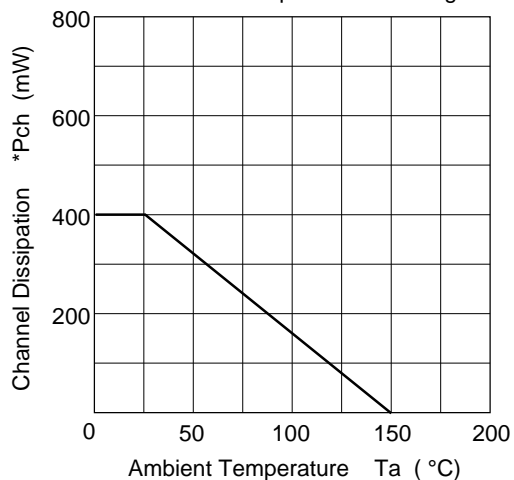
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 16 V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.3	—	-2.3	V	$I_D = -10 \mu A, V_{DS} = -5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.1	1.3	Ω	$I_D = -150 mA, V_{GS} = -10 V$ ^{Note 3}
	$R_{DS(on)}$	—	2.2	3.1	Ω	$I_D = -150 mA, V_{GS} = -4 V$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	195	300	—	mS	$I_D = -150 mA, V_{DS} = -10 V$ ^{Note 3}
Input capacitance	Ciss	—	50	—	pF	$V_{DS} = -10 V$
Output capacitance	Coss	—	40	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	15	—	pF	f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$I_D = -150 mA, V_{GS} = -10 V$
Rise time	t_r	—	50	—	ns	$R_L = 66.6 \Omega$
Turn-off delay time	$t_{d(off)}$	—	110	—	ns	
Fall time	t_f	—	105	—	ns	

Note: 3. Pulse test
 4. Marking is BP

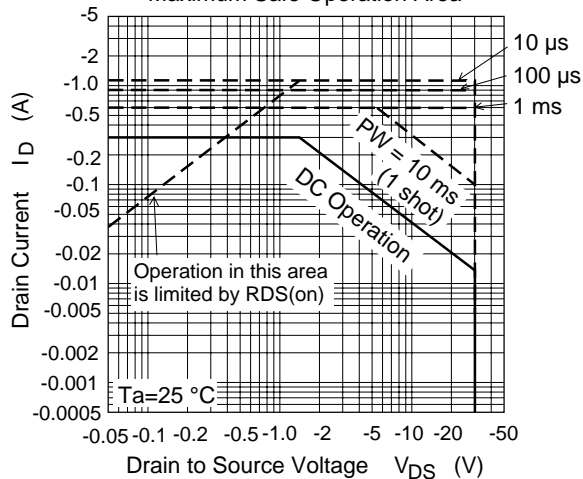
Main Characteristics

Power vs. Temperature Derating



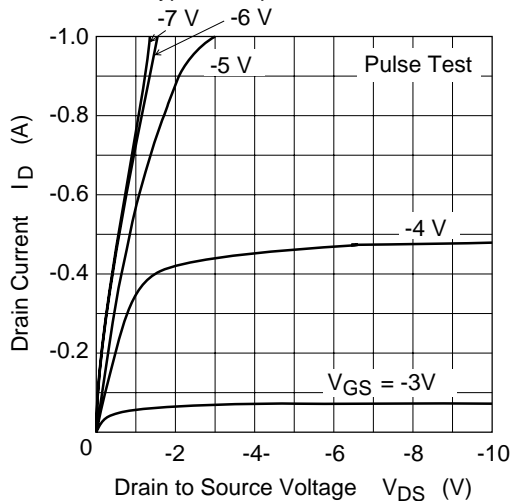
*Value on the alumina ceramic board.(12.5x20x0.7mm)

Maximum Safe Operation Area

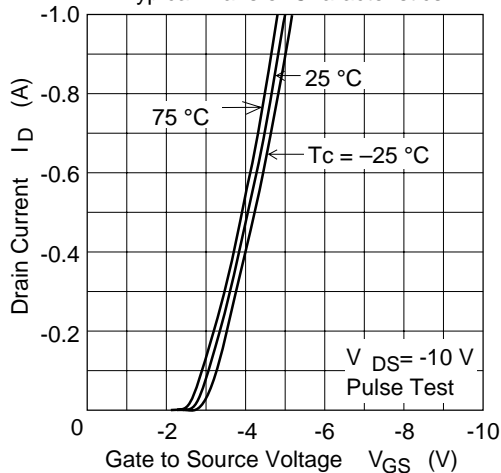


Value on the alumina ceramic board.(12.5x20x0.7mm)

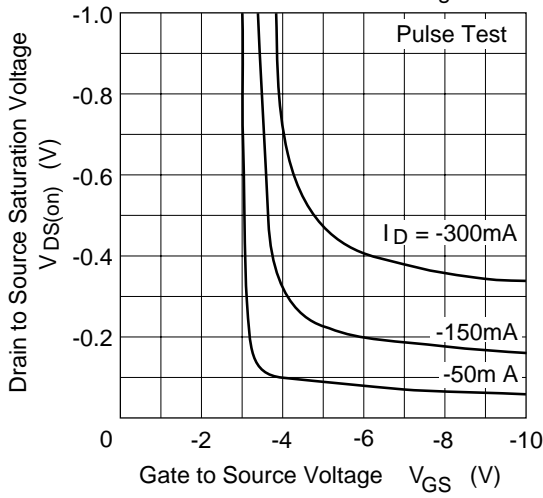
Typical Output Characteristics



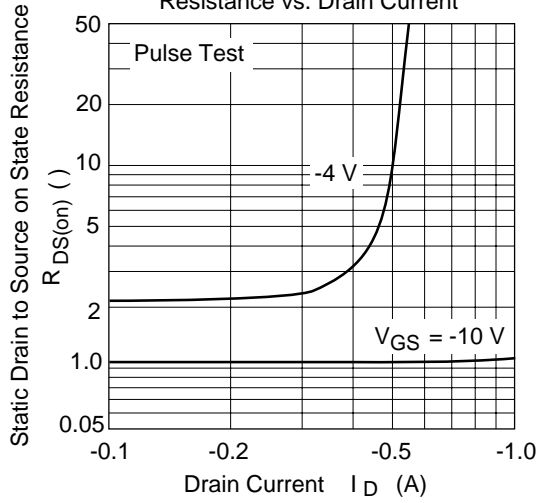
Typical Transfer Characteristics



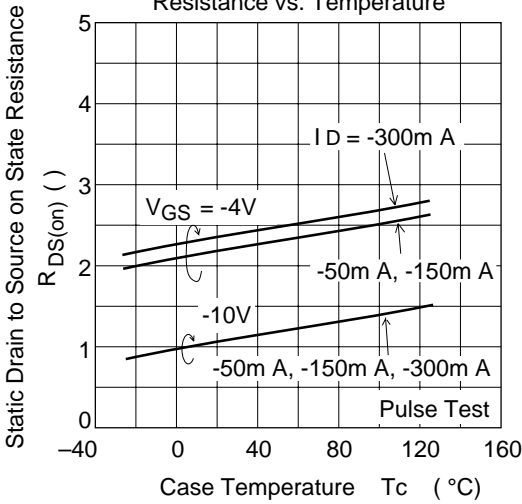
Drain to Source Saturation Voltage vs. Gate to Source Voltage



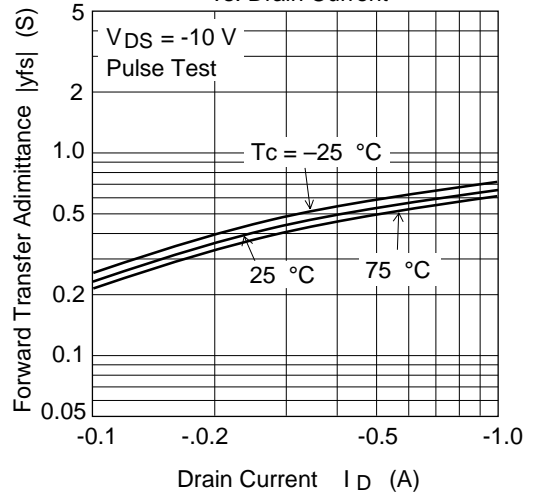
Static Drain to Source on State Resistance vs. Drain Current

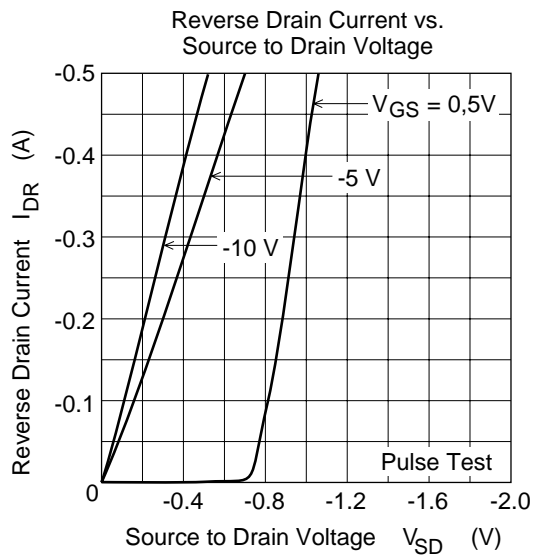
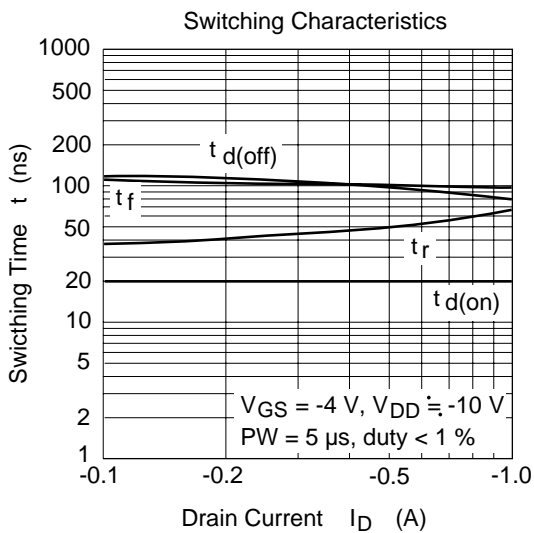
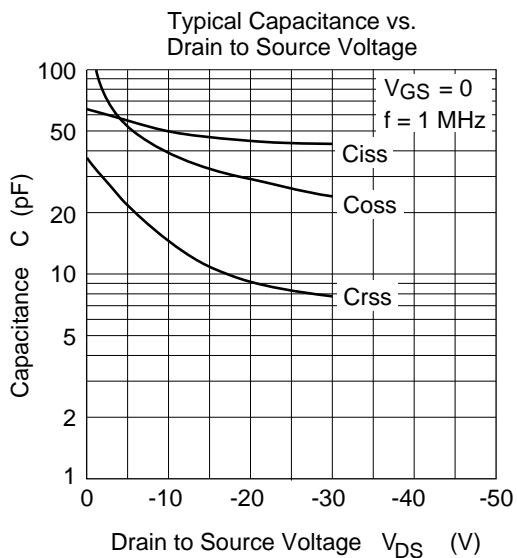


Static Drain to Source on State Resistance vs. Temperature

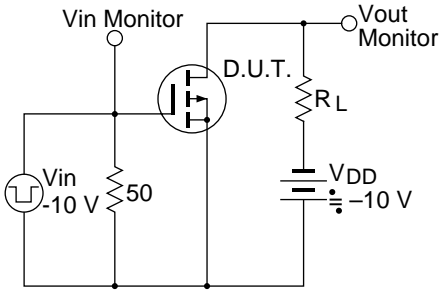


Forward Transfer Admittance vs. Drain Current

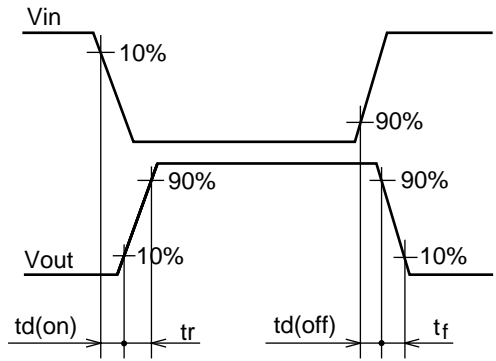




Switching Time Test Circuit

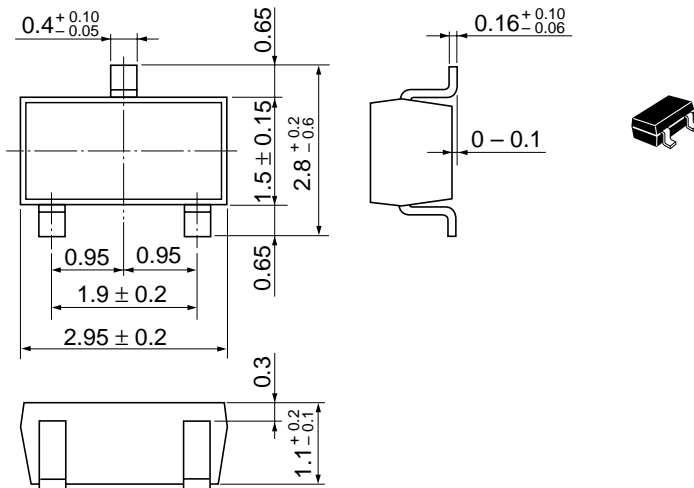


Waveforms



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	MPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.011 g

Cautions

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