PRELIMINARY

8K X 8 CMOS Electrically Erasable PROM

The fully-automatic, 64-byte page-write allows the entire memory to be programmed in less than 0.65 sec. Internal latches, for address and data, free the system bus during the 5ms self-timed, nonvolatile write period. Moreover, the byte-load cycle time matches the read

FEATURES

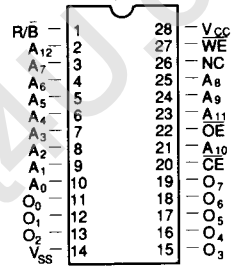
- Fast Read Access Time
  —70ns
- 5 Volt-only Operation
  —Including Write
- Fast Nonvolatile Write Cycle
  —Internally Latched Data and Address
  —70ns Byte-load Cycle
  —5ms Byte-write Cycle
- Automatic Page Write
  —1 to 64 Bytes in a Single High Voltage Cycle
  —Full-chip Rewrite in .65 second
- Software Control Capability
  —Protection Against Nonvolatile Writes
  —5V Chip Erase
  —5V Read of Electronic Signature
- On-chip False Write Protection
- 10,000 Rewrites per Byte
  —High Voltage Applied Only to Updated Bytes

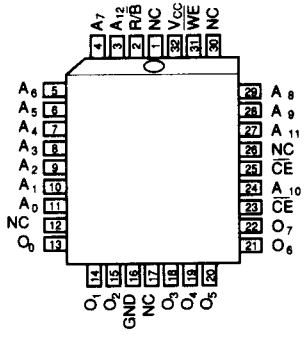
OVERVIEW

The XL28C65A is a full-featured, 8K x 8 bit CMOS E²PROM (Electrically Erasable Programmable Read Only Memory). Operationally, it is compatible with industry standard 64K devices, but it offers improved speed and power efficiency. (Read access times can be as low as 70ns; standby current, less than 100μA). It features a page-wide input buffer and improved protection against inadvertent writes. Most operating modes function from a single 5V power supply, and the XL28C65A is manufactured with EXEL's proven double-metal, 2μ CMOS process.

PIN CONFIGURATION

28 pin DIP; 32 pin LCC



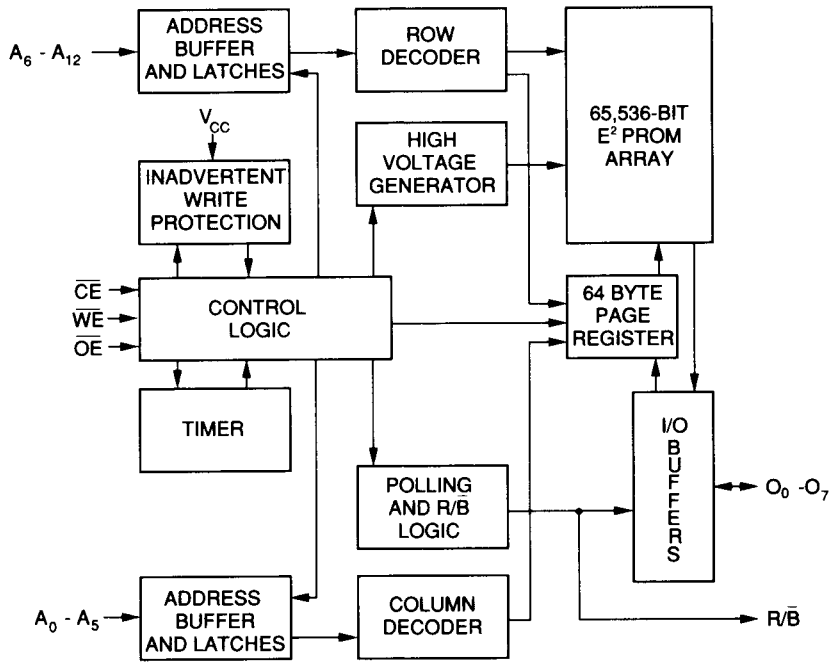


PIN NAMES

R/$\overline{B}$	Ready/$\overline{Busy}$ Indicator
A_0-A_{12}	Address Inputs
O_0-O_7	Data Outputs
$\overline{CE}$	$\overline{Chip}$ Enable
$\overline{OE}$	$\overline{Output}$ Enable
$\overline{WE}$	$\overline{Write}$ Enable
V_{CC}	Supply Voltage
V_{SS}	Power and Signal Ground
NC	No Connect

MEMORY PRODUCTS

BLOCK DIAGRAM



access time, adding to system performance. Three separate status indicators maximize the device's versatility: DATA polling, toggle polling and the R/B pin.

Inadvertent writes are inhibited by a wide range of protections built into the XL28C65A. A low V_{CC} lockout feature disables nonvolatile writes when V_{CC} drops below 4.0V (±5%). Software controlled data protection (not previously available on 64K E²PROMs) utilizes a nonvolatile data-protect bit that enables and disables nonvolatile writes. Additionally, the XL28C65A features power-on reset and noise protected WE.

The XL28C65A is compatible with existing 64K E²PROMs—both pinout and operating modes conform to industry standards. This compatibility extends to higher and lower density E²PROMs as well. The addition of such features as software control does not impact standard modes of operation.

APPLICATIONS

The nonvolatile storage in the XL28C65A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL28C65A is ideal in applications that are self-adapting (such as video games and systems that require automatic re-calibration), as well as those that must tolerate power failures.

ENDURANCE and DATA RETENTION

The XL28C65A is designed for applications requiring up to 10,000 rewrites per E²PROM byte. It provides 10 years of secure data retention, with or without power applied.

DEVICE OPERATION—STANDARD MODES

Three control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$) select all standard, user operating modes for the XL28C65A. Two modes—chip erase and electronic signature read—each require a higher supply voltage on one input pin. (This conforms with existing E²PROM technology.) Software command sequences, described below, provide an alternative, 5V-only, access to these special modes.

Read Mode

Data is read from the XL28C65A by bringing both $\overline{CE}$ and $\overline{OE}$ low while keeping $\overline{WE}$ high. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E²PROM array. Read access time is measured from the latter of: the time when the controlling line goes low ($\overline{CE}$ or $\overline{OE}$), or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle.

Write Mode

The XL28C65A uses a two-step process to store new data. Byte-load cycles fill latches in a volatile page buffer. A subsequent high voltage cycle transfers new entries in the page-buffer to the E²PROM array.

The XL28C65A contains 128 64-byte pages. Address line A_6-A_{12} identify the page; lines A_0-A_5 identify the byte within the page. All bytes written within one write cycle must be on the same page (A_6-A_{12} must remain unchanged). Any number of the 64 bytes in the page can be written or re-written, in any order; the last data written is retained.

Either $\overline{WE}$ or $\overline{CE}$ can be used to trigger the byte-load cycle. The address is latched into internal address latches upon the falling edge of $\overline{WE}$ or $\overline{CE}$ (the other line already being low). A byte-load timer is started on the subsequent rising edge of the controlling line. The timer provides a 100 μS window for initiating the next byte-load cycle. Byte-loading can continue indefinitely if each new load cycle is started within the timeout period.

When the timer times out, additional byte-loads are inhibited and data is automatically transferred from the page buffer to the E²PROM array by a high voltage cycle. Byte flags, set during the byte-load cycles, ensure that high voltage is applied only to newly written bytes. By avoiding the unnecessary cycling of bytes, the endurance of the array is extended. The high voltage cycle is immune to any overlapping control pin activity.

A write-latch is set on the first byte-load of each write cycle. Output pins remain in a high impedance state except during a byte-load (when they contain new input data) or during a status register read (see below). When the high voltage cycle is completed, the write-latch is reset and the operating mode is again determined by the control pins ($\overline{CE}$, $\overline{OE}$ and $\overline{WE}$).

Output Disable Mode

If, while in the read mode, $\overline{OE}$ is brought high, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a high impedance state). When $\overline{WE}$ is brought low, the device enters the write mode regardless of the state of $\overline{OE}$.

Standby Mode

Whenever $\overline{CE}$ is brought high, the device operates in standby mode, with the I/O pins in a high impedance state. Standby power dissipation is less than 100μA with CMOS level inputs. While $\overline{CE}$ remains high, all input pins except $\overline{WE}$ are on standby, insulating the device from activity on the system busses.

MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Address Lines			Data Lines
				A_{12}-A_{10}	A_9	A_8-A_0	
Read	V_{IL}	V_{IL}	V_{IH}	Memory Address			Data Out
Write	V_{IL}	X	V_{IL}	Memory Address			Data In
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	High Z
Standby	V_{IH}	X	X	X	X	X	High Z
Chip Erase	V_{IL}	V_H*	V_{IL}	X	X	X	Data In = X
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	X	V_H*	X	Data Out

* V_H = 12V ± .5V

DEVICE OPERATION—HIGH VOLTAGE MODES

Chip Erase Mode

The chip erase mode allows the entire E²PROM array to be erased with a single command. Chip erase operates like an ordinary write cycle except for the high voltage (11.5V to 12.5V) required on the OE control pin. Chip erase occurs after the first byte-load cycle, but in this case, the data on the I/O pins is ignored. A byte containing all "1s" is automatically written to all locations in the E²PROM array.

Electronic Signature Mode

The electronic signature identifies the manufacturer and the type of the part. It can be read by a standard read operation accompanied by a high voltage (11.5V to 12.5V) on the A_9 pin. A_0 selects one of two 8-bit codes to be output: $A_0 = 0$ returns the manufacturer's ID, $A_0 = 1$ returns the part type. All other address lines are "don't care" during this operation.

DEVICE OPERATION—SOFTWARE CONTROL

Under software control, the XL28C65A offers 5V-only data protect, chip erase and electronic signature modes. Software control is accomplished by byte-load sequences involving specific address and data patterns. Only the high order (page) address lines (A_{12}-A_6) are significant; however, all data lines are utilized.

Short command sequences require three byte-loads; long sequences require six byte-loads. Whenever one of these sequences is recognized in a write operation, it is executed as a software command sequence, and any preceding byte-loads are lost.

These address and data patterns could conceivably occur in a normal application. However, the protocol utilizes differing page addresses within one write cycle—a practice that is illegal in standard write operations.

Electronic Signature

If executed within the timeout period following the second byte-load in a software command sequence, a standard read operation will access the electronic signature. At all other times in a software command sequence, the contents of the status register will be returned, as during a standard write cycle.

Chip Erase Mode

This software command sequence activates the standard chip erase, but without the high voltage input on the $\overline{OE}$ pin. When the byte-loads for the command are complete, all byte flag latches are set. When the byte-load timer expires, a special mass-mode high voltage cycle is performed, erasing the entire E²PROM array. The device then returns to standard read mode.

Software Command Sequence:

Byte-load	A_{12}-A_6	O_7-O_0
1	55 (hex)	AA (hex)
2	2A (hex)	55 (hex)
3	55 (hex)	XX00XXXX (binary)
4	55 (hex)	AA (hex)
5	2A (hex)	55 (hex)
6	55 (hex)	1X01XXXX (binary)

Set Data Protect/Write Mode

This software command sequence disables the high voltage cycle for standard writes (those controlled by the enable lines). Each set data protect command can be followed by data for one page of the E²PROM array. Thereafter, standard writes are disabled, and can be enabled only by a reset data protect command. However, additional pages can be written by the set data protect command.

Software Command Sequence:

Byte-load	A_{12}-A_6	O_7-O_0
1	55 (hex)	AA (hex)
2	2A (hex)	55 (hex)
3	55 (hex)	XX10XXXX (binary)

When this command is recognized, the part remains in write mode. Any number of normal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E²PROM array and setting a nonvolatile data protect bit. If the data protect bit was already set—by a previous set data protect command—it remains set. If a power failure interrupts the operation, neither the data nor the protect bit is written.

Setting the data protect bit inhibits only the high voltage cycles of standard writes (those controlled by the enable lines); byte-load cycles are still accepted. When the byte-load timer expires, the part skips the high voltage cycle and becomes accessible to the standard read mode.

Because the data protect bit is a nonvolatile E^2 element, protect mode status is maintained during power off.

Reset Data Protect/Write Mode

This software command sequence re-enables the high voltage cycle of the standard write. Each reset data protect command can be accompanied by data for one page of the E^2PROM. Standard writes are then enabled, until disabled by a subsequent set data protect command.

Software Command Sequence:

Byte-load	A_{12}-A_6	O_7-O_0
1	55 (hex)	AA (hex)
2	2A (hex)	55 (hex)
3	55 (hex)	XX00XXXX (binary)
4	55 (hex)	AA (hex)
5	2A (hex)	55 (hex)
6	55 (hex)	XX10XXXX (binary)

The six byte-loads specifying this command leave the part in write mode: any number of nomal byte-load cycles can be performed in the same write cycle. When the byte-load timer expires, a normal high voltage cycle occurs, writing the page buffer data to the E^2PROM array and resetting the nonvolatile data protect bit. If the data protect bit was already reset (by a previous reset data protect command), it remains set. If a power failure interrupts the operation, neither the data nor the protect bit is written.

For normal, hardware-controlled writes, the data protect bit inhibits only the high voltage cycles; byte-load cycles are accepted. When the byte-load timer expires, the part skips the high voltage cycle and reverts to read mode.

Because the data protect bit is a nonvolatile E^2 element, protect mode status is maintained during power off.

MONITORING DEVICE STATUS

Because the byte-load timer and its high voltage cycle are completely under the control of the XL28C65A, a status register and READY/$\overline{\text{BUSY}}$ pin allow the host system to monitor device status.

Status Register

Any read performed while the write-latch is set is interpreted as a status register read. (Reading the status register has no effect on the byte-load timer, byte-load flags, high voltage cycle or the contents of the page buffer.)

The status of a write operation is monitored in one of two ways: Toggle Polling or $\overline{\text{DATA}}$ Polling. While the write-latch is set, O_6 will toggle between 0 and 1 on successive reads; O_7 will hold the complement of bit 7 of the last byte loaded. When the write-latch is reset, the write operation is complete. O_6 and O_7 become bits 6 and 7 of the actual byte location. Bit 6 will no longer toggle; bit 7 will no longer be a complement.

While the write cycle is in progress, there is additional information available from the status register, as follows:

Bits 0 and 1: Reserved for use by factory
Bit 2: Always 0
Bit 3: 1 means data protect feature is enabled
0 means data protect feature is disabled
Bit 4: Always 1
Bit 5: Reserved for use by factory
Bit 6: Used in Toggle polling
Bit 7: Used in $\overline{\text{DATA}}$ polling

Ready/$\overline{\text{Busy}}$ Pin

The R/$\overline{\text{B}}$ pin (Pin 1) is a dedicated device status indicator. During device operation, it remains at a logic '1' except when the XL28C65A is internally occupied with a nonvolatile write cycle, or when the supply voltage is below 4.0V (see Low V_{CC} Lockout).

When a write cycle is initiated, R/$\overline{\text{B}}$ is brought to a logic '0'. It returns to a logic '1' when the corresponding high voltage cycle is completed. R/$\overline{\text{B}}$ can be polled to determine write cycle status, or it can be used to initiate an interrupt to the controller.

This output line is configured as an open-drain driver, allowing R/$\overline{\text{B}}$ outputs from two or more XL28C65As to be OR-tied. Consequently, it requires an appropriate pull-up resistor. (See Figure 1.) For either CMOS or TTL logic, a good starting value for this resistor is 2.2K ohms. A higher value can be used to save power in CMOS applications.

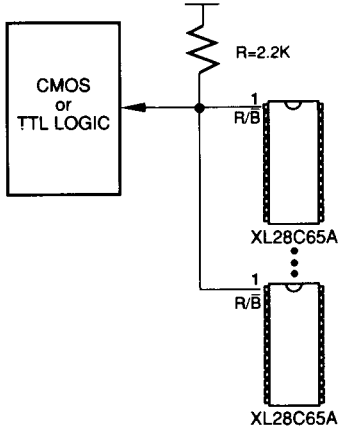


Figure 1. OR-Tied R/$\overline{\text{B}}$ Pins

WRITE PROTECT MECHANISMS

The XL28C65A features several mechanisms to protect it from inadvertent writes that might occur during power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following are built in.

Power on Reset

At power on, operation is inhibited until V_{CC} is stable and sufficiently high. All modes are disabled until V_{CC} reaches 3.0 to 3.5V. Read operations are enabled as soon as V_{CC} is adequate; write operations are enabled 1ms later.

Low V_{CC} Lockout

High voltage cycles are automatically disabled whenever V_{CC} drops below 4V (±5%). (Byte-load cycles are not directly affected: the V_{CC} sensor is sampled when the byte-load timer expires.) If V_{CC} is below threshold, the part skips the high voltage cycle and will operate only in read mode. All attempts to write the E²PROM array are locked out until V_{CC} reaches the required voltage. R/$\overline{\text{B}}$ outputs V_{IL} while V_{CC} is below threshold (and above 1.0V).

Noise Protection

Write pulses of less than 10ns duration on the $\overline{\text{WE}}$ pin will not set the write-latch.

MAXIMUM RATINGS

Temperature under bias..... -65 to +135°C
Storage temperature..... -65 to +150°C
Voltage on any pin*..... -1.0 to +7.0V
Voltage on $\overline{OE}$ pin*..... -1.0 to +22.0V
DC output current..... 5 mA

* With respect to ground

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to avoid any voltages higher than the rated maxima.

D.C. CHARACTERISTICS

TA = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Max	Units	Test Conditions
I_{CC}	V_{CC} Current – Active		30+ 5/MHz	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} $\overline{WE}$ = V_{IH} I/O's = open AO-A12 toggling
I_{SB}	V_{CC} Current–Standby		2	mA	$\overline{CE}$ = $\overline{WE}$ = V_{IH} $\overline{OE}$ = V_{IL} I/O's = open A_0 -A_{12} = V_{CC}
I_{SBC}	V_{CC} Current– CMOS Standby		100	uA	$\overline{CE}$ = $\overline{WE}$ >= V_{CC}-.2 $\overline{OE}$ = V_{IL} I/O's = open A_0 -A_{12} = V_{CC}
I_{LI}	Input Leakage Current		10	uA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	uA	V_{OUT} = GND to V_{CC} $\overline{CE}$ = V_{IH}
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL}= 2.1 mA
V_{OH}	Output High Voltage	2.4 V_{CC}-0.1		V V	I_{OH} = -400 uA I_{OH} = -10 uA

CAPACITANCE

TA = +25°C, f = 1.0 MHz,

Symbol	Test	Max.	Units	Test Conditions
$C_{I/O}$	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V

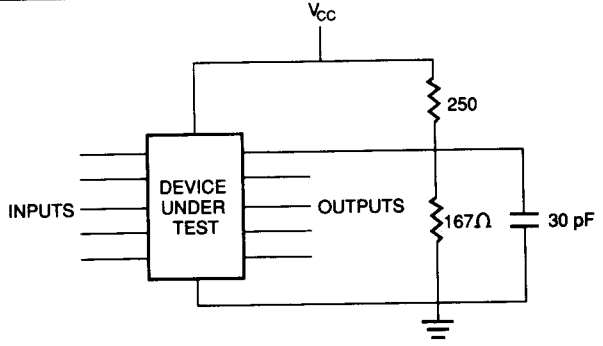
AC OPERATING CHARACTERISTICS

READ CYCLE (See Figures 2&3)

Symbol	Parameter	Min	Max	Units
t_{RC}	Read Cycle Time	70		nS
t_{AA}	Address Access Time		90	nS
t_{CE}	Chip Enable Access Time		90	nS
t_{OE}	Output Enable Access Time		40	nS
t_{LZ}	Chip Enable to Output in Low Z	5		nS
t_{HZ}	Chip Disable to Output in High Z	5	35	nS
t_{OLZ}	Output Enable to Output in Low Z	5		nS
t_{OHZ}	Output Disable to Output inHigh Z	5	35	nS
t_{OH}	Output Hold from Address Change	15		nS

WRITE CYCLE (See Figures 4, 5, 6)

Symbol	Parameter	Min	Max	Units
t_{WC}	Write Cycle Time		5	mS
t_{BLC}	Byte Load Cycle	1	100	μS
t_{BLT}	Byte Load Time		100	μS
t_{AS}	Address Setup Time	0		nS
t_{AH}	Address Hold Time	35		nS
t_{CS}	Write Setup Time	0		nS
t_{CH}	Write Hold Time	0		nS
t_{CP}	Chip Enable Pulse Width	50		nS
t_{OES}	Output Enable Setup Time	5		nS
t_{OEH}	Output Enable Hold Time	5		nS
t_{WP}	Write Enable Pulse Width	60		nS
t_{WPH}	Write Pulse Width High	60		nS
t_{DS}	Data Setup Time	30		nS
t_{DH}	Data Hold Time	0		nS
t_{BWR}	Busy to Write Recovery Time	50		nS
t_{BP}	$\overline{CE}$ and $\overline{WE}$ Low to R/$\overline{B}$ Low		150	nS



Input Signal Amplitude	0V to 3V
Input Rise and Fall Times	5ns from 1V to 2V
Frequency	10 MHz
Timing Reference Value	1.5V

Figure 2. AC Test Conditions

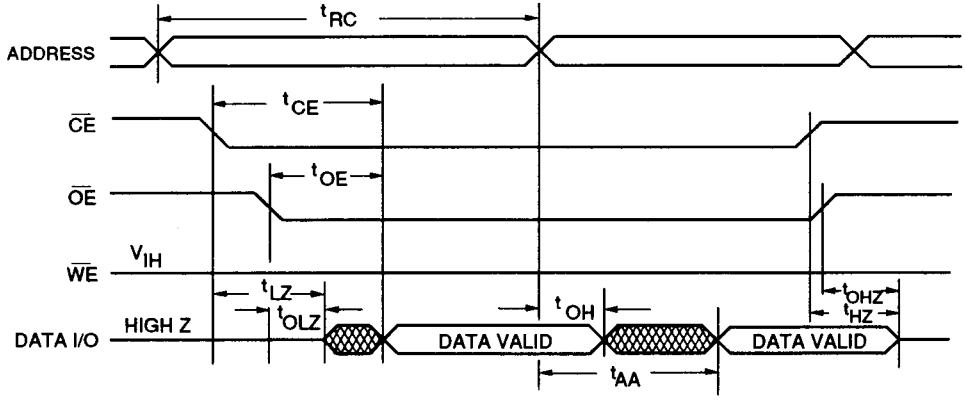


Figure 3. Read Cycle Timing

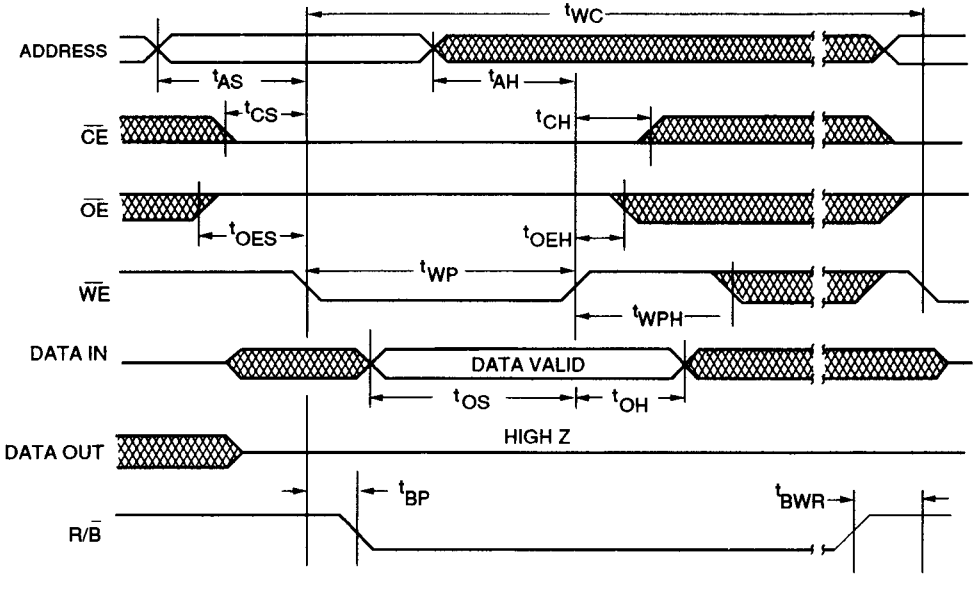


Figure 4. $\overline{WE}$ Controlled Write Cycle Timing

MEMORY PRODUCTS

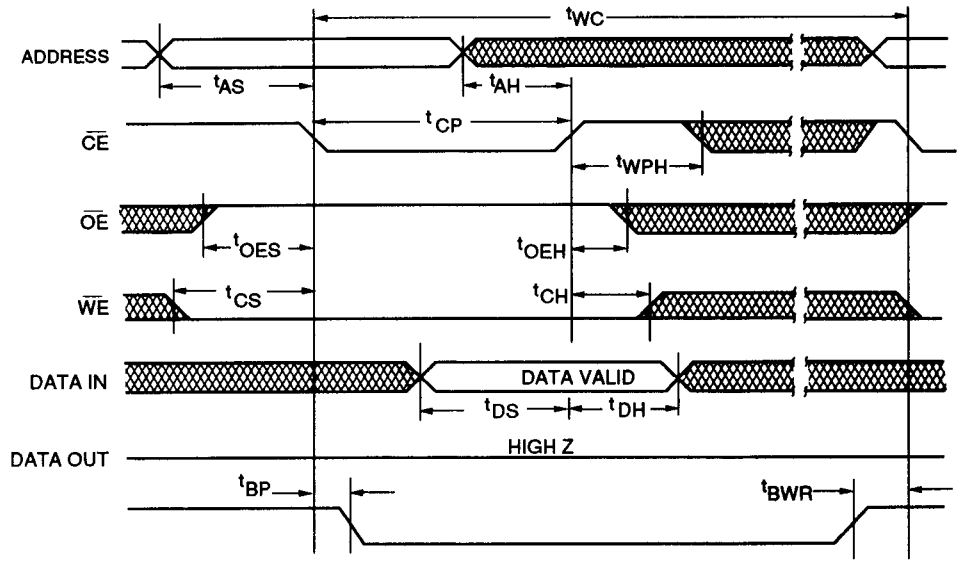


Figure 5. $\overline{CE}$ Controlled Write Cycle Timing (Single Byte Load)

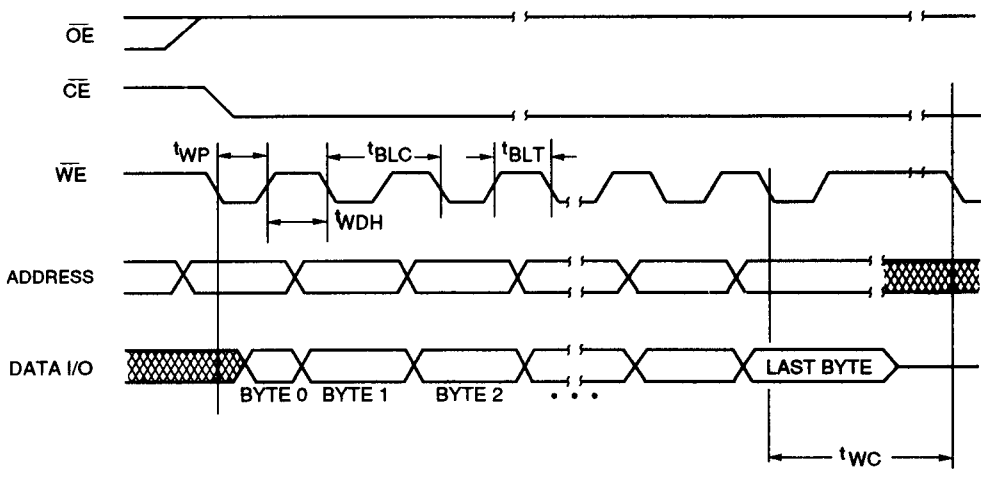


Figure 6. Page Mode Write Cycle Timing ($\overline{WE}$ Controlled)

ORDERING INFORMATION

Standard Configurations:

Prefix	Temperature Range	Part Type	Package* Type	Access Time ns
XL	S	28C65A	C, D, P	70, 90, 110
XL	E	28C65A	C, D, P	70, 90, 110
XL	M	28C65A	C	90, 110, 130

*Contact EXEL for your special packaging requirements

Part Numbers: