

DATA SHEET

TDA3608Q

Multiple voltage regulator with
switch

Preliminary specification
File under Integrated Circuits, IC01

1997 Aug 14

Multiple voltage regulator with switch

TDA3608Q

FEATURES

General

- Two V_P -state controlled regulators (regulator 1 and 3) and a power switch
- Regulator 2 and reset operate during load dump and thermal shutdown
- Separate control pins for switching regulator 1, regulator 3 and the power switch
- Supply voltage range of -18 to $+50$ V
- Low reverse current of regulator 2
- Low quiescent current (when regulator 1, regulator 3, and power switch are switched off)
- Hold output (only valid when regulator 1 is switched on)
- Reset and hold outputs (open collector outputs)
- Adjustable reset delay time
- High ripple rejection
- Back-up capacitor for regulator 2.

Protections

- Reverse polarity safe (down to -18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short-circuited)
- ESD protected on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulators 1, 2 and 3
- Delayed second current limit protection for the power switch (at short-circuit)
- The regulator outputs and the power switch are DC short-circuited safe to ground and V_P .

GENERAL DESCRIPTION

The TDA3608Q is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. It contains:

- Two fixed voltage regulators with a foldback current protection (regulator 1 and regulator 3) and one fixed voltage regulator (regulator 2), intended to supply a microcontroller, that also operates during load dump and thermal shutdown.
- A power switch with protections, operated by an enable input
- Reset and hold outputs that can be used to interface by the microcontroller. The reset signal can be used to call up the microcontroller and the hold output indicates regulator 1 voltage available and within range.
- A supply pin which can withstand load dump pulses and negative supply voltages
- Regulator 2 that will be switched on at a back-up voltage higher than 6.5 V and off when the output voltage of regulator 2 drops below 1.9 V
- A provision for use of a reserve supply capacitor that will hold enough energy for regulator 2 (5 V continuous) to allow a microcontroller to prepare for loss of voltage.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA3608Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

Multiple voltage regulator with switch

TDA3608Q

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage operating		9.5	14.4	18	V
	reverse polarity	non-operating	–	–	–18	V
	regulator 2 on		2.4	14.4	50	V
	jump start	$t \leq 10$ minutes	–	–	30	V
	load dump protection	$t \leq 50$ ms; $t_r \geq 2.5$ ms	–	–	50	V
$I_{q(\text{tot})}$	total quiescent supply current	standby mode	–	500	600	μA
T_j	junction temperature		–	–	150	$^{\circ}\text{C}$
Voltage regulators						
$V_{O(\text{REG}1)}$	output voltage regulator 1	$1 \text{ mA} \leq I_{\text{REG}1} \leq 600 \text{ mA}$	8.15	8.5	8.85	V
$V_{O(\text{REG}2)}$	output voltage regulator 2	$0.5 \text{ mA} \leq I_{\text{REG}2} \leq 300 \text{ mA}$; $V_P = 14.4 \text{ V}$	4.75	5.0	5.25	V
$V_{O(\text{REG}3)}$	output voltage regulator 3	$1 \text{ mA} \leq I_{\text{REG}3} \leq 400 \text{ mA}$	4.75	5.0	5.25	V
Power switch						
V_d	drop-out voltage	$I_{\text{SW}} = 1 \text{ A}$	–	0.45	0.7	V
		$I_{\text{SW}} = 1.8 \text{ A}$	–	1	1.8	V
I_M	peak current		3	–	–	A

Multiple voltage regulator with switch

TDA3608Q

BLOCK DIAGRAM

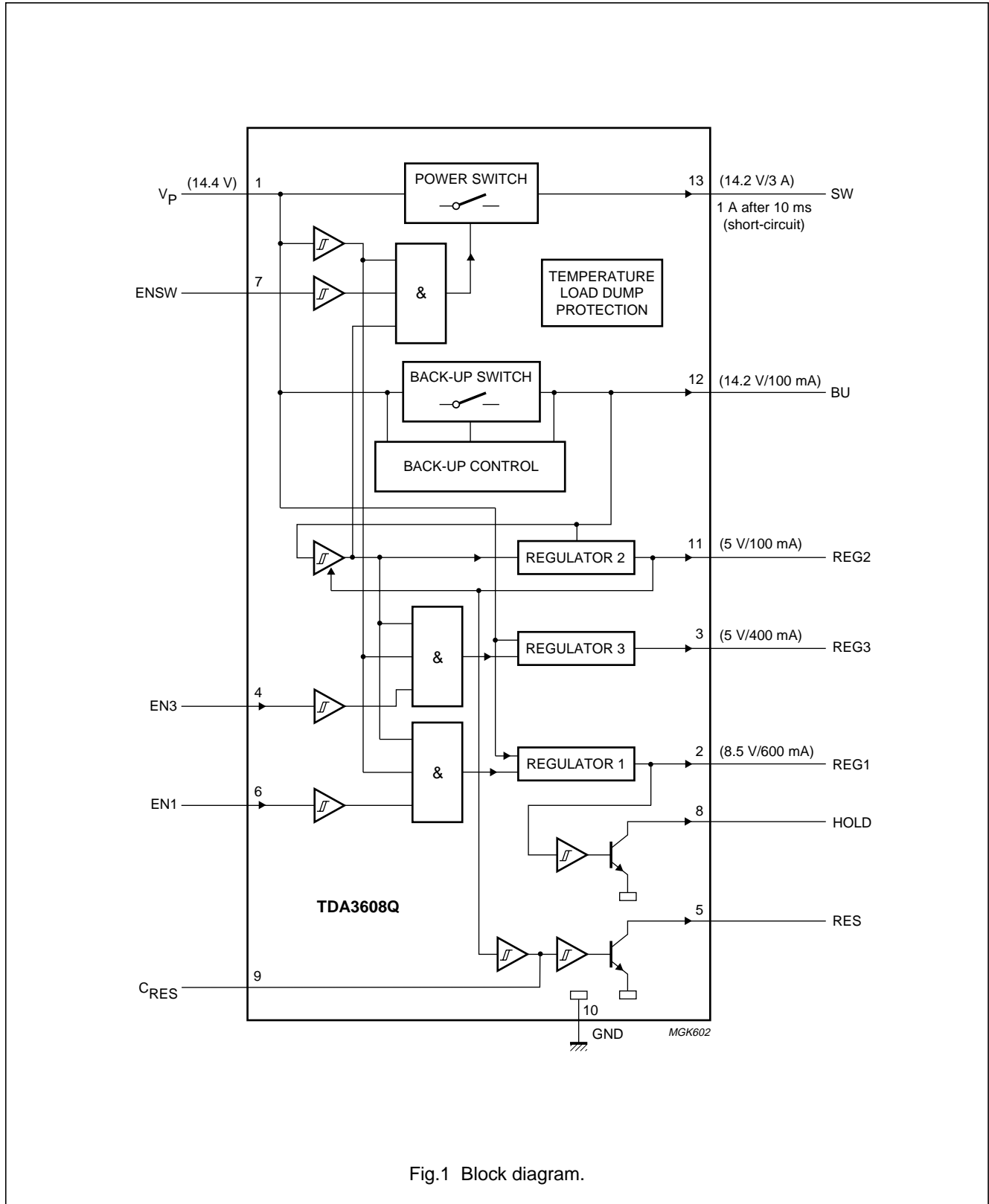


Fig.1 Block diagram.

Multiple voltage regulator with switch

TDA3608Q

PINNING

SYMBOL	PIN	DESCRIPTION
V _P	1	supply voltage
REG1	2	regulator 1 output
REG3	3	regulator 3 output
EN3	4	enable input regulator 3
RES	5	reset output
EN1	6	enable input regulator 1
ENSW	7	enable input power switch
HOLD	8	hold output
C _{RES}	9	reset delay capacitor
GND	10	ground
REG2	11	regulator 2 output
BU	12	back-up
SW	13	power switch output

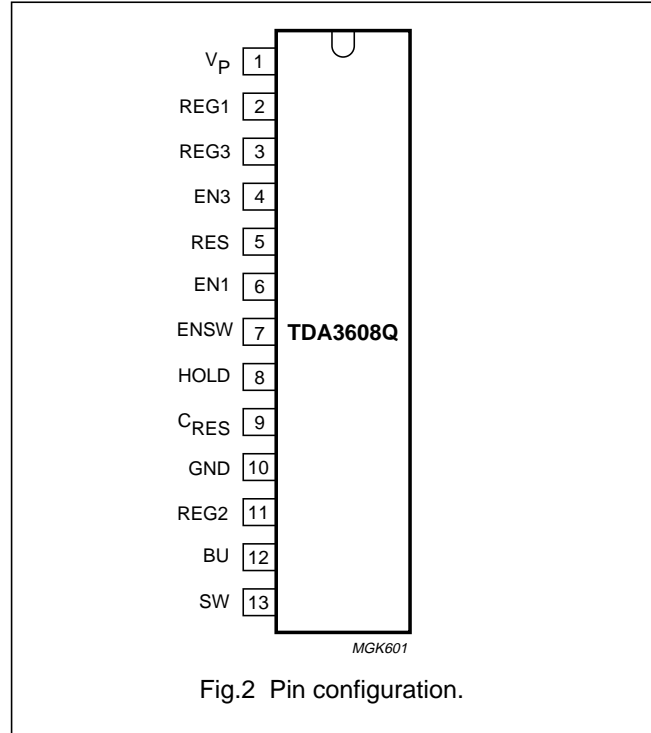


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA3608Q is a multiple output voltage regulator with a power switch, intended for use in car radios with or without a microcontroller. Because of low-voltage operation of the car radio, low-voltage drop regulators are used in the TDA3608Q.

Regulator 2 will switch on when the back-up voltage exceeds 6.5 V for the first time and will switch off again when the output voltage of regulator 2 drops below 1.9 V (this is far below an engine start). When regulator 2 is switched on and the output voltage of this regulator is within its voltage range, the reset output will be enabled (reset will go HIGH via a pull-up resistor) to generate a reset to the microcontroller. The reset cycles can be extended by an external capacitor at pin 9. The above mentioned start-up feature is built-in to secure a smooth start-up of the microcontroller at first connection, without uncontrolled switching of regulator 2 during the start-up sequence.

The charge of the back-up capacitor can be used to supply regulator 2 for a short period when the supply falls down to 0 V (time depends on value of storage capacitor). When regulator 2 and the supply voltage (V_P > 4.5 V) are both available, regulators 1 and 3 can be operated by means of enable inputs (pins 6 and 4 respectively).

Regulator 1 has a hold output (open collector) indicating that the output voltage of this regulator is settled (held HIGH by external pull-up resistor) and when the output voltage of this regulator drops out of regulation (because of supply voltage drop or high load) the hold output will go LOW. The hold output signal is only valid when regulator 1 is enabled by its enable input (pin 6).

The power switch can also be controlled by means of a separate enable input (pin 7) as shown in Fig.3 for the behaviour of the power switch output.

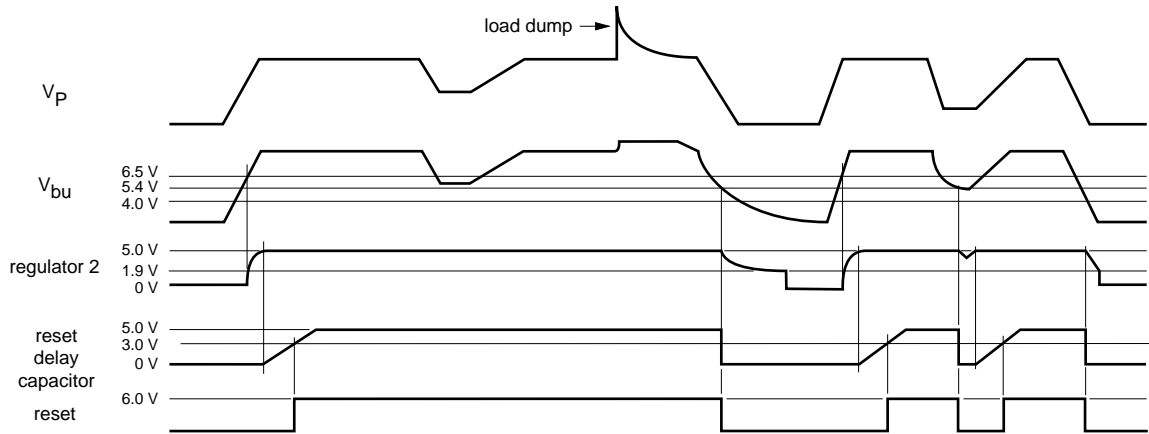
All output pins are fully protected. The regulators are protected against load dump (regulators 1 and 3 will switch off at supply voltages >18 V) and short-circuit (foldback current protection).

The power switch contains a current protection, but this protection is delayed at short-circuit condition for at least 10 ms. During this time the output current is limited to a peak value of at least 3 A and 2 A continuous (V_P ≤ 18 V). At supply voltages >17 V the power switch is clamped at maximum 16 V (to avoid external connected circuitry being damaged by an overvoltage) and the power switch will switch off at load dump.

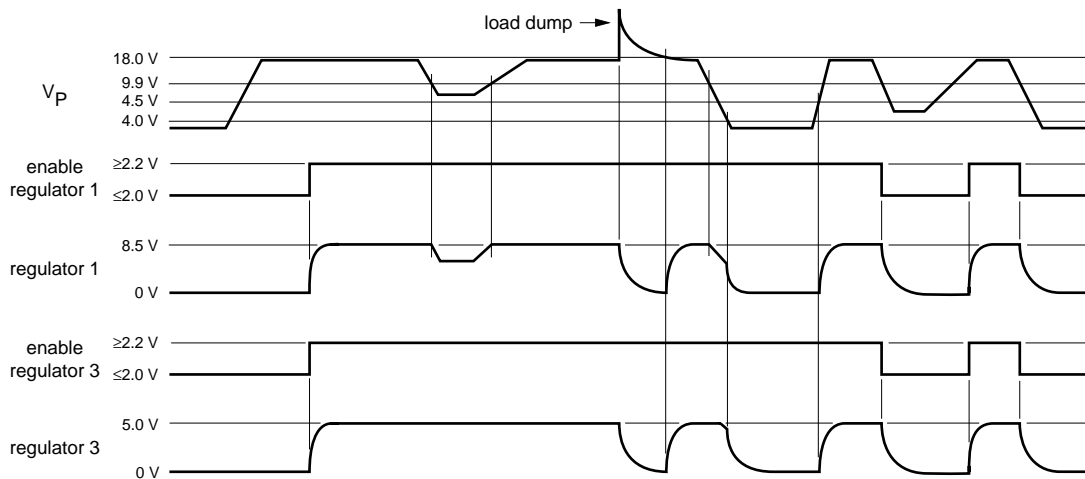
The total timing diagram is shown in Fig.3.

Multiple voltage regulator with switch

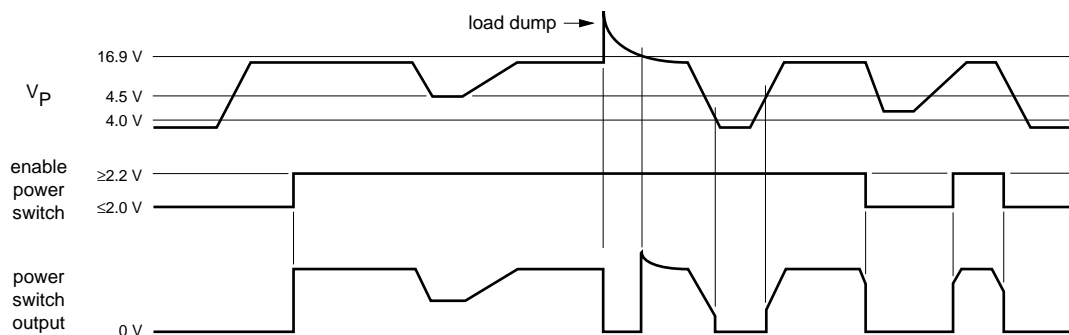
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Back-up Schmitt trigger and reset behaviour



V_P and enable Schmitt trigger



Power switch behaviour

MGK603

Fig.3 Timing diagrams.

Multiple voltage regulator with switch

TDA3608Q

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _P	supply voltage				
	operating		–	18	V
	reverse polarity	non-operating	–	–18	V
	jump start	t ≤ 10 minutes	–	30	V
	load dump protection	t ≤ 50 ms; t _r ≥ 2.5 ms	–	50	V
P _{tot}	total power dissipation		–	62	W
T _{stg}	storage temperature	non-operating	–55	+150	°C
T _{amb}	ambient temperature	operating	–40	+85	°C
T _j	junction temperature	operating	–40	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th(j-c)}	thermal resistance from junction to case		2	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	50	K/W

Multiple voltage regulator with switch

TDA3608Q

CHARACTERISTICS

$V_P = 14.4\text{ V}$; $T_{\text{amb}} = 25\text{ °C}$; see Fig.6; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage		9.5	14.4	18	V
	operating regulator 2 on	note 1	2.4	14.4	18	V
	jump start	$t \leq 10\text{ minutes}$	–	–	30	V
	load dump protection	$t \leq 50\text{ ms}$; $t_r \geq 2.5\text{ ms}$	–	–	50	V
I_q	quiescent supply current	$V_P = 12.4\text{ V}$; note 2; $I_{\text{REG2}} = 0.1\text{ mA}$	–	500	600	μA
		$V_P = 14.4\text{ V}$; note 2; $I_{\text{REG2}} = 0.1\text{ mA}$	–	520	–	μA
Schmitt trigger power supply for regulator 1, regulator 3 and power switch						
V_{thr}	rising threshold voltage		4.0	4.5	5.0	V
V_{thf}	falling threshold voltage		3.5	4.0	4.5	V
V_{hys}	hysteresis voltage		–	0.5	–	V
Schmitt trigger for regulator 2						
V_{thr}	rising threshold voltage		6.0	6.5	7.1	V
V_{thf}	falling threshold voltage		1.7	1.9	2.2	V
V_{hys}	hysteresis voltage		–	4.6	–	V
Schmitt trigger for enable input (regulator 1, regulator 3 and power switch)						
V_{thr}	rising threshold voltage		1.7	2.2	2.7	V
V_{thf}	falling threshold voltage		1.5	2.0	2.5	V
V_{hys}	hysteresis voltage	$I_{\text{REG}} = I_{\text{SW}} = 1\text{ mA}$	0.1	0.2	0.5	V
I_{LI}	input leakage current	$V_{\text{EN}} = 5\text{ V}$	1	5	10	μA
Schmitt trigger for reset						
V_{thr}	rising threshold voltage of regulator 2	V_P rising; $I_{\text{REG1}} = 50\text{ mA}$; note 3	–	$V_{\text{REG2}} - 0.15$	$V_{\text{REG2}} - 0.075$	V
V_{thf}	falling threshold voltage of regulator 2	V_P rising; $I_{\text{REG1}} = 50\text{ mA}$; note 3	4.3	$V_{\text{REG2}} - 0.35$	–	V
V_{hys}	hysteresis voltage		0.1	0.2	0.3	V
Schmitt trigger for hold						
V_{thr}	rising threshold voltage of regulator 1	V_P rising; note 3	–	$V_{\text{REG1}} - 0.15$	$V_{\text{REG1}} - 0.075$	V
V_{thf}	falling threshold voltage of regulator 1	V_P rising; note 3	9.2	$V_{\text{REG1}} - 0.35$	–	V
V_{hys}	hysteresis voltage		0.1	0.2	0.3	V

Multiple voltage regulator with switch

TDA3608Q

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reset and hold buffer						
I_{sinkL}	LOW-level sink current	$V_{\text{RES/HOLD}} \leq 0.8 \text{ V}$	2	–	–	mA
I_{LO}	output leakage current	$V_{\text{P}} = 14.4 \text{ V}; V_{\text{RES/HOLD}} = 5 \text{ V}$	–	–	2	μA
t_{r}	rise time	note 4	–	7	50	μs
t_{f}	fall time	note 4	–	1	50	μs
Reset delay						
I_{ch}	charge current		2	4	8	μA
I_{dch}	discharge current		500	800	–	μA
V_{thr}	rising threshold voltage		2.5	3.0	3.5	V
t_{d}	delay time	$C = 47 \text{ nF};$ note 5	20	35	70	ms
Regulator 1 ($I_{\text{REG1}} = 5 \text{ mA}$ unless otherwise specified)						
$V_{\text{O(off)}}$	output voltage off		–	1	400	mV
V_{O}	output voltage	$1 \text{ mA} \leq I_{\text{REG1}} \leq 600 \text{ mA}$	8.15	8.5	8.85	V
		$11 \text{ V} \leq V_{\text{P}} \leq 18 \text{ V}$	8.15	8.5	8.85	V
ΔV	line regulation	$11 \text{ V} \leq V_{\text{P}} \leq 18 \text{ V}$	–	2	75	mV
ΔV_{L}	load regulation	$1 \text{ mA} \leq I_{\text{REG1}} \leq 600 \text{ mA}$	–	20	50	mV
I_{q}	quiescent current	$I_{\text{REG1}} = 600 \text{ mA}$	–	25	60	mA
SVRR	supply voltage ripple rejection	$f_{\text{i}} = 3 \text{ kHz}; V_{\text{i(p-p)}} = 2 \text{ V}$	60	70	–	dB
V_{d}	drop-out voltage	$I_{\text{REG1}} = 550 \text{ mA}; V_{\text{P}} = 8.5 \text{ V};$ note 6	–	0.4	0.7	V
I_{m}	current limit	$V_{\text{REG1}} > 7.5 \text{ V};$ note 7	0.65	1.2	–	A
I_{sc}	short-circuit current	$R_{\text{L}} \leq 0.5 \Omega;$ note 8	250	800	–	mA
Regulator 2 ($I_{\text{REG2}} = 5 \text{ mA}$ unless otherwise specified)						
V_{O}	output voltage	$0.5 \text{ mA} \leq I_{\text{REG2}} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
		$I_{\text{REG2}} = 300 \text{ mA};$ note 9	4.75	5.0	5.25	V
		$7 \text{ V} \leq V_{\text{P}} \leq 18 \text{ V}$	4.75	5.0	5.25	V
		$18 \text{ V} \leq V_{\text{P}} \leq 50 \text{ V};$ $I_{\text{REG2}} \leq 150 \text{ mA}$	4.75	5.0	5.25	V
ΔV	line regulation	$6 \text{ V} \leq V_{\text{P}} \leq 18 \text{ V}$	–	2	50	mV
		$18 \text{ V} \leq V_{\text{P}} \leq 50 \text{ V}$	–	15	75	mV
ΔV_{L}	load regulation	$1 \text{ mA} \leq I_{\text{REG2}} \leq 150 \text{ mA}$	–	20	50	mV
		$1 \text{ mA} \leq I_{\text{REG2}} \leq 300 \text{ mA}$	–	–	100	mV
SVRR	supply voltage ripple rejection	$f_{\text{i}} = 3 \text{ kHz}; V_{\text{i(p-p)}} = 2 \text{ V}$	60	70	–	dB

Multiple voltage regulator with switch

TDA3608Q

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _d	drop-out voltage	I _{REG2} = 100 mA; V _P = 4.75 V; note 6	–	0.4	0.6	V
		I _{REG2} = 200 mA; V _P = 5.75 V; note 6	–	0.8	1.2	V
		I _{REG2} = 100 mA; V _{BU} = 4.75 V; note 10	–	0.2	0.5	V
		I _{REG2} = 200 mA; V _{BU} = 5.75 V; note 10	–	0.8	1.0	V
I _m	current limit	V _{REG2} > 4.5 V; note 7	0.32	0.37	–	A
I _{sc}	short-circuit current	R _L ≤ 0.5 Ω; note 8	20	100	–	mA
Regulator 3 (I_{REG3} = 5 mA unless otherwise specified)						
V _{O(off)}	output voltage off		–	1	400	mV
V _O	output voltage	1 mA ≤ I _{REG3} ≤ 400 mA	4.75	5.0	5.25	V
		7 V ≤ V _P ≤ 18 V	4.75	5.0	5.25	V
ΔV	line regulation	7 V ≤ V _P ≤ 18 V	–	2	50	mV
ΔV _L	load regulation	1 mA ≤ I _{REG3} ≤ 400 mA	–	20	50	mV
I _q	quiescent current	I _{REG3} = 400 mA	–	15	40	mA
SVRR	supply voltage ripple rejection	f _i = 3 kHz; V _{i(p-p)} = 2 V	60	70	–	dB
V _d	drop-out voltage	I _{REG3} = 400 mA; V _P = 5.75 V; note 6	–	1	1.5	V
I _m	current limit	V _{REG3} > 4.5 V; note 7	0.45	0.70	–	A
I _{sc}	short-circuit current	R _L ≤ 0.5 Ω; note 8	100	400	–	mA
Power switch						
V _d	drop-out voltage	I _{SW} = 1 A; note 11	–	0.45	0.7	V
		I _{SW} = 1.8 A; note 11	–	1.0	1.8	V
I _{dc}	continuous current	V _P = 16 V, V _{SW} = 13.5 V	1.8	2.0	–	A
V _{cl}	clamping voltage	V _P ≥ 17 V	13.5	15.0	16.0	V
I _M	peak current	V _P = 17 V; notes 12 and 13	3	–	–	A
V _{fb}	fly back voltage behaviour	I _{SW} = –100 mA	–	V _P + 3	22	V
I _{sc}	short-circuit current	V _P = 14.4 V; V _{SW} < 1.2 V; note 13	–	0.8	–	A
Back-up switch						
I _{dc}	continuous current		0.3	0.35	–	A
V _{cl}	clamping voltage	V _P ≥ 16.7 V	–	–	16	V
I _r	reverse current	V _P = 0; V _{BU} = 12.4 V; note 14	–	–	900	mA

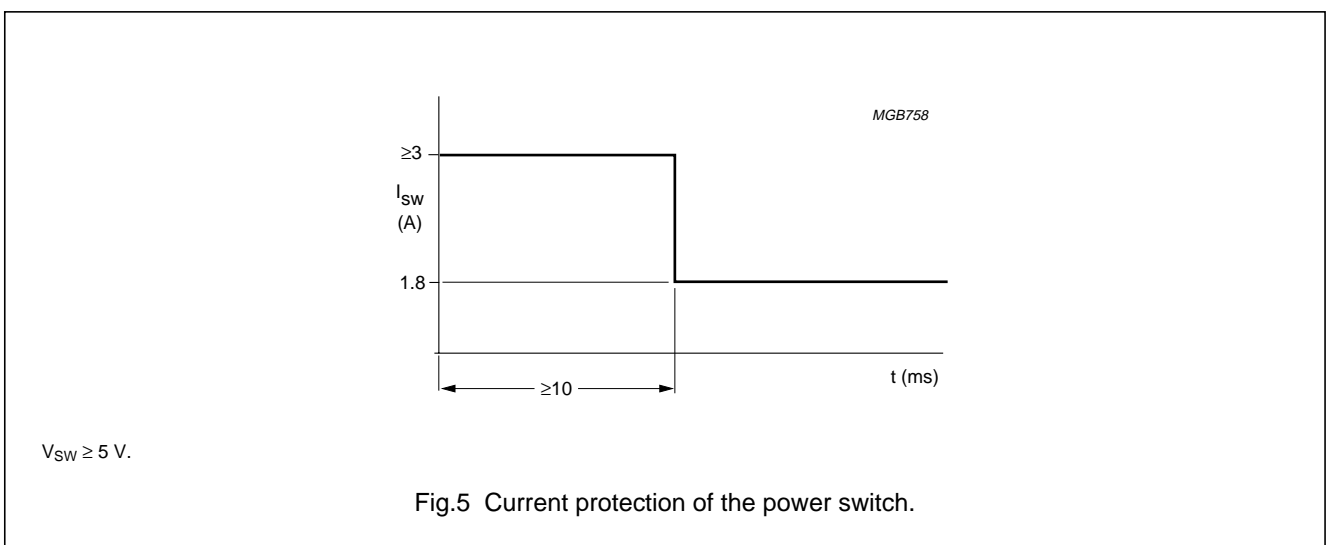
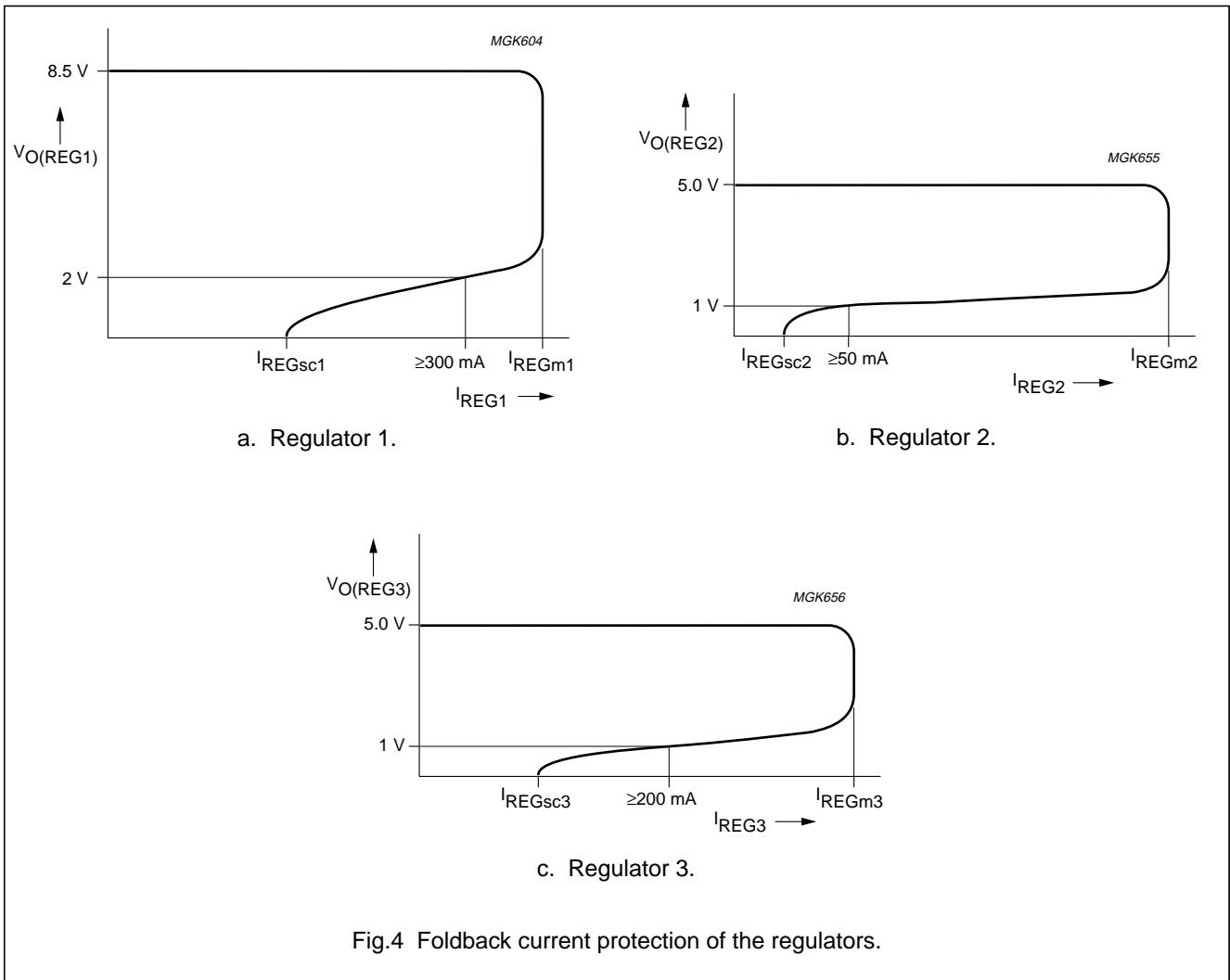
Multiple voltage regulator with switch**TDA3608Q**

Notes

1. Minimum operating voltage, only if V_P has exceeded 6.5 V.
2. The quiescent current is measured in the standby mode. So, the enable inputs of regulators 1, 3 and the switch are grounded and $R_{L(REG2)} = \infty$ (see Fig.6).
3. The voltage of the regulator sinks as a result of a V_P drop.
4. The rise and fall time is measured with a 10 k Ω pull-up resistor and a 50 pF load capacitor.
5. The delay time depends on the value of the capacitor: $t_d = \frac{C}{I_{ch}} \times V_{C(th)} = C \times (750 \times 10^3)$ (ms)
6. The drop-out voltage of regulators 1, 2 and 3 is measured between V_P and REGn.
7. At current limit, I_{REGmn} is held constant (see Fig.4 for behaviour of I_{REGmn}).
8. The foldback current protection limits the dissipated power at short-circuit (see Fig.4).
9. The peak current of 300 mA can only be applied for short periods ($t < 100$ ms).
10. The drop-out voltage measured between BU and REG2.
11. The drop-out voltage of the power switch is measured between V_P and SW.
12. The maximum output current of the power switch is limited to 1.8 A when the supply voltage exceeds 18 V.
13. At short-circuit, I_{sc} of the power switch is held constant to a lower value than the continuous current after a delay of at least 10 ms (see Fig.5).
14. The reverse current of the back-up switch is measured when flowing out of pin V_P with $V_P = 0$ V.

Multiple voltage regulator with switch

TDA3608Q

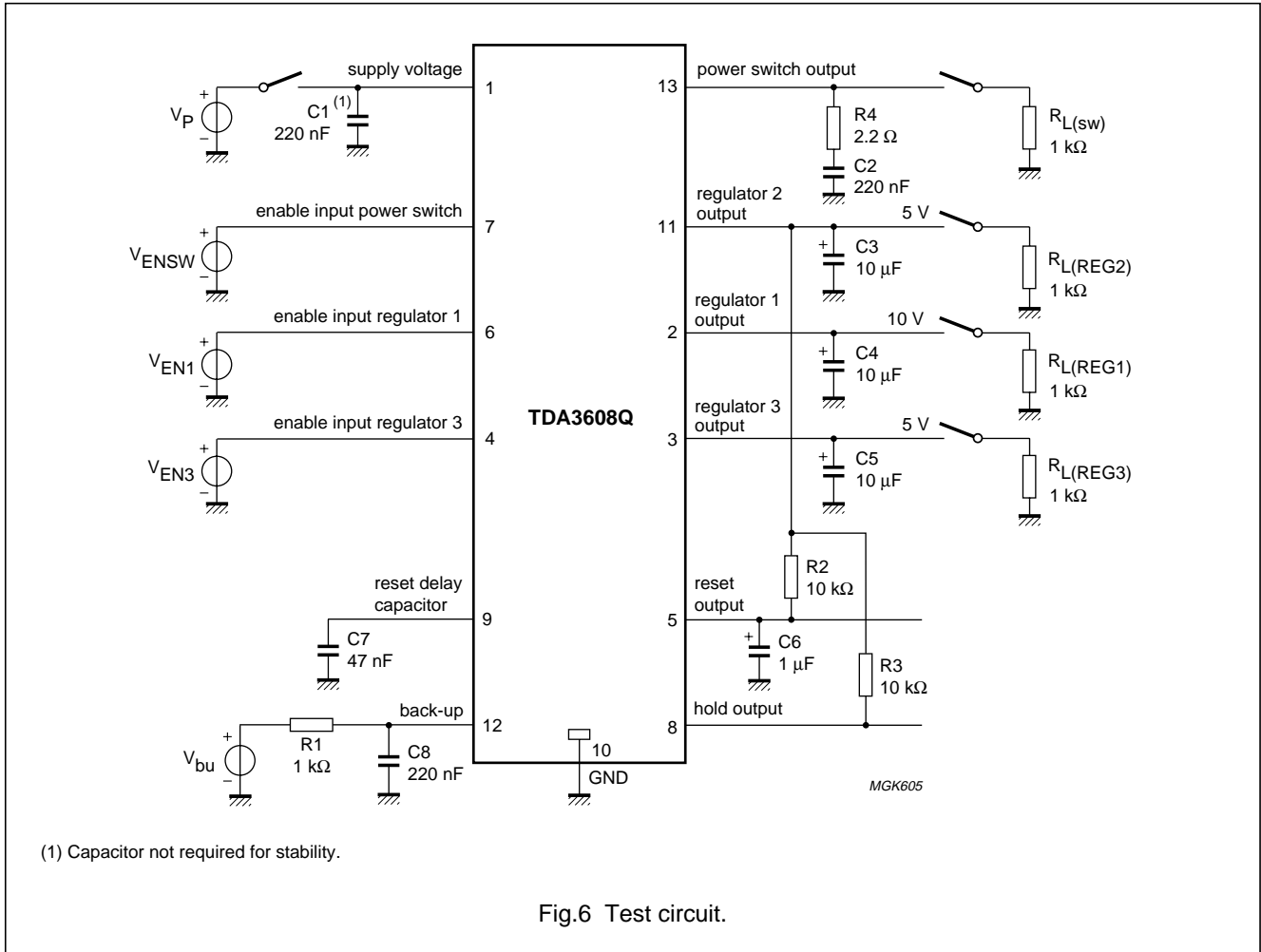


Multiple voltage regulator with switch

TDA3608Q

TEST AND APPLICATION INFORMATION

Test information



Application information

NOISE

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (output noise of the regulators is translated into a current noise by means of the output capacitors). Table 1 shows the noise figure with the corresponding output capacitor for each regulator. The noise is minimal when a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 μF is connected directly to pins V_P and GND.

Table 1 Noise figures

REGULATOR	NOISE FIGURE ⁽¹⁾		
	C _O = 10 μF	C _O = 47 μF	C _O = 100 μF
1	225 μV	150 μV	135 μV
2	225 μV	150 μV	135 μV
3	255 μV	200 μV	180 μV

Note

1. Measured at a bandwidth of 200 kHz.

Multiple voltage regulator with switch

TDA3608Q

STABILITY

The regulators are made stable with the external connected output capacitors. The output capacitors can be selected using the graphs of Figs 7 and 8.

When an electrolytic capacitor is used, the temperature behaviour of this output capacitor can cause oscillations at low temperature. The next two examples show how an output capacitor value is selected.

Example 1

The regulator 1 is made stable with an electrolytic output capacitor of 220 μF , Equivalent Series Resistance (ESR) = 0.15 Ω . At -30°C the capacitor value is

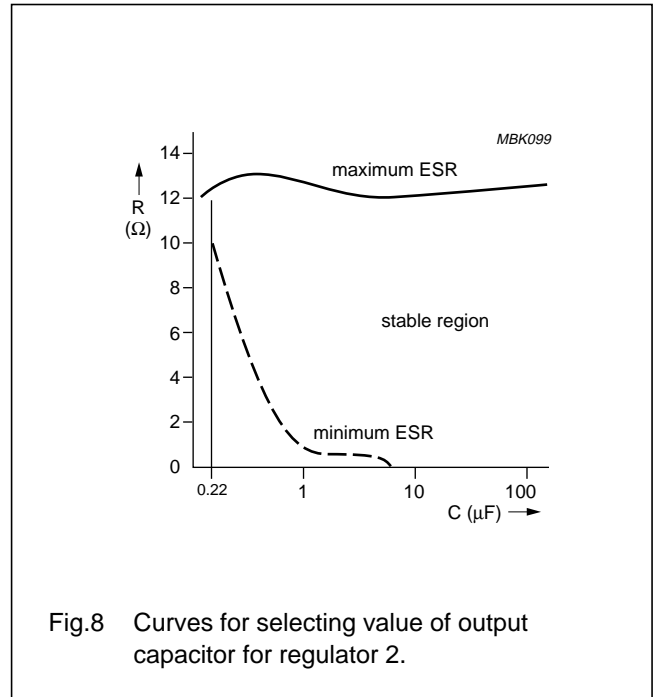
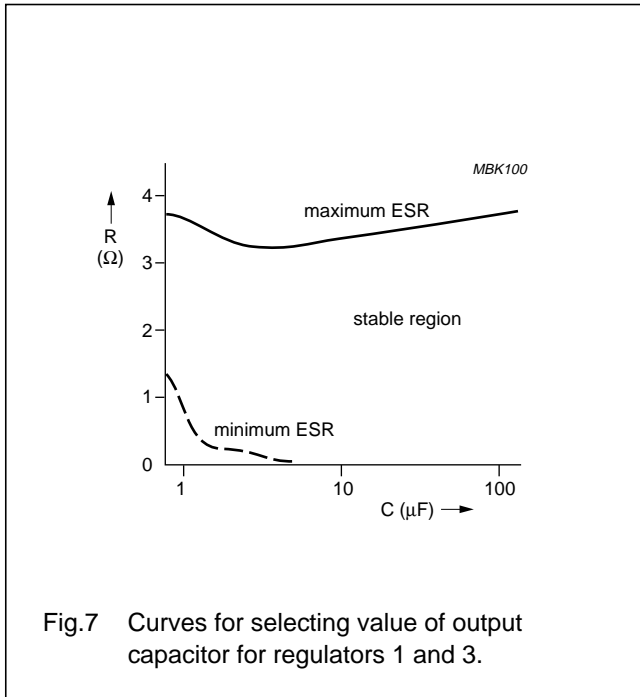
decreased to 73 μF and the ESR is increased to 1.1 Ω . The regulator will remain stable at -30°C (see Fig.7).

Example 2

The regulator 2 is made stable with a 10 μF electrolytic capacitor (ESR = 3 Ω). At -30°C the capacitor value is decreased to 3 μF and the ESR is increased to 23.1 Ω . The regulator will be instable at -30°C (see Fig.8).

Solution

Use a tantalum capacitor of 10 μF or a larger electrolytic capacitor. The use of tantalum capacitors is recommended to avoid problems with stability at low temperatures.



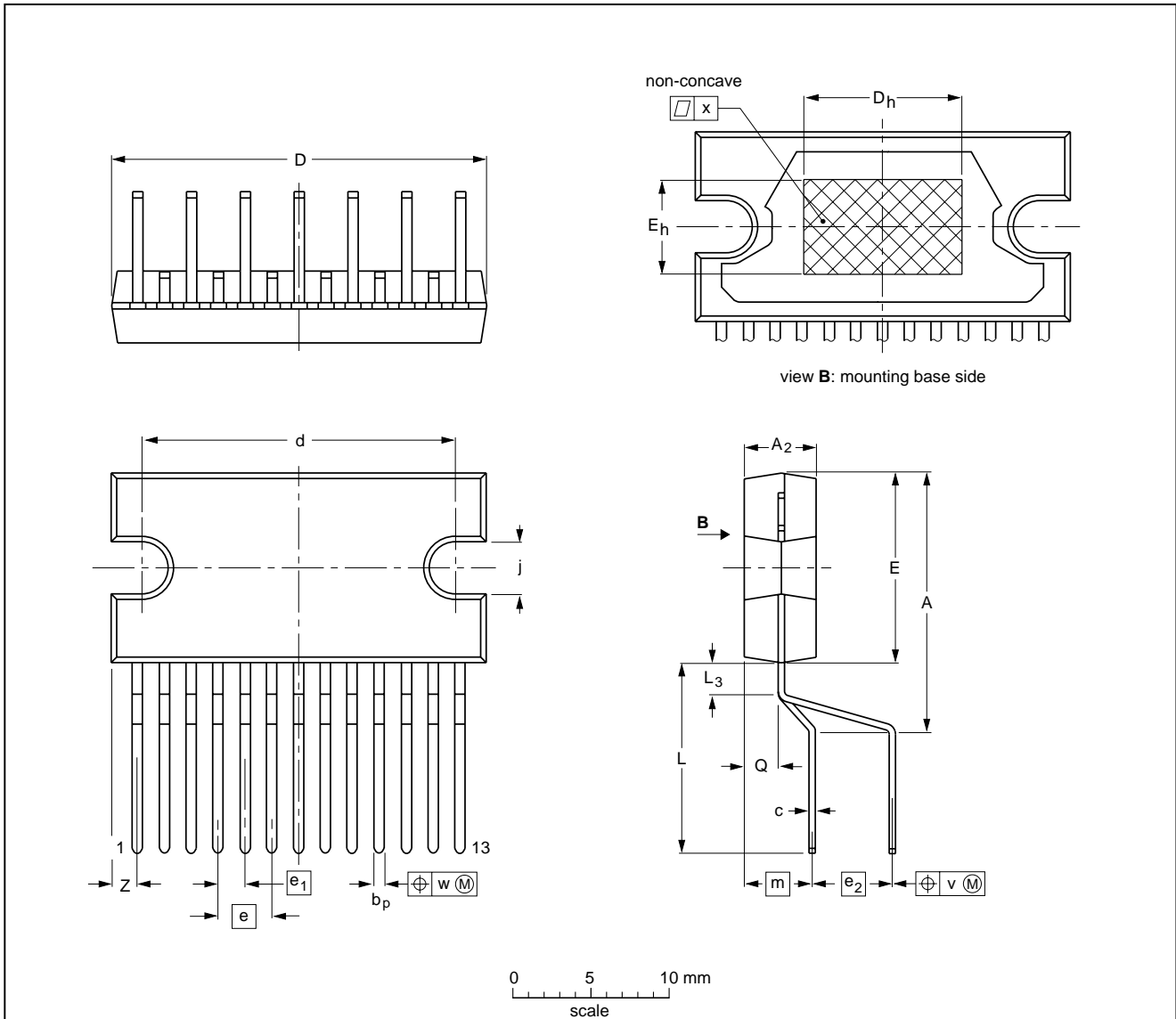
Multiple voltage regulator with switch

TDA3608Q

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-6						92-11-17 95-03-11

Multiple voltage regulator with switch

TDA3608Q

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

Multiple voltage regulator with switch

TDA3608Q

NOTES

Multiple voltage regulator with switch

TDA3608Q

NOTES

Multiple voltage regulator with switch

TDA3608Q

NOTES

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