

# TOSHIBA MOS MEMORY PRODUCTS

1,024 WORD × 4 BIT CMOS STATIC RAM  
SILICON GATE CMOS

## TC5514AP-2/-3 TC5514APL-2/-3

### DESCRIPTION

The TC5514AP is a 4,096 bit high speed and low power random access memory organized as 1,024 words by 4 bits using CMOS technology, and operates from a single 5-volt supply.

The TC5514AP is compatible with the industry produced NMOS 2114 type 4KRAM, yet offers a more than 90% reduction in power of their NMOS equivalents.

The TC5514AP is a fully CMOS RAM, therefore it is suited for use in low power applications where

battery operation and battery back up for nonvolatility are required. Furthermore the TC5514APL guaranteed a standby current equal to or less than  $1\mu\text{A}$  at  $60^\circ\text{C}$  ambient temperature is available.

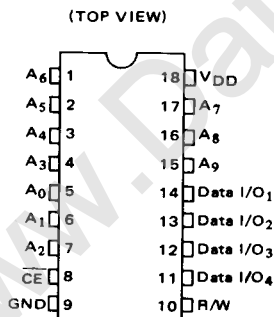
The TC5514AP is guaranteed for data retention at a power supply as low as 2 volts. The TC5514AP is directly TTL compatible in all inputs and outputs.

The TC5514AP is offered in standard 18 pin plastic, 0.3inch in width.

### FEATURES

- Standby Current
  - 0.2 $\mu\text{A}$  (Max.) at  $T_a=25^\circ\text{C}$
  - 1.0 $\mu\text{A}$  (Max.) at  $T_a=60^\circ\text{C}$
- Low Power Dissipation : 15mW (Typ.) operating
- Single 5-volt Supply :  $5\text{V} \pm 10\%$
- Data Retention Supply Voltage : 2 ~ 5.5V
- Three State Outputs
- All Inputs and Outputs : Directly TTL Compatible
- Access Time
  - 200ns (Max.) : TC5514 AP/APL-2
  - 300ns (Max.) : TC5514 AP/APL-3
- Fully Static Operation
- On-chip Address Transition Detector
- Fully Compatible with TMM2114AP Family (Nch 2114 type 4KRAM)
- Package
  - Plastic DIP : TC5514AP/APL

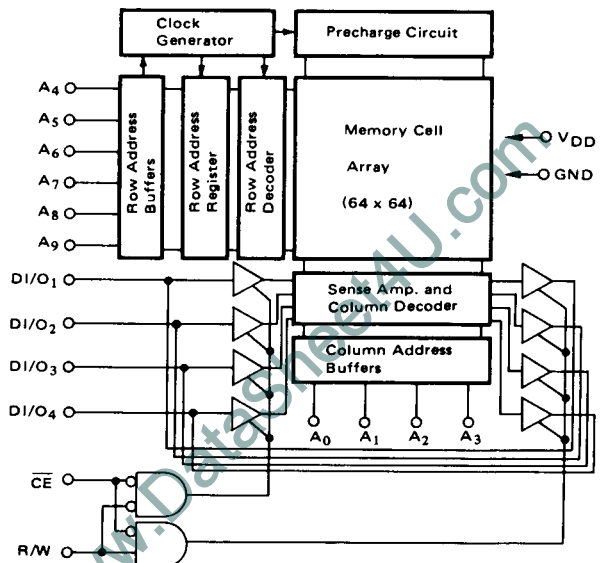
### PIN CONNECTION



### PIN NAMES

$A_0 \sim A_9$	Address Inputs
R/W	Read Write Control Input
$\overline{\text{CE}}$	Chip Enable Input
Data I/O <sub>1</sub> ~ 4	Data Input/Output
V <sub>DD</sub> /GND	Power Supply Terminals

### BLOCK DIAGRAM



# TC5514AP-2/-3

# TC5514APL-2/-3

## MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
$V_{DD}$	Power Supply Voltage	-0.3 ~ 7.0	V
$V_{IN}$	Input Voltage	-0.3 ~ 7.0	V
$V_{I/O}$	I/O Voltage	0 ~ $V_{DD}$	V
$P_D$	Power Dissipation( $T_a = 85^\circ\text{C}$ )	550	mW
$T_{SOLDER}$	Soldering Temperature · Time	260 · 10	$^\circ\text{C} \cdot \text{sec}$
$T_{STG}$	Storage Temperature	-55 ~ 150	$^\circ\text{C}$
$T_{OPR}$	Operating Temperature	-30 ~ 85	$^\circ\text{C}$

## D.C. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{DD}$	Power Supply Voltage	4.5	5.0	5.5	V
$V_{IH}$	Input High Level Voltage	2.2	-	$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Level Voltage	-0.3	-	0.8	V
$V_{DH}$	Data Retention Voltage	2.0	-	5.5	V

## D.C. CHARACTERISTICS ( $V_{DD} = 5V \pm 10\%$ , $T_a = -30 \sim 85^\circ\text{C}$ unless otherwise noted.)

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP. (1)	MAX.	UNIT	
$I_{IL}$	Input Leakage Current	$0V \leq V_{IN} \leq V_{DD}$		-	-	$\pm 1.0$	$\mu\text{A}$	
$I_{LO}$	Output Leakage Current	$\overline{CE} = V_{IH}$ , $0V \leq V_{I/O} \leq V_{DD}$		-	-	$\pm 1.0$	$\mu\text{A}$	
$I_{OH}$	Output High Current	$V_{OH} = 2.4V$		-1.0	-	-	mA	
$I_{OL}$	Output Low Current	$V_{OL} = 0.4V$		2.0	-	-	mA	
$I_{DD5}$	Standby Current	$V_{DD} = 2V \sim 5.5V$ All Inputs = $0.2V$ or $V_{DD} - 0.2V$	TC5514APL	$T_a = 25^\circ\text{C}$	-	-	0.2	$\mu\text{A}$
				$T_a = 60^\circ\text{C}$	-	-	1.0	$\mu\text{A}$
			TC5514AP	-	0.05	20	$\mu\text{A}$	
$I_{DDO1}$	Operating Current	$t_{\text{cycle}} = 1\mu\text{s}$ , $I_{OUT} = 0\text{mA}$		-	5.0	9.0	mA	
$I_{DDO2}$		$t_{\text{cycle}} = 1\mu\text{s}$ , $V_{IH} = V_{DD}$ , $V_{IL} = 0V$ , $I_{OUT} = 0\text{mA}$		-	3.0	5.0		

Note (1):  $V_{DD} = 5V$ ,  $T_a = 25^\circ\text{C}$

## CAPACITANCE<sup>(2)</sup> ( $T_a = 25^\circ\text{C}$ , $f = 1\text{MHz}$ )

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	-	4	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0V$	-	5	10	pF

Note (2): This parameter is periodically sampled and is not 100% tested.

# TC5514AP-2/-3 TC5514APL-2/-3

## A.C. CHARACTERISTICS (V<sub>DD</sub> = 5V ± 10%, T<sub>a</sub> = -30 ~ 85°C)

### • READ CYCLE

SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>RC</sub>	Read Cycle Time	200	—	300	—	ns
t <sub>ACC</sub>	Access Time	—	200	—	300	ns
t <sub>CO</sub>	CE Access Time	—	70	—	100	ns
t <sub>OH</sub>	Output Data Hold Time	15	—	20	—	ns
t <sub>DIS</sub>	Output Disable Time	—	60	—	80	ns
t <sub>COE</sub>	Output Enable Time	5	—	5	—	ns

### • WRITE CYCLE

SYMBOL	PARAMETER	TC5514AP-2/APL-2		TC5514AP-3/APL-3		UNIT
		MIN.	MAX.	MIN.	MAX.	
t <sub>WC</sub>	Write Cycle Time	200	—	300	—	ns
t <sub>AW</sub>	Address Setup Time	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	120	—	150	—	ns
t <sub>DS</sub>	Data Setup Time	120	—	150	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	ns

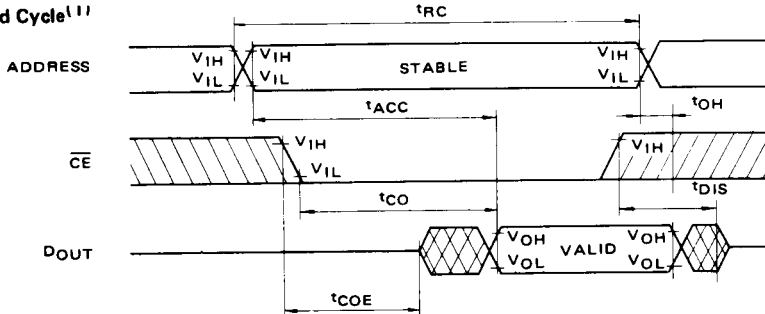
## A.C. TEST CONDITIONS

- Output Load : 100 pF + 1 TTL Gate
- Input Pulse Levels : 0.6V, 2.4V
- Timing Measurement Reference Levels
  - Input : 0.8V, 2.2V
  - Output : 0.8V, 2.2V
- Input Pulse Rise and Fall Times : 10 ns

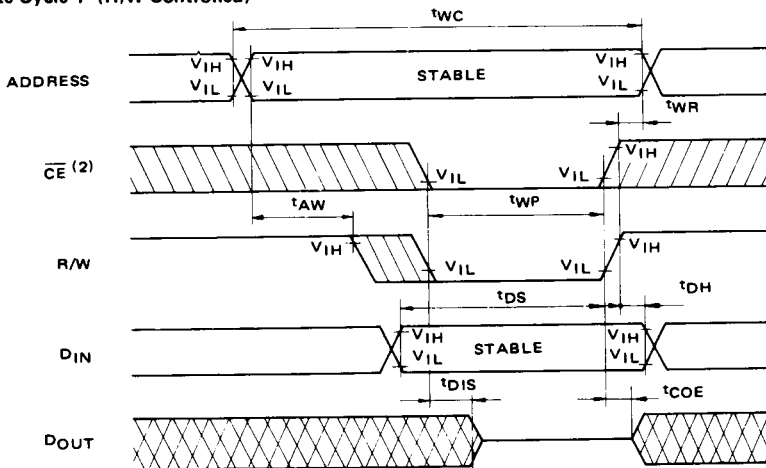
# TC5514AP-2/-3 TC5514APL-2/-3

## TIMING WAVEFORMS

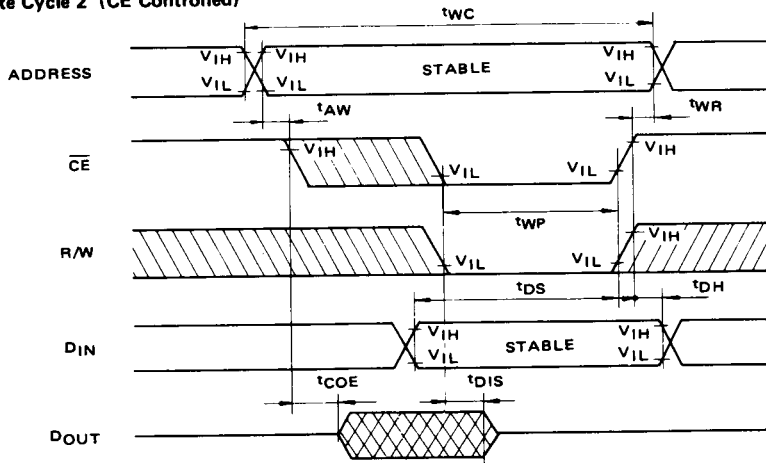
### • Read Cycle<sup>(1)</sup>



### • Write Cycle 1 (R/W Controlled)



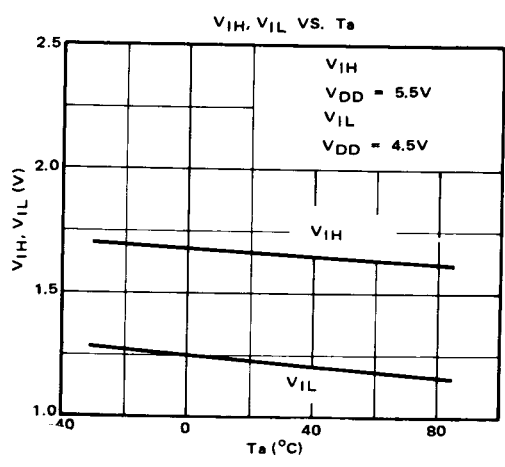
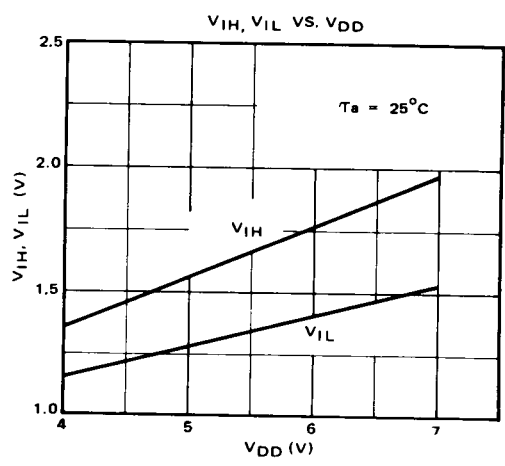
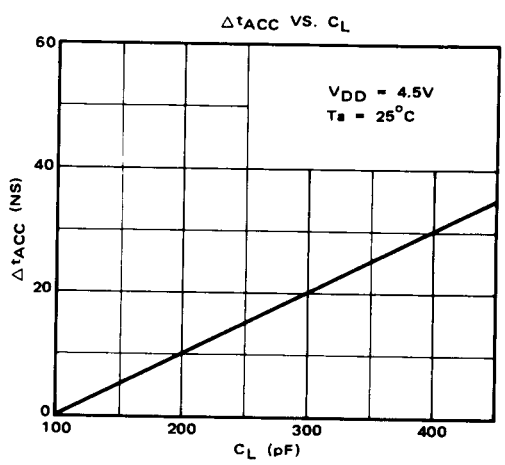
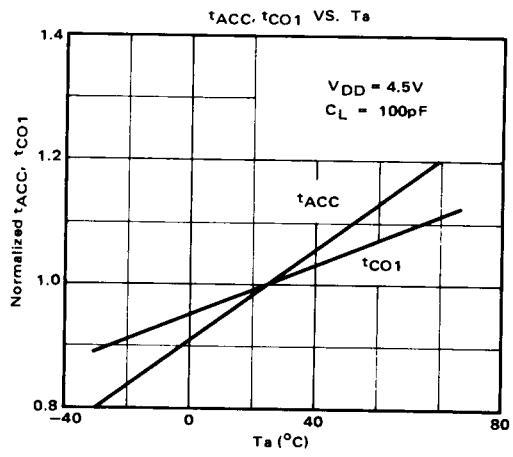
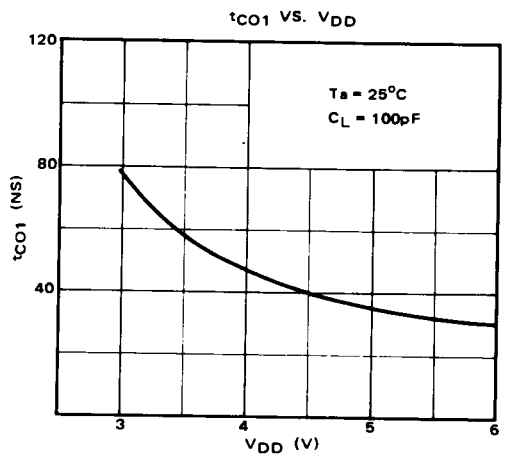
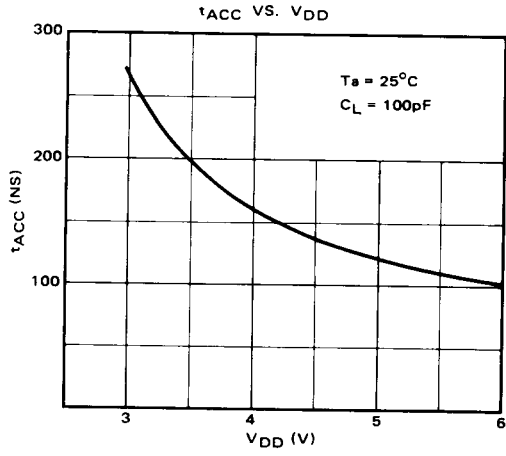
### • Write Cycle 2 ( $\overline{CE}$ Controlled)



- Notes: (1)  $R/W$  is high for a Read Cycle.  
 (2) If the  $\overline{CE}$  low transition occurs simultaneously with the  $R/W$  low transition, the output buffers remain in a high impedance state.

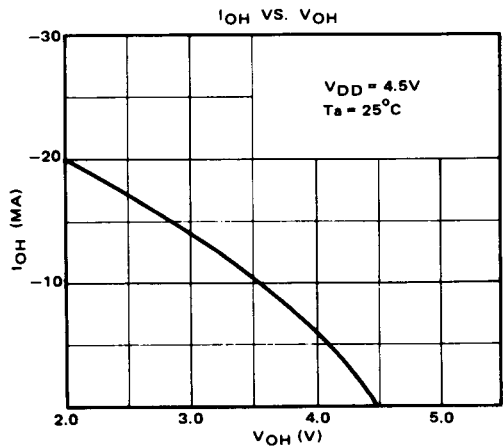
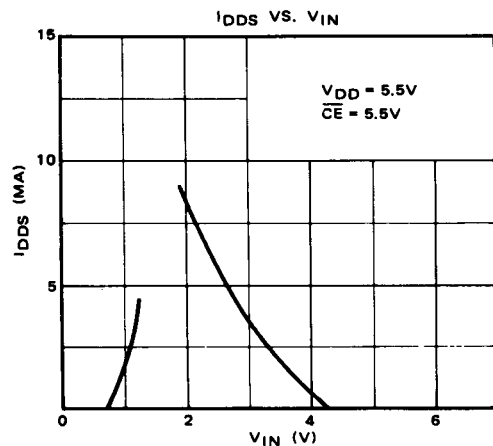
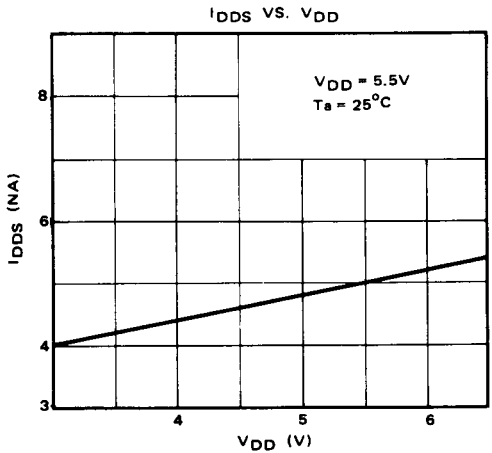
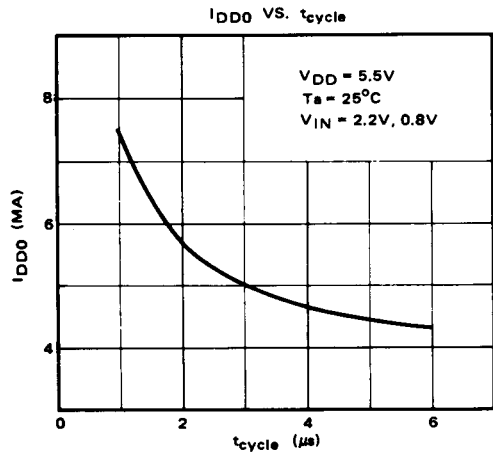
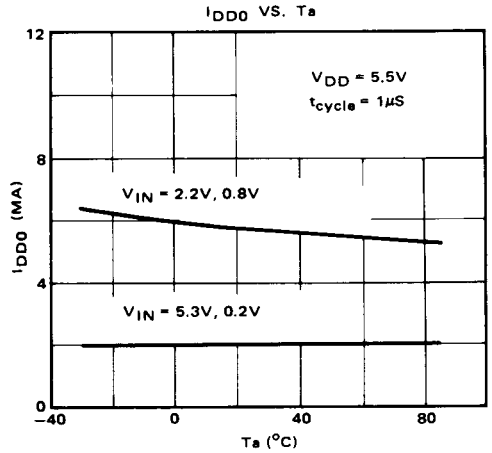
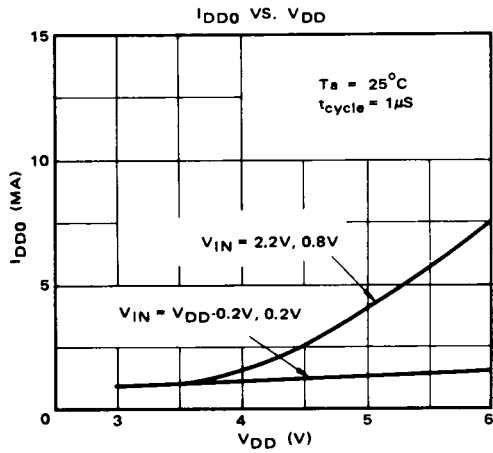
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# TC5514APL-2/-3



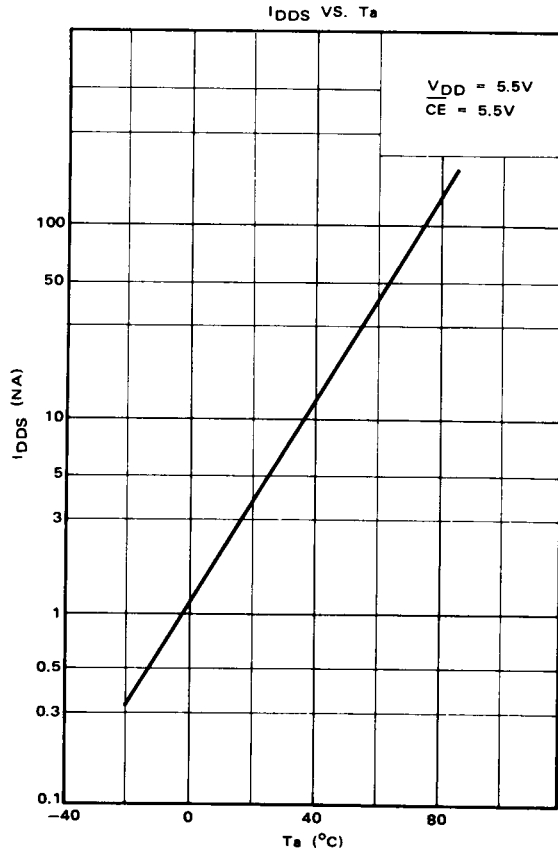
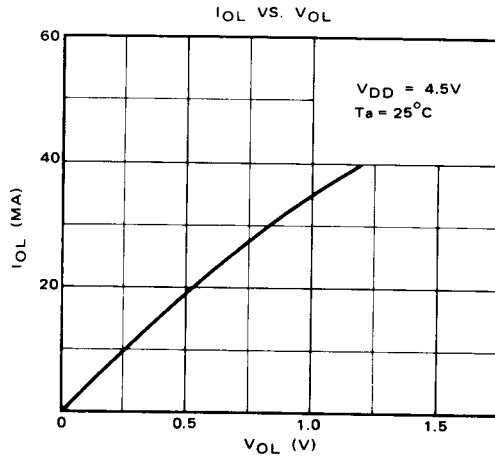
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## TC5514APL-2/-3



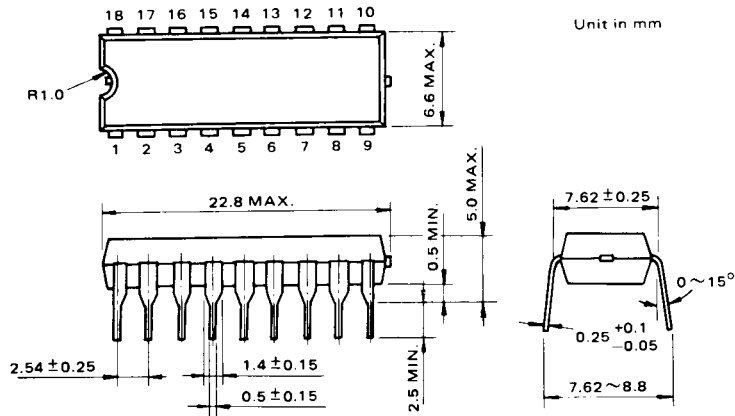
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## TC5514APL-2/-3



# TC5514AP-2/-3 TC5514APL-2/-3

● PLASTIC PACKAGE



Note : Each lead pitch is 2.54mm. All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.  
All dimensions are in millimeters.

Notes: Toshiba does not assume any responsibility for use of any circuitry described; no circuit patent licenses are implied, and Toshiba reserves the right, at any time without notice, to change said circuitry.

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