IEEE 1284 Parallel Port ESD/EMI/Termination Network

Features

- Enhanced pin-for-pin replacement for the PACSZ1284
- 17 high performance EMI filters with excellent attenuation characteristics to beyond 3GHz
- Stable, tune-free filter characteristics
- 17 ESD protectors rated at 30kV contact discharge, per the IEC 61000-4-2 ESD standard
- 17 terminators with choice of resistor values
- 28-pin QSOP-QB package

Applications

- ESD protection and EMI filtering for devices implementing a parallel port interface
- Printers
- Peripherals
- Notebook computers
- Desktop PCs
- Set Top Boxes

Product Description

The PACZIG1284 combines excellent EMI filtering, ESD protection, and signal termination in a single QSOP-QB package for parallel port interfaces complying with the IEEE 1284 standard.

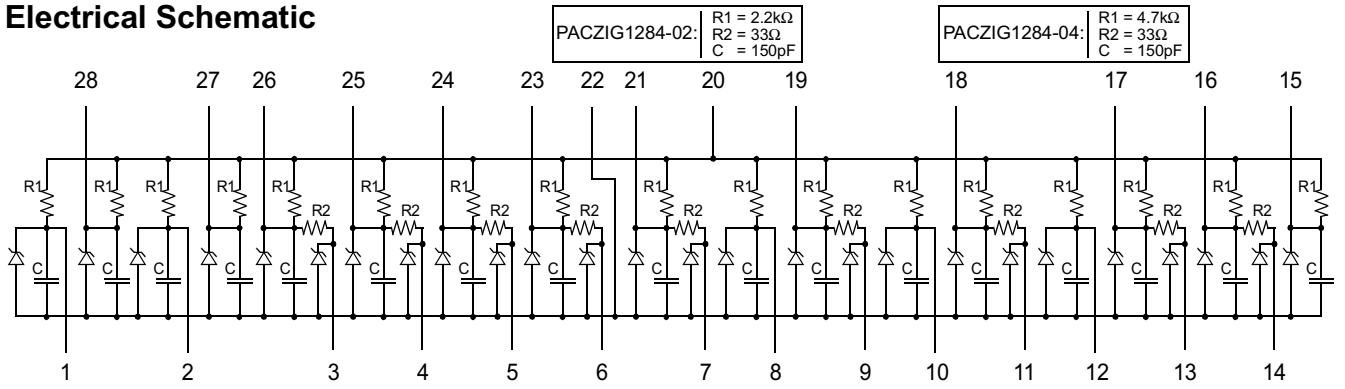
The enhanced EMI filters offer excellent attenuation characteristics, with better than 30dB rejection of unwanted frequencies from 300MHz to beyond 3GHz. This level of performance is difficult to achieve with discrete RC or ferrite bead filters, and often requires laborious tuning through trial and error. Key to the PACZIG1284's excellent EMI rejection is the innovative "Zero Inductance Ground" (ZIG™) package, which allows connection of filter grounds to the ground plane of the PC board via an essentially inductance-free ground conductor on the underside of the package.

The PACZIG1284 provides a complete parallel port termination solution. It integrates the equivalent of 60 discrete components, making it ideal for space-critical applications. The pins of the device that connect to the parallel port are protected to 30kV contact discharge, well beyond Level 4 of the IEC 61000-4-2 specification. All other pins are ESD-protected for contact discharges up to 8kV, per IEC 61000-4-2.

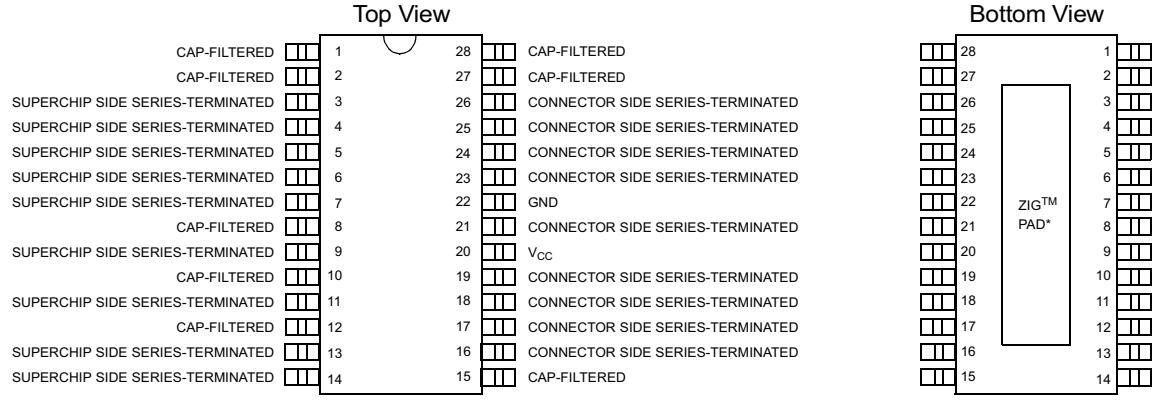
There are two available values for pull-up resistor R1. For the PACZIG1284-02, R1 = 2.2kΩ; for the PACZIG1284-04, R1 = 4.7kΩ.

P/Active® technology provides high reliability and low cost through manufacturing efficiency. The PACZIG1284 is silicon-based and has the same reliability characteristics as today's integrated circuits.

Electrical Schematic



PACKAGE / PINOUT DIAGRAMS



Note: These drawings are not to scale.

PIN DESCRIPTIONS

PINS	NAME	DESCRIPTION
1,2,8,10,12, 15,27,28	Capacitor-filtered	IEEE 1284 signals which require no series termination.
3-7, 9, 11, 13, 14	Super I/O Chip side series-terminated	IEEE 1284 signals on Super I/O Chip side which require series termination.
16-19, 21, 23-26	Parallel Port connector side series-terminated	IEEE 1284 signals on the Parallel Port Connector side which require series termination.
ZIG™ Substrate Ground Pad	Zero Inductance Ground	Exposed ground connection on underside of package. This should be electrically connected to the ground plane of the PC board. Please refer to PC board layout recommendation in Application Information section.

Ordering Information

PART NUMBERING INFORMATION

RC Code	Pins	Package	Ordering Part Number[1]	Part Marking
02	28	QSOP-QB	PACZIG128402Q	PACZIG128402Q
04	28	QSOP-QB	PACZIG128404Q	PACZIG128404Q

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

STANDARD VALUES

RC Code	R1 (Ω)	R2 (Ω)	C (pF)
02	2.2k	33	150
04	4.7k	33	150

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	**RATING**	**UNITS**
V_{CC} Voltage	5.5	V
Operating Input Voltage Range	-0.4 to 5.5	V
Storage Temperature Range	-40 to +150	°C
Power Dissipation per Resistor	0.1	W
Package Power Dissipation	1.0	W

STANDARD OPERATING CONDITIONS		
PARAMETER	**RATING**	**UNITS**
V_{CC} Voltage	5.0	V
Operating Temperature	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
TOL_R	Absolute Resistance Tolerance	Measured at 25°C			±20	%
TOL_C	Absolute Capacitance Tolerance	Measured at 1MHz, 2.5VDC, 25°C			±20	%
I_{LEAK}	Leakage current to GND	Measured at 5.0VDC, 25°C		1	10	µA
V_{ESDi}	ESD protection, input pins	Pins 3,4,5,6,7,9,11,13, & 14, per IEC 61000-4-2 specification, Notes 1,2,3	±8			kV
V_{ESD}	ESD protection, connector pins	Pins 1,2,8,10,12,15,16,17,18,19, 21,23,24,25,26,27, & 28, per IEC 61000-4-2 specification Notes 1,2,4	±30			kV
V_{CL}	Clamping voltage under ESD discharge	ESD applied to connector pin, measured at corresponding input pin; +8kV discharge, Human Body Model Notes 1,2		8.3		V
		ESD applied to connector pin, measured at corresponding input pin; -8kV discharge, Human Body Model; Notes 1,2		-2.7		V

Note 1: Guaranteed by design and characterization.
Note 2: ESD voltage applied between Input/Connector pins and ground, one pin at a time.
Note 3: Pins 3-7, 9, 11, 13, and 14 typically connect to the I/O pins of a Super I/O chip. These pins are not exposed to external ESD hazards.
Note 4: Pins 1, 2, 8, 10, 12, 15-19, 21, and 23-28 typically connect to the Parallel Port connector.

Performance Information

Filter Capacitors

The IEEE 1284 specification requires both termination and EMI filtering on a total of 17 lines. Basic filtering is provided through the presence of a capacitor on all signal lines. The filter capacitor is the junction capacitance of an ESD diode. The typical capacitance at a reverse voltage of 2.5V is 150pF. This diode capacitance is somewhat voltage dependent. See Figure 1.

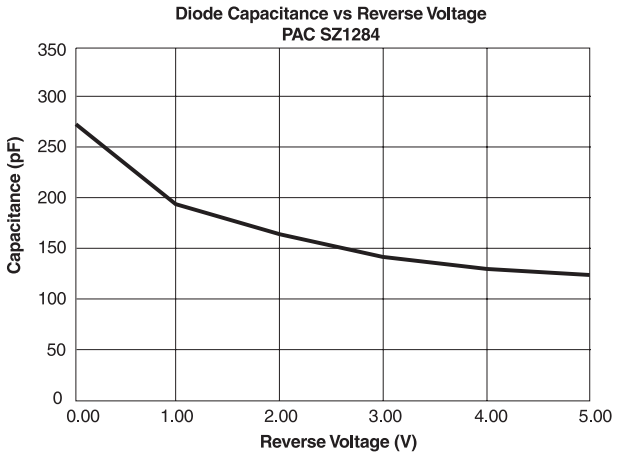


Figure 1. Diode Capacitance vs. Reverse Voltage

The higher speed Data and Strobe lines (9 in total) require an additional series resistor termination for proper operation, while the eight (8) Status lines do not. See Table 1 on page 5.

Filter Insertion Loss

Figure 2 shows the typical Insertion Loss graphs of the PACZIG1284 for Data and Strobe channels. These graphs are measured in a 50Ω environment on a Hewlett Packard HP 8753C Analyzer. The signal source is introduced at the resistor input and the output is measured at the corresponding protection diode (for example, for an input applied to pin 11, the output would be measured at pin 18). Connection to the Device Under Test (DUT) are made with RF microprobes between the respective package pins and the ZIG pad.

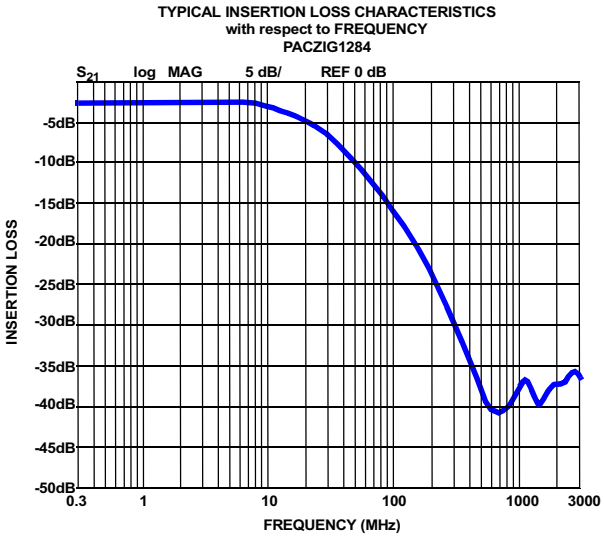


Figure 2. Typical Filter Insertion Loss

Application Information

Termination

The IEEE 1284 specification requires both termination and EMI filtering on a total of 17 signal lines. Control and Status lines (8 in total) only require a pull-up resistor and a filter capacitor. The Data lines and Strobe also require a series termination resistor in addition to the pull-up resistors and filter capacitors. See Table 1, in conjunction with the schematic diagram on page 1.

Table 1: IEEE 1284 Termination Requirements

SIGNAL TERMINATION REQUIREMENTS	
Signal Name	**Series Termination**
Data1 - Data8	Yes
Strobe	Yes
Init	Not Required
AutoFeedXT	Not Required
Selectin	Not Required
ACK	Not Required
Busy	Not Required
Paper Empty	Not Required
Select	Not Required
Fault	Not Required

Interfacing to IEEE 1284 Connectors

IEEE 1284 defines three interface connectors:

- 1284 A is a 25-pin DB series connector which is the de facto PC standard for the host connection.
- 1284 B is a 36-pin, 0.085 inch centerline connector used on the peripheral device.
- 1284 C is a new 36-pin, 0.050 inch centerline connector which can be used for both host and peripheral.

Figure 3A shows a possible hook-up between the 1284-A connector on a PC motherboard and the PACZIG1284, illustrating how the pin configuration of the PACZIG1284 allows for easy interconnect between the two. The dotted I/O signals of the PACZIG1284 will typically be connected to a Super I/O chip on the motherboard.

Figure 3B shows a possible hook-up between the 1284-B connector on a peripheral and the PACZIG1284.

Figure 3C shows a possible hook-up between the 1284-C connector and the PACZIG1284.

Operation of the PACZIG1284 **requires** proper electrical (soldered) connection of the ZIG™ substrate ground pad, as shown in Figure 4 on Page 7.

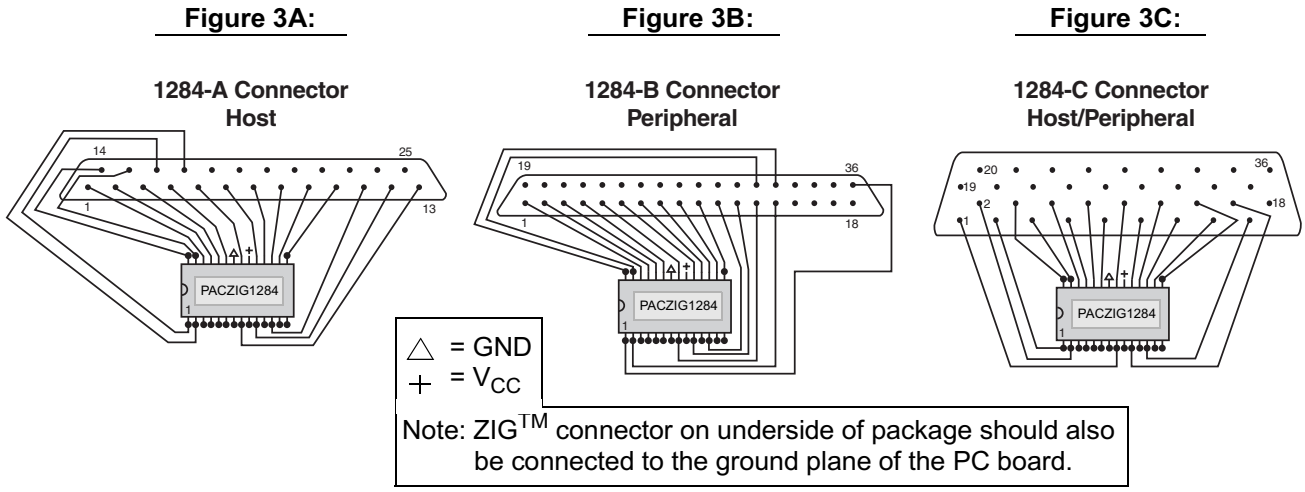


Figure 3. Example Connections of IEEE 1284 Connectors with PACZIG1284

Application Information (continued)

Table 2 provides the IEEE 1284 signal assignments for the three connectors, and example PACZIG1284 pin connections.

When connecting a 1284-A host to a 1284-B peripheral, the "Peripheral Logic High" signal is not used. Similarly, when a 1284-A host is connected to a 1284-C peripheral, the "Peripheral Logic High" and "Host Logic High" are not used. These two signals are optionally used to detect a "Power Off" or "Cable Disconnect" state for host and peripheral, respectively.

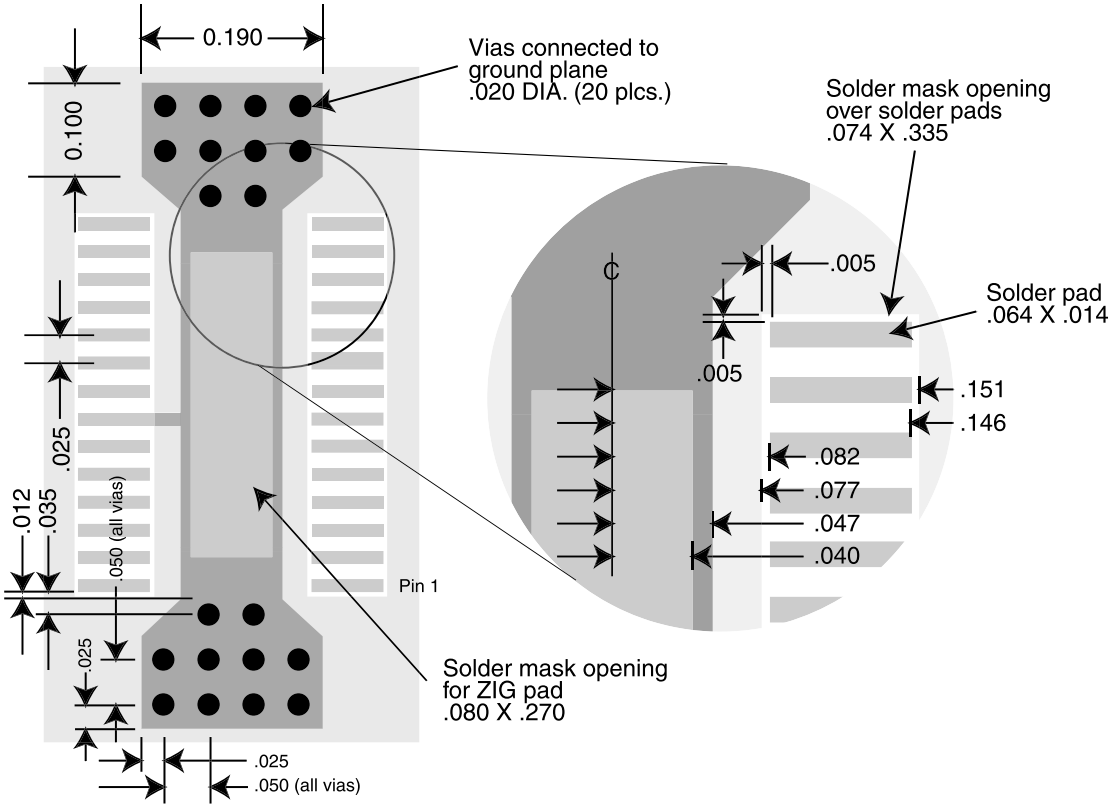
Table 2: IEEE 1284 Connector Pinouts and PACZIG1284 Connection Guidelines

PACZIG1284 PIN TYPE	1284-A 25-PIN DSUB		1284-B 36-PIN CHAMP		1284-C 36-PIN HIGH DENSITY	
	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	STROBE	1	STROBE	1	STROBE	15
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 1	2	Data 1	2	Data 1	6
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 2	3	Data 2	3	Data 2	7
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 3	4	Data 3	4	Data 3	8
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 4	5	Data 4	5	Data 4	9
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 5	6	Data 5	6	Data 5	10
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 6	7	Data 6	7	Data 6	11
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 7	8	Data 7	8	Data 7	12
P-Port conn. side, series-terminated (16-19, 21, or 23-26)	Data 8	9	Data 8	9	Data 8	13
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	ACK	10	ACK	10	ACK	3
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	BUSY	11	BUSY	11	BUSY	1
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	PError	12	PError	12	PError	5
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	Select	13	Select	13	Select	2
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	AUTOFD	14	AUTOFD	14	AUTOFD	17
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	FAULT	15	FAULT	32	FAULT	4
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	INIT	16	INIT	31	INIT	14
Capacitor-filtered (1, 2, 8, 10, 12, 15, 27, or 28)	Selectin	17	Selectin	36	Selectin	16
	Ground	18	Ground	19	Ground	19
	Ground	19	Ground	20	Ground	20
	Ground	20	Ground	21	Ground	21
	Ground	21	Ground	22	Ground	22
	Ground	22	Ground	23	Ground	23
	Ground	23	Ground	24	Ground	24
	Ground	24	Ground	25	Ground	25
	Ground	25	Ground	26	Ground	26
			Ground	27	Ground	27
			Ground	28	Ground	28
			Ground	29	Ground	29
			Ground	30	Ground	30
			Not Defined	33	Ground	31
			Not Defined	34	Ground	32
			Not Defined	35	Ground	33
			Not Defined	15	Ground	34
			Logic Ground	16	Ground	35
			Chassis GND	17	Not Required	36
			Peripheral Logic	18	Host Logic High	18

Application Information (continued)

PC Board Layout

Figure 4 shows the recommended printed circuit board layout for connecting the PACZIG1284. Multiple ground plane vias should be placed at both ends and as close as possible to the PACZIG1284.



Notes
1) All dimensions in Inches.
2) Solder mask over Bare Copper (SMOBC).
3) Solder pad finish is OSP (Entec Cu Plus 106A) or tin-lead reflow.

Figure 4. Recommended PC Board Layout for ZIG™ Connection

Mechanical Details

QSOP-QB Mechanical Specifications:

PACZIG1284 devices are packaged in 28-pin QSOP-QB packages which feature a large zero-inductance substrate ground connection (ZIG™ PAD) on the undersurface of the package. Dimensions are presented below.

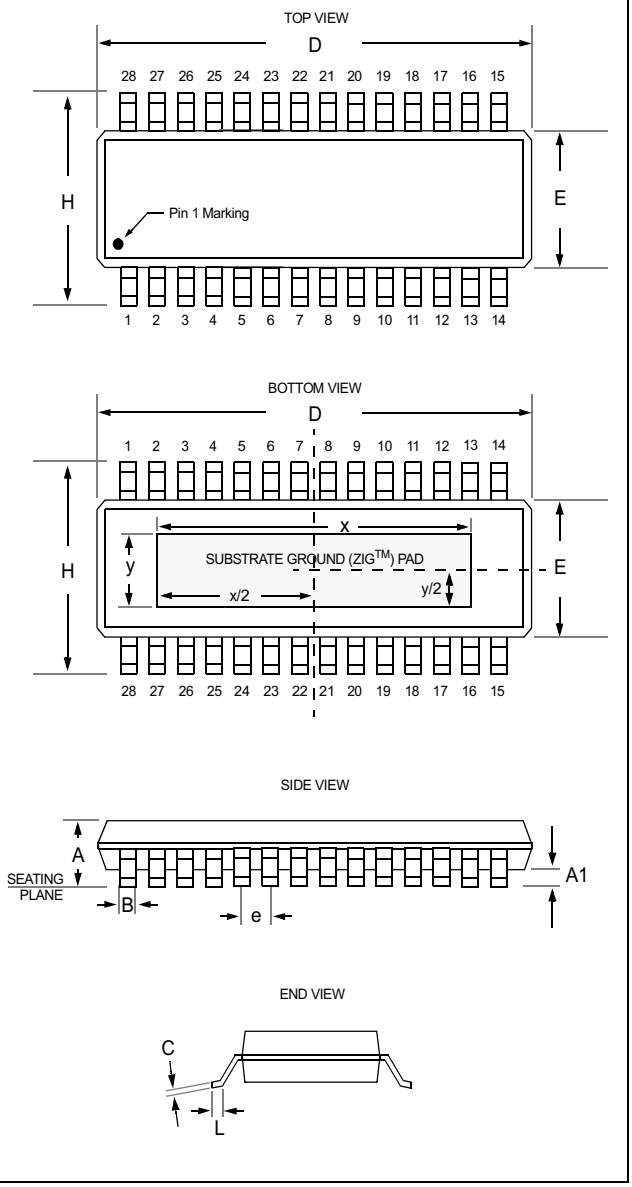
For complete information on the QSOP-QB-28 package, see the California Micro Devices QSOP-QB Package Information document.

PACKAGE DIMENSIONS				
Package	QSOP-QB (JEDEC name is SSOP)			
Pins	28			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	1.35	1.75	0.053	0.069
A1	0.03	0.1	0.001	0.004
B	0.20	0.30	0.008	0.012
C	0.18	0.25	0.007	0.010
D	9.80	10.00	0.386	0.394
E	3.81	3.98	0.150	0.157
e	0.64 BSC		0.025 BSC	
H	5.79	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
x**	6.60	7.11	0.260	0.280
y**	2.29	2.79	0.090	0.110
# per tube	50 pieces*			
# per tape and reel	2500 pieces			
Controlling Dimensions: inches				

* This is an approximate amount which may vary.

** Centered on package centerline.

Mechanical Package Diagrams



Package Dimensions for QSOP-QB-28