

**MD51V65165****4,194,304-Word × 16-Bit DYNAMIC RAM : FAST PAGE MODE TYPE WITH EDO****DESCRIPTION**

The MD51V65165 is a 4,194,304-word × 16-bit dynamic RAM fabricated in Oki's silicon-gate CMOS technology. The MD51V65165 achieves high integration, high-speed operation, and low-power consumption because Oki manufactures the device in a quadruple-layer polysilicon/double-layer metal CMOS process. The MD51V65165 is available in a 50-pin plastic SOJ or 50-pin plastic TSOP.

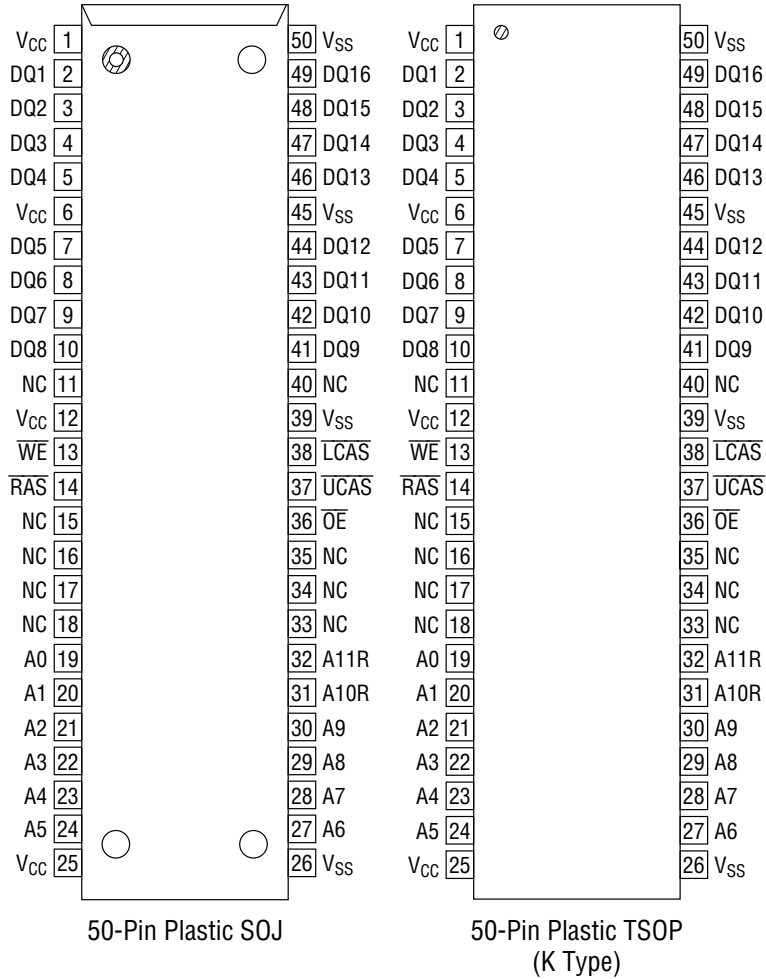
**FEATURES**

- 4,194,304-word × 16-bit configuration
  - Single 3.3 V power supply, ±0.3 V tolerance
  - Input : LVTTTL compatible, low input capacitance
  - Output : LVTTTL compatible, 3-state
  - Refresh :
    - $\overline{\text{RAS}}$ -only refresh : 4096 cycles/64 ms
    - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh : 4096 cycles/64 ms
  - Fast page mode with EDO, read modify write capability
  - $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh, hidden refresh,  $\overline{\text{RAS}}$ -only refresh capability
  - Package options:
    - 50-pin 400 mil plastic SOJ (SOJ50-P-400-0.80) (Product : MD51V65165-xxJA)
    - 50-pin 400 mil plastic TSOP (TSOPII50-P-400-0.80-1K) (Product : MD51V65165-xxTA)
- xx indicates speed rank.

**PRODUCT FAMILY**

Family	Access Time (Max.)				Cycle Time (Min.)	Power Dissipation	
	t <sub>RAC</sub>	t <sub>AA</sub>	t <sub>CAC</sub>	t <sub>OEa</sub>		Operating (Max.)	Standby (Max.)
MD51V65165-50	50 ns	25 ns	13 ns	13 ns	84 ns	504 mW	1.8 mW
MD51V65165-60	60 ns	30 ns	15 ns	15 ns	104 ns	432 mW	

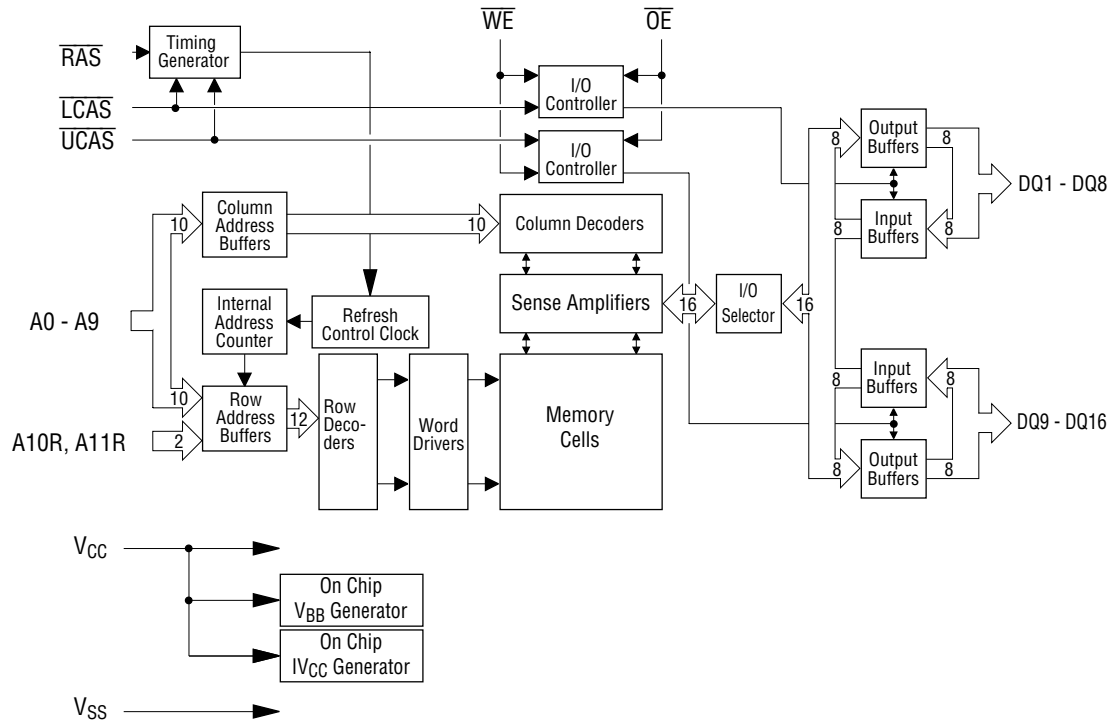
**PIN CONFIGURATION (TOP VIEW)**



Pin Name	Function
A0 - A9, A10R, A11R	Address Input
RAS	Row Address Strobe
LCAS	Lower Byte Column Address Strobe
UCAS	Upper Byte Column Address Strobe
DQ1 - DQ16	Data Input/Data Output
OE	Output Enable
WE	Write Enable
V <sub>CC</sub>	Power Supply (3.3 V)
V <sub>SS</sub>	Ground (0 V)
NC	No Connection

Note : The same power supply voltage must be provided to every V<sub>CC</sub> pin, and the same GND voltage level must be provided to every V<sub>SS</sub> pin.

**BLOCK DIAGRAM**



**ELECTRICAL CHARACTERISTICS****Absolute Maximum Ratings**

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_T$	-0.5 to 4.6	V
Short Circuit Output Current	$I_{OS}$	50	mA
Power Dissipation	$P_D^*$	1	W
Operating Temperature	$T_{opr}$	0 to 70	°C
Storage Temperature	$T_{stg}$	-55 to 150	°C

\*:  $T_a = 25^\circ\text{C}$ **Recommended Operating Conditions** $(T_a = 0^\circ\text{C to } 70^\circ\text{C})$ 

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	$V_{CC}$	3.0	3.3	3.6	V
	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.0	—	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	—	0.8	V

**Capacitance** $(V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}, T_a = 25^\circ\text{C}, f = 1\text{ MHz})$ 

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A0 - A9, A10R, A11R)	$C_{IN1}$	—	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{LCAS}}$ , $\overline{\text{UCAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{IN2}$	—	7	pF
Output Capacitance (DQ1 - DQ16)	$C_{I/O}$	—	7	pF

**DC Characteristics**

( $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ,  $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Condition	MD51V65165 -50		MD51V65165 -60		Unit	Note
			Min.	Max.	Min.	Max.		
Output High Voltage	$V_{OH}$	$I_{OH} = -2.0\text{ mA}$	2.4	$V_{CC}$	2.4	$V_{CC}$	V	
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.0\text{ mA}$	0	0.4	0	0.4	V	
Input Leakage Current	$I_{LI}$	$0\text{ V} \leq V_I \leq V_{CC} + 0.3\text{ V}$ ; All other pins not under test = 0 V	-10	10	-10	10	$\mu\text{A}$	
Output Leakage Current	$I_{LO}$	DQ disable $0\text{ V} \leq V_O \leq V_{CC}$	-10	10	-10	10	$\mu\text{A}$	
Average Power Supply Current (Operating)	$I_{CC1}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ cycling, $t_{RC} = \text{Min.}$	—	140	—	120	mA	1, 2
Power Supply Current (Standby)	$I_{CC2}$	$\overline{\text{RAS}}$ , $\overline{\text{CAS}} = V_{IH}$	—	1	—	1	mA	1
		$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ $\geq V_{CC} - 0.2\text{ V}$	—	0.5	—	0.5		
Average Power Supply Current ( $\overline{\text{RAS}}$ -only Refresh)	$I_{CC3}$	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ , $t_{RC} = \text{Min.}$	—	140	—	120	mA	1, 2
Power Supply Current (Standby)	$I_{CC5}$	$\overline{\text{RAS}} = V_{IH}$ , $\overline{\text{CAS}} = V_{IL}$ , DQ = enable	—	5	—	5	mA	1
Average Power Supply Current ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	$I_{CC6}$	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$	—	140	—	120	mA	1, 2
Average Power Supply Current (Fast Page Mode)	$I_{CC7}$	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ cycling, $t_{HPC} = \text{Min.}$	—	140	—	120	mA	1, 3

- Notes :
1.  $I_{CC}$  Max. is specified as  $I_{CC}$  for output open condition.
  2. The address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ .
  3. The address can be changed once or less while  $\overline{\text{CAS}} = V_{IH}$ .

## AC Characteristics (1/2)

 $(V_{CC} = 3.3 V \pm 0.3 V, T_a = 0^\circ C \text{ to } 70^\circ C)$  Note 1, 2, 3

Parameter	Symbol	MD51V65165 -50		MD51V65165 -60		Unit	Note
		Min.	Max.	Min.	Max.		
Random Read or Write Cycle Time	$t_{RC}$	84	—	104	—	ns	
Read Modify Write Cycle Time	$t_{RWC}$	110	—	135	—	ns	
Fast Page Mode Cycle Time	$t_{HPC}$	20	—	25	—	ns	
Fast Page Mode Read Modify Write Cycle Time	$t_{HPRWC}$	58	—	68	—	ns	
Access Time from $\overline{RAS}$	$t_{RAC}$	—	50	—	60	ns	4, 5, 6
Access Time from $\overline{CAS}$	$t_{CAC}$	—	13	—	15	ns	4, 5
Access Time from Column Address	$t_{AA}$	—	25	—	30	ns	4, 6
Access Time from $\overline{CAS}$ Precharge	$t_{CPA}$	—	30	—	35	ns	4, 13
Access Time from $\overline{OE}$	$t_{OEA}$	—	13	—	15	ns	4
Output Low Impedance Time from $\overline{CAS}$	$t_{CLZ}$	0	—	0	—	ns	4
Data Output Hold After $\overline{CAS}$ Low	$t_{DOH}$	5	—	5	—	ns	
$\overline{CAS}$ to Data Output Buffer Turn-off Delay Time	$t_{CEZ}$	0	13	0	15	ns	7, 8
$\overline{RAS}$ to Data Output Buffer Turn-off Delay Time	$t_{REZ}$	0	13	0	15	ns	7, 8
$\overline{OE}$ to Data Output Buffer Turn-off Delay Time	$t_{OEZ}$	0	13	0	15	ns	7
$\overline{WE}$ to Data Output Buffer Turn-off Delay Time	$t_{WEZ}$	0	13	0	15	ns	7
Transition Time	$t_T$	1	50	1	50	ns	3
Refresh Period	$t_{REF}$	—	64	—	64	ms	
$\overline{RAS}$ Precharge Time	$t_{RP}$	30	—	40	—	ns	
$\overline{RAS}$ Pulse Width	$t_{RAS}$	50	10,000	60	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode with EDO)	$t_{RASP}$	50	100,000	60	100,000	ns	
$\overline{RAS}$ Hold Time	$t_{RSH}$	7	—	10	—	ns	
$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	$t_{ROH}$	7	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Fast Page Mode with EDO)	$t_{CP}$	7	—	10	—	ns	15
$\overline{CAS}$ Pulse Width	$t_{CAS}$	7	10,000	10	10,000	ns	
$\overline{CAS}$ Hold Time	$t_{CSH}$	35	—	40	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	$t_{CRP}$	5	—	5	—	ns	13
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	$t_{RHCP}$	30	—	35	—	ns	13
$\overline{OE}$ Hold Time from $\overline{CAS}$ (DQ Disable)	$t_{CHO}$	5	—	5	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	$t_{RCD}$	11	37	14	45	ns	5
$\overline{RAS}$ to Column Address Delay Time	$t_{RAD}$	9	25	12	30	ns	6
Row Address Set-up Time	$t_{ASR}$	0	—	0	—	ns	
Row Address Hold Time	$t_{RAH}$	7	—	10	—	ns	
Column Address Set-up Time	$t_{ASC}$	0	—	0	—	ns	12
Column Address Hold Time	$t_{CAH}$	7	—	10	—	ns	12
Column Address to $\overline{RAS}$ Lead Time	$t_{RAL}$	25	—	30	—	ns	

## AC Characteristics (2/2)

(V<sub>CC</sub> = 3.3 V ±0.3 V, T<sub>a</sub> = 0°C to 70°C) Note 1, 2, 3

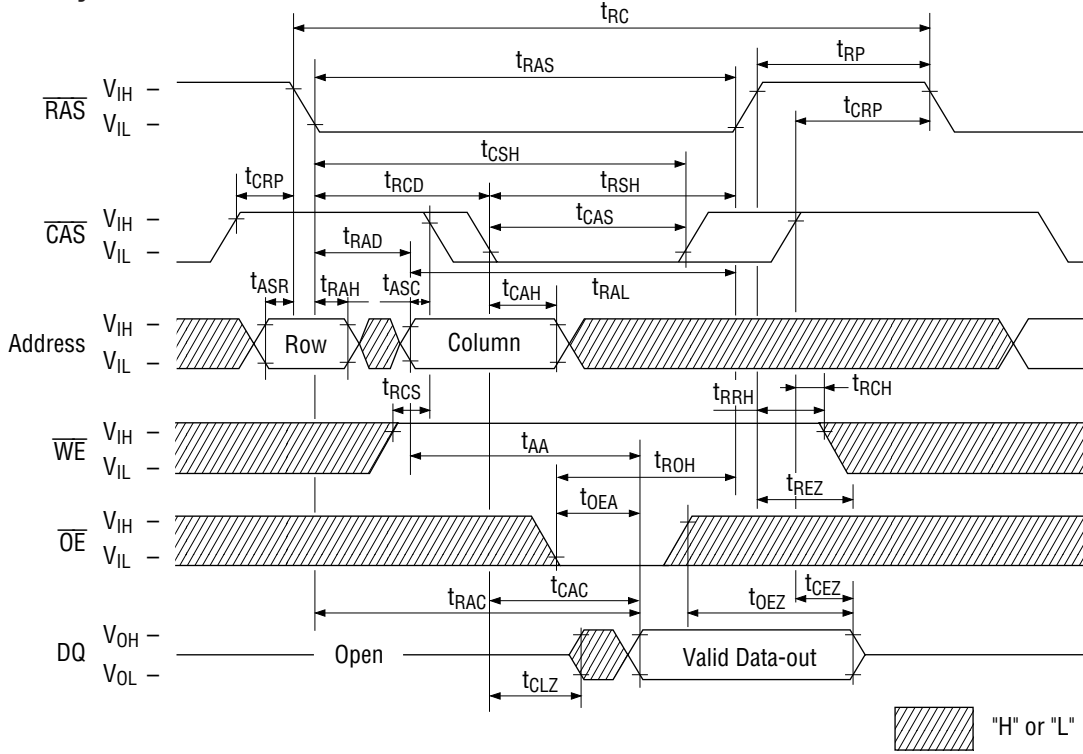
Parameter	Symbol	MD51V65165 -50		MD51V65165 -60		Unit	Note
		Min.	Max.	Min.	Max.		
Read Command Set-up Time	t <sub>RCS</sub>	0	—	0	—	ns	12
Read Command Hold Time	t <sub>RCH</sub>	0	—	0	—	ns	9, 12
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t <sub>RRH</sub>	0	—	0	—	ns	9
Write Command Set-up Time	t <sub>WCS</sub>	0	—	0	—	ns	10, 12
Write Command Hold Time	t <sub>WCH</sub>	7	—	10	—	ns	12
Write Command Pulse Width	t <sub>WP</sub>	7	—	10	—	ns	
$\overline{\text{WE}}$ Pulse Width (DQ Disable)	t <sub>WPE</sub>	7	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OEH</sub>	7	—	10	—	ns	
$\overline{\text{OE}}$ Precharge Time	t <sub>OEP</sub>	7	—	10	—	ns	
$\overline{\text{OE}}$ Command Hold Time	t <sub>OCH</sub>	7	—	10	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t <sub>RWL</sub>	7	—	10	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t <sub>CWL</sub>	7	—	10	—	ns	14
Data-in Set-up Time	t <sub>DS</sub>	0	—	0	—	ns	11, 12
Data-in Hold Time	t <sub>DH</sub>	7	—	10	—	ns	11, 12
$\overline{\text{OE}}$ to Data-in Delay Time	t <sub>OED</sub>	13	—	15	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>CWD</sub>	30	—	34	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t <sub>AWD</sub>	42	—	49	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t <sub>RWD</sub>	67	—	79	—	ns	10
$\overline{\text{CAS}}$ Precharge $\overline{\text{WE}}$ Delay Time	t <sub>CPWD</sub>	47	—	54	—	ns	10
$\overline{\text{CAS}}$ Active Delay Time from $\overline{\text{RAS}}$ Precharge	t <sub>RPC</sub>	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Set-up Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CSR</sub>	5	—	5	—	ns	12
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>CHR</sub>	10	—	10	—	ns	13
$\overline{\text{WE}}$ to $\overline{\text{RAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>WRP</sub>	10	—	10	—	ns	
$\overline{\text{WE}}$ Hold Time from $\overline{\text{RAS}}$ ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ )	t <sub>WRH</sub>	10	—	10	—	ns	

- Notes:
1. A start-up delay of 200  $\mu$ s is required after power-up, followed by a minimum of eight initialization cycles ( $\overline{\text{RAS}}$ -only refresh or  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh) before proper device operation is achieved.
  2. The AC characteristics assume  $t_T = 2$  ns.
  3.  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.) are reference levels for measuring input timing signals. Transition times ( $t_T$ ) are measured between  $V_{IH}$  and  $V_{IL}$ .
  4. This parameter is measured with a load circuit equivalent to 1 TTL load and 100 pF. The output timing reference levels are  $V_{OH} = 2.0$  V and  $V_{OL} = 0.8$  V.
  5. Operation within the  $t_{RCD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RCD}$  (Max.) is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (Max.) limit, then the access time is controlled by  $t_{CAC}$ .
  6. Operation within the  $t_{RAD}$  (Max.) limit ensures that  $t_{RAC}$  (Max.) can be met.  $t_{RAD}$  (Max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (Max.) limit, then the access time is controlled by  $t_{AA}$ .
  7.  $t_{CEZ}$  (Max.),  $t_{REZ}$  (Max.),  $t_{WEZ}$  (Max.) and  $t_{OEZ}$  (Max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
  8.  $t_{CEZ}$  and  $t_{REZ}$  must be satisfied for open circuit condition.
  9.  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
  10.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CPWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}$  (Min.), then the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle. If  $t_{CWD} \geq t_{CWD}$  (Min.),  $t_{RWD} \geq t_{RWD}$  (Min.),  $t_{AWD} \geq t_{AWD}$  (Min.) and  $t_{CPWD} \geq t_{CPWD}$  (Min.), then the cycle is a read modify write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, then the condition of the data out (at access time) is indeterminate.
  11. These parameters are referenced to the  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ , leading edges in an early write cycle, and to the  $\overline{\text{WE}}$  leading edge in an  $\overline{\text{OE}}$  control write cycle, or a read modify write cycle.
  12. These parameters are determined by the falling edge of either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ , whichever is earlier.
  13. These parameters are determined by the rising edge of either  $\overline{\text{UCAS}}$  or  $\overline{\text{LCAS}}$ , whichever is later.
  14.  $t_{CWL}$  should be satisfied by both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$ .
  15.  $t_{CP}$  is determined by the time both  $\overline{\text{UCAS}}$  and  $\overline{\text{LCAS}}$  are high.

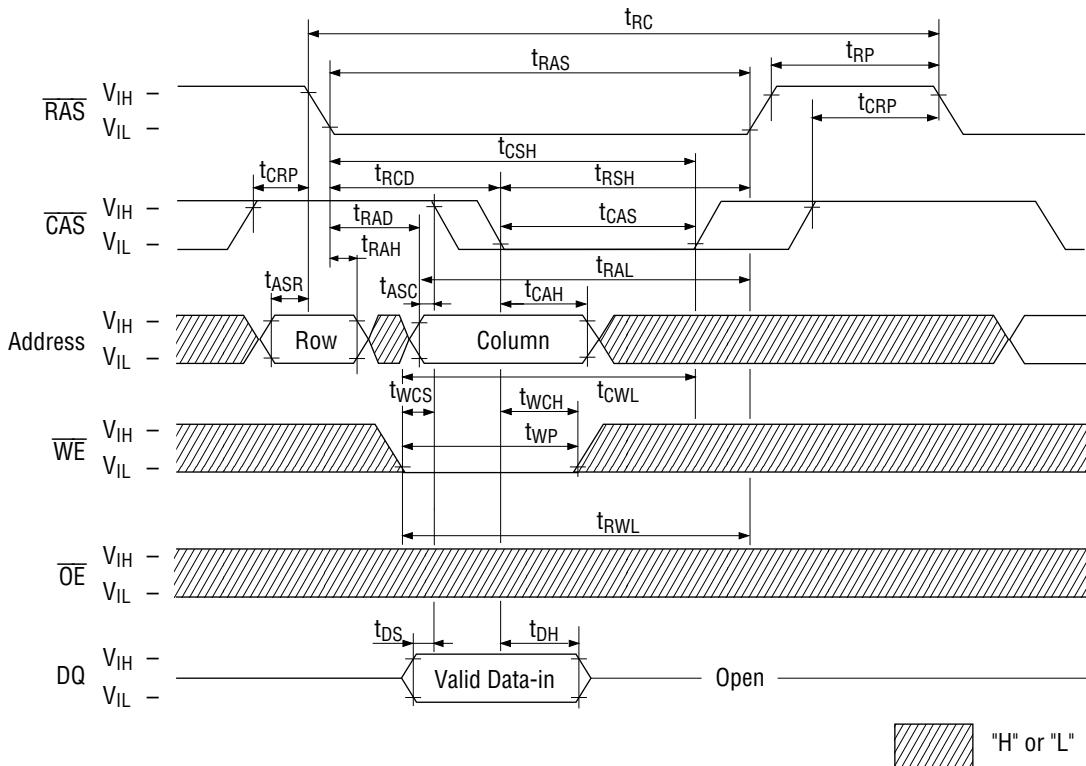


**TIMING WAVEFORM**

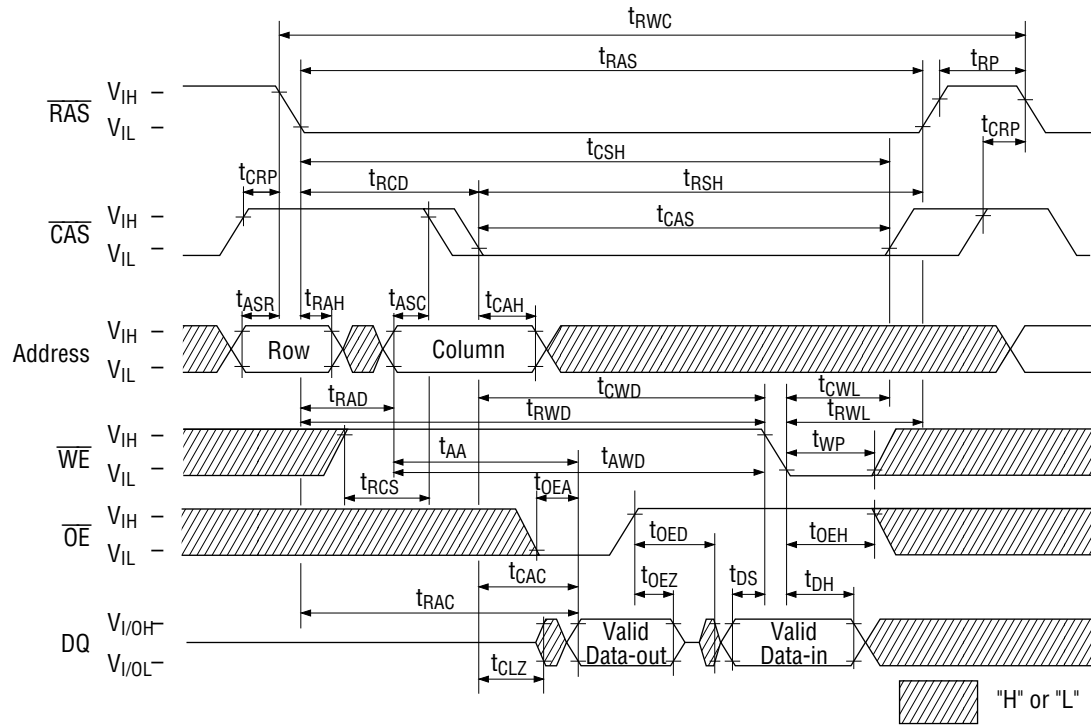
**Read Cycle**



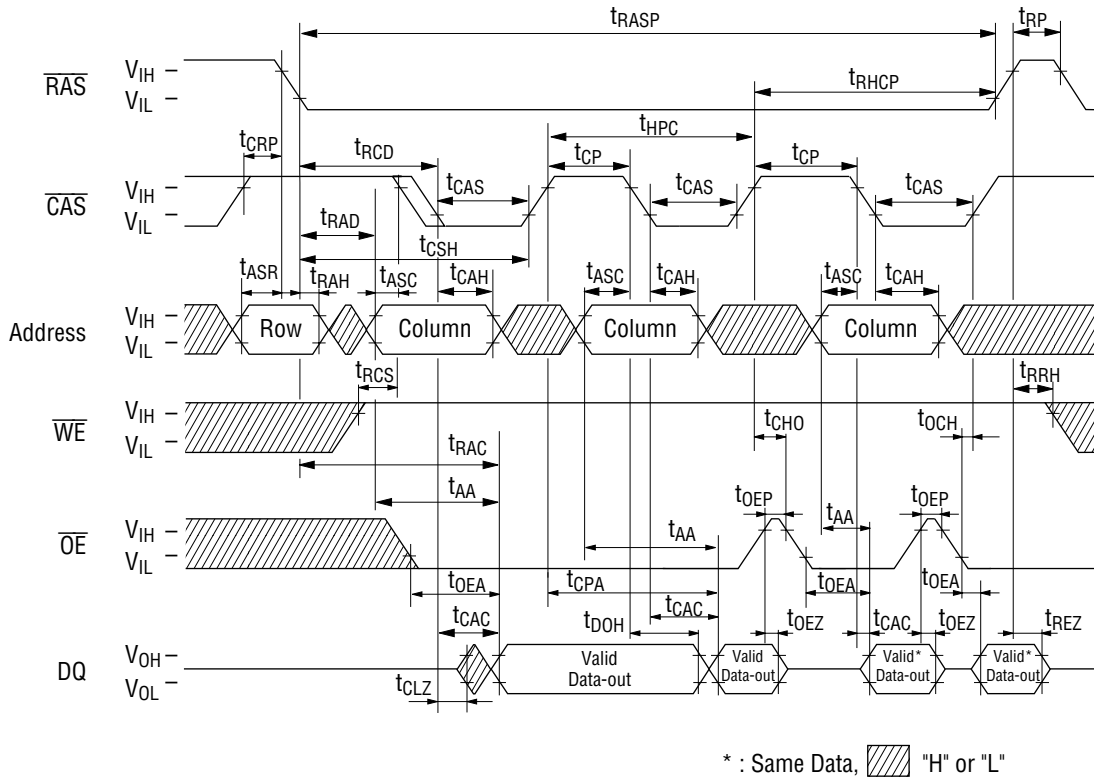
**Write Cycle (Early Write)**



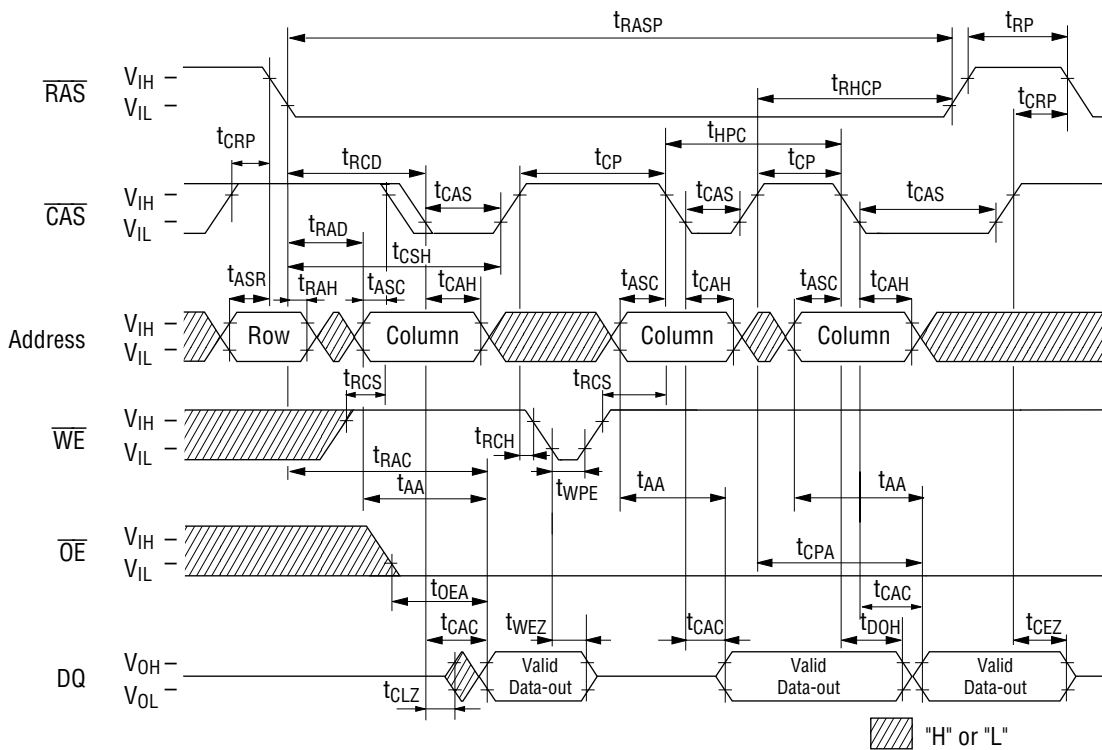
Read Modify Write Cycle



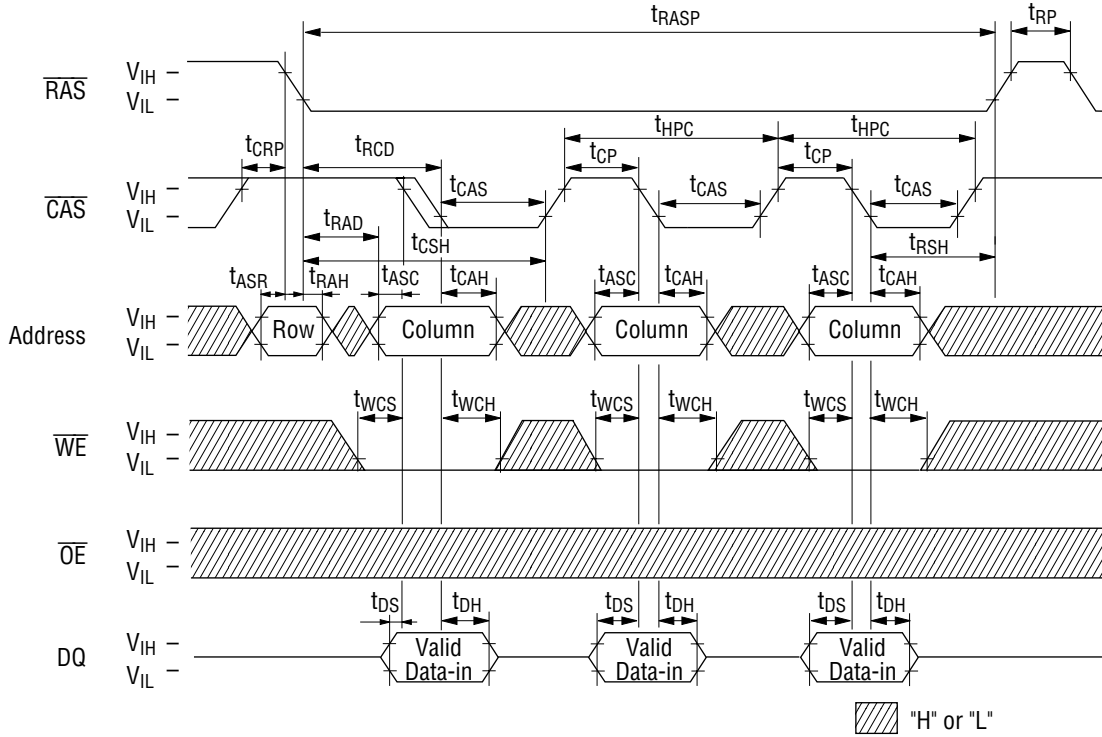
Fast Page Mode Read Cycle (Part-1)



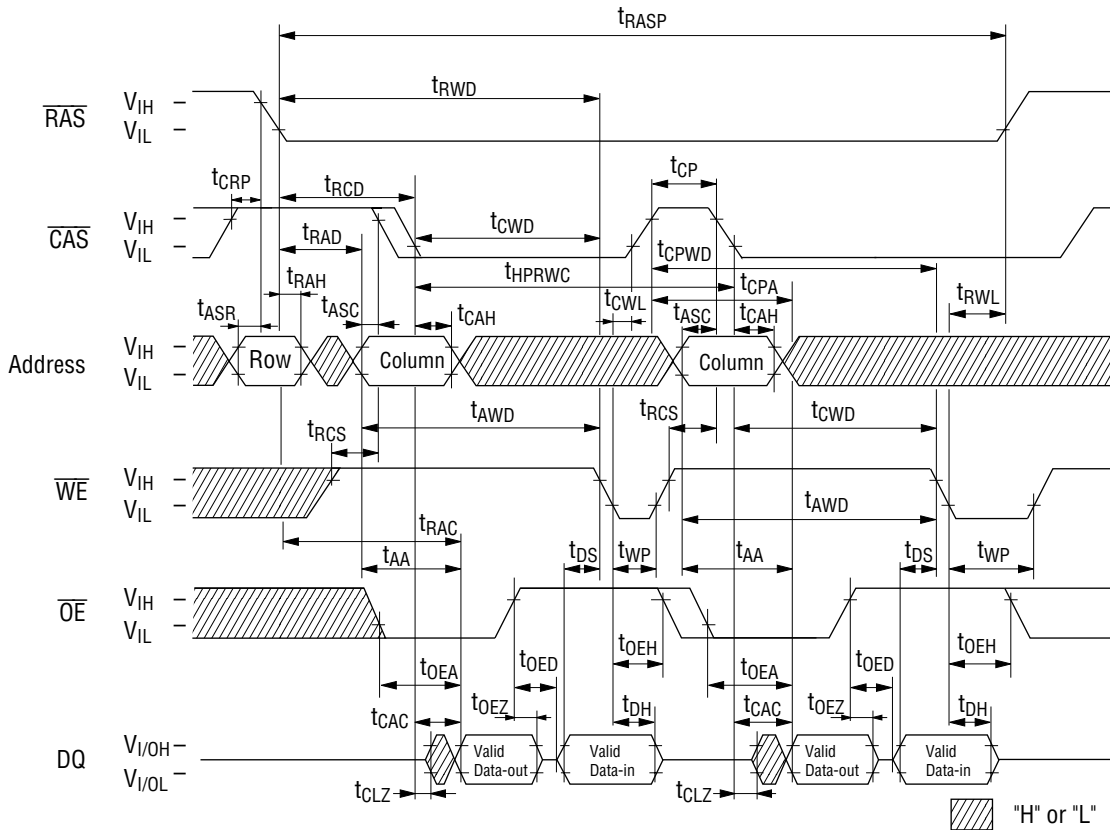
Fast Page Mode Read Cycle (Part-2)



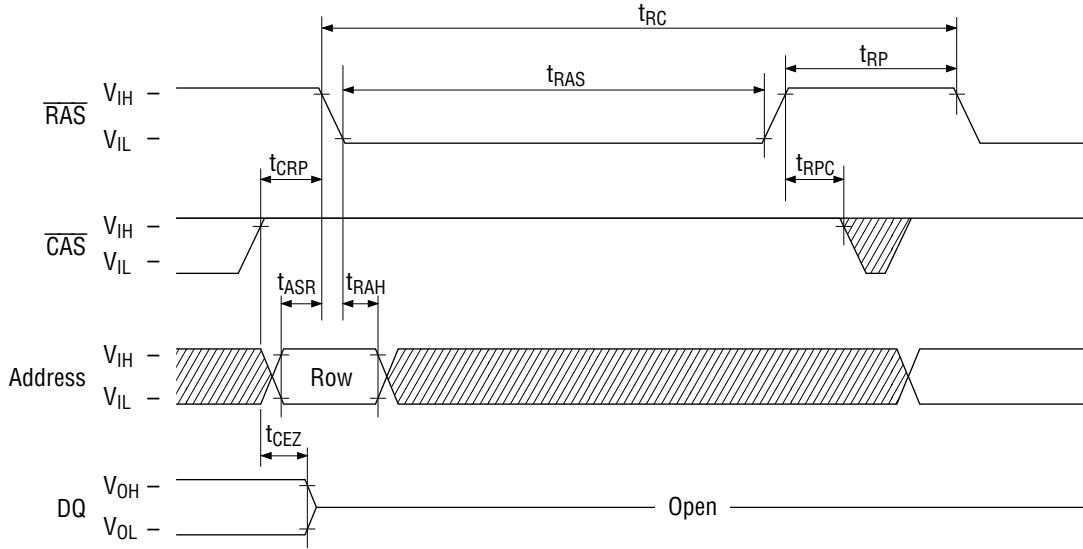
**Fast Page Mode Write Cycle (Early Write)**



**Fast Page Mode Read Modify Write Cycle**

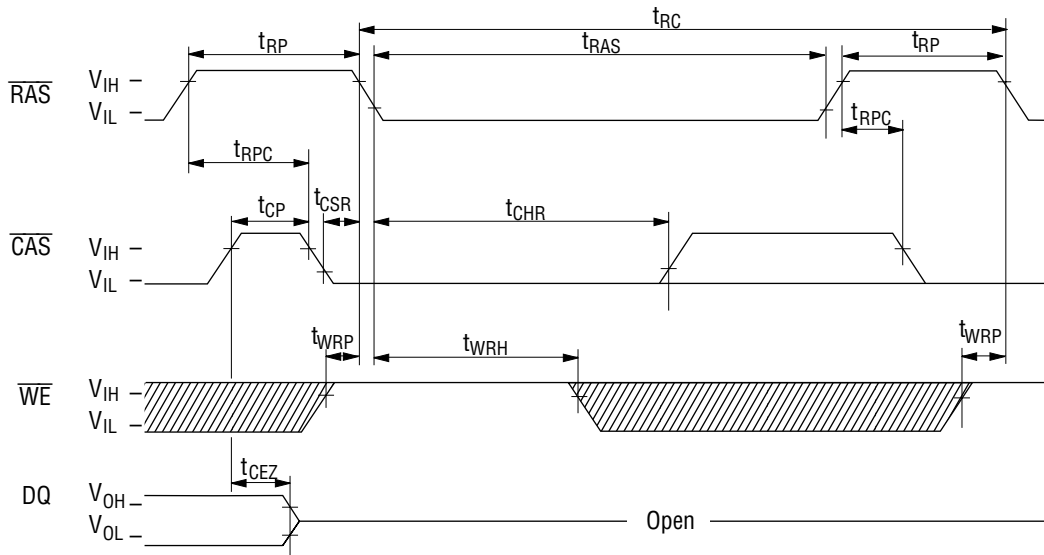


**RAS-Only Refresh Cycle**



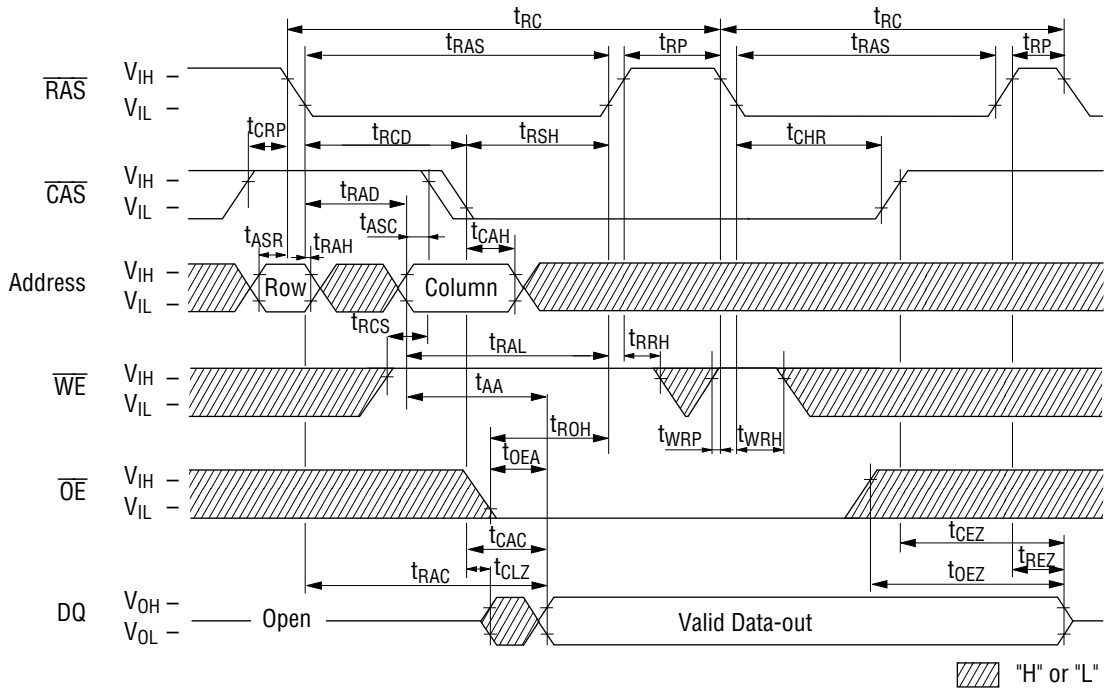
Note:  $\overline{\text{WE}}, \overline{\text{OE}} = \text{"H" or "L"}$   "H" or "L"

**CAS before RAS Refresh Cycle**

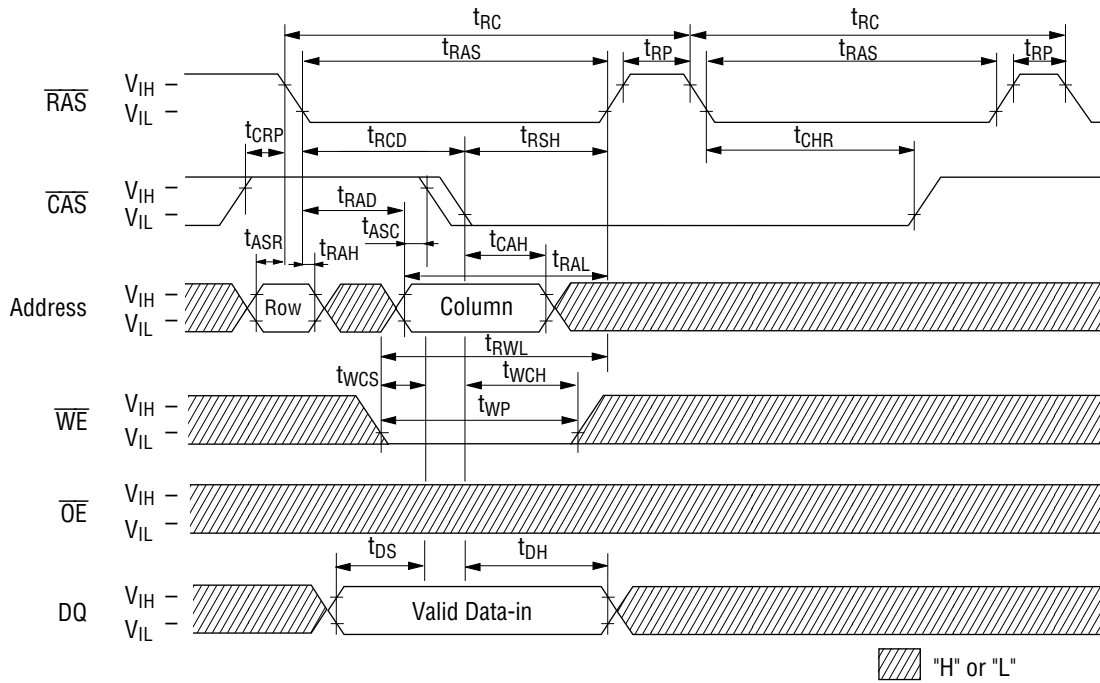


Note:  $\overline{\text{OE}}, \text{Address} = \text{"H" or "L"}$   "H" or "L"

Hidden Refresh Read Cycle

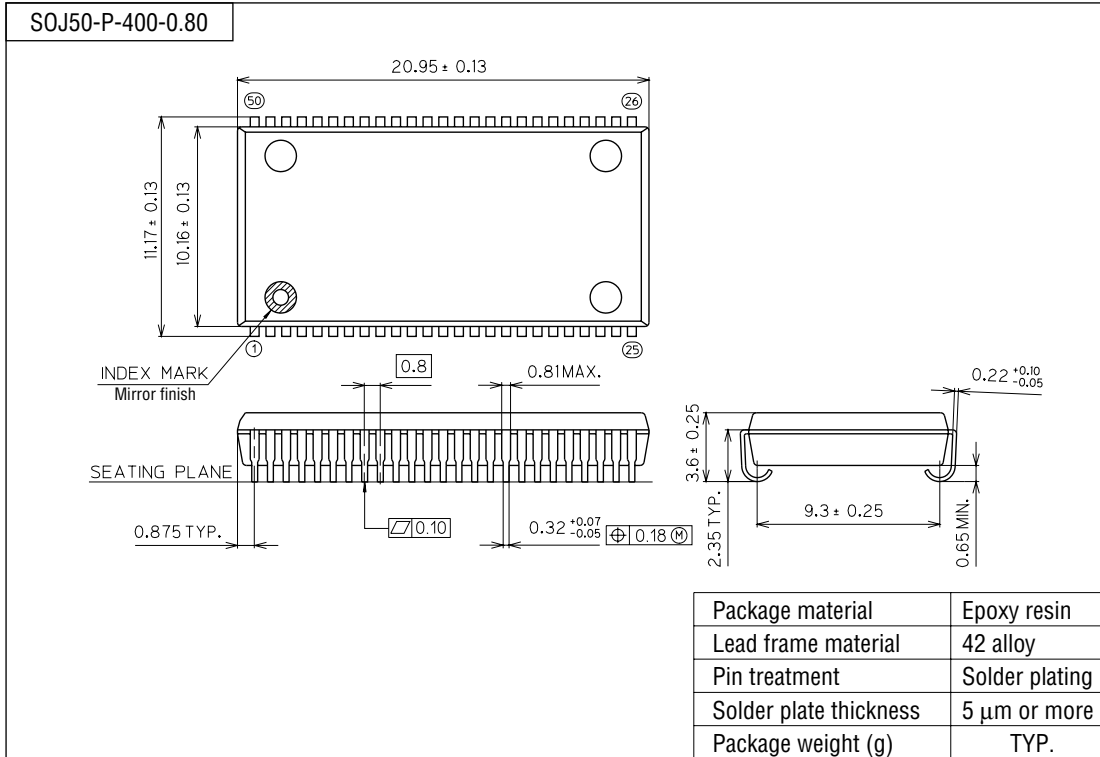


Hidden Refresh Write Cycle



**PACKAGE DIMENSIONS**

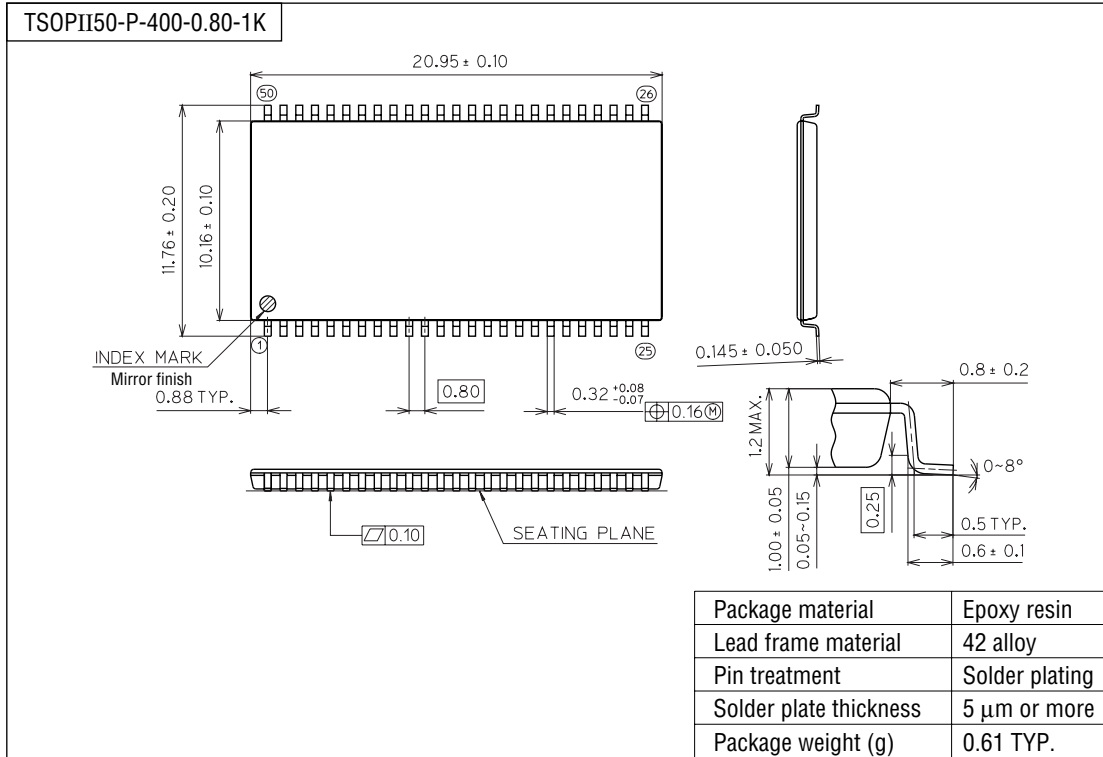
(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)



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