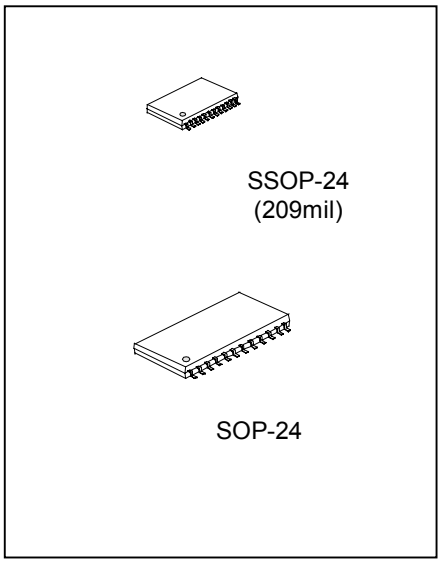
8-BIT 8-CH MULTIPLYING D-A CONVERTER WITH BUFFER AMPLIFIERS



GENERAL DESCRIPTION

The UTC M62364 is a CMOS 8-bit, 8-ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by the simple three-wiring method (DI,CLK,LD).

The output buffer amplifiers operating in AB-class has both sinking and driving capabilities of 1.0mA or more and can operate in a whole supply range from V_{DD} to GND.

The IC is suitable for a use in automatic adjustment applications in conjunction with a MCU by utilizing the terminal Do for a cascading connection.

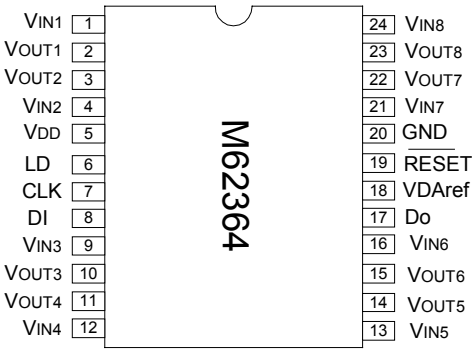
FEATURES

*Three-wiring serial data transmission
*Doubled precision 8-ch D/A converter employing an R-2R with higher-order segment method
*8 buffer amplifiers operating in a whole supply voltage range from V_{DD} to GND
*4-quadrant multiplication

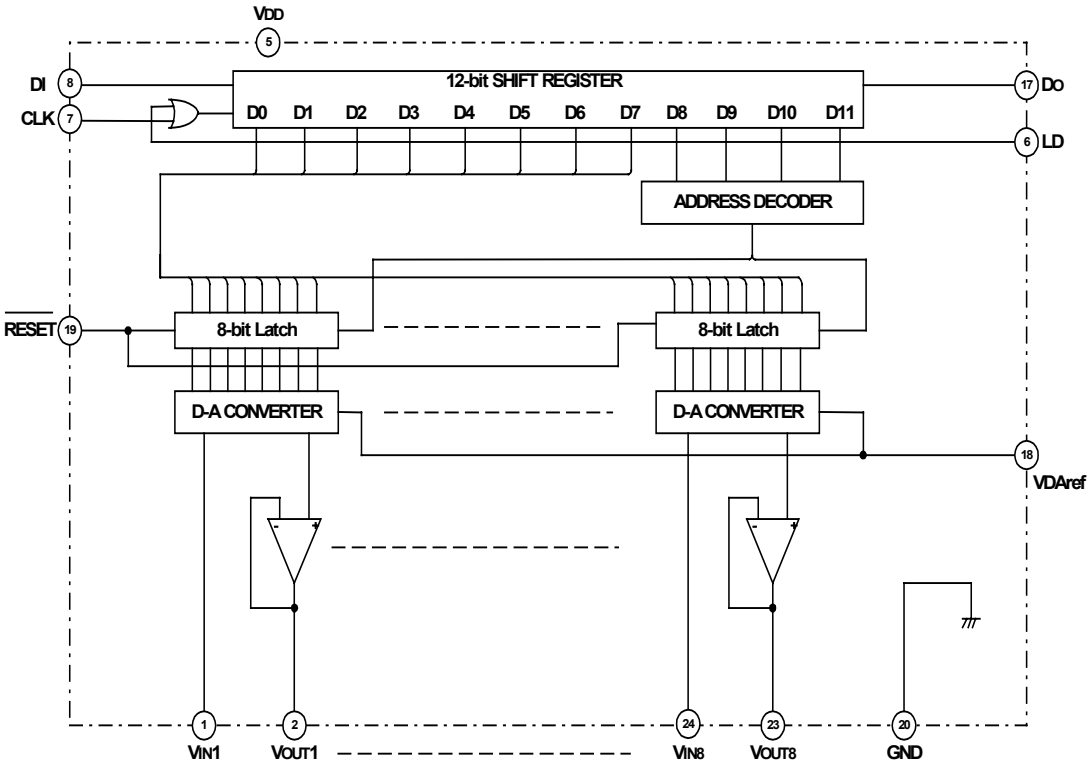
APPLICATION

Digital to analog conversion for consumer and industrial equipment. Gain setting and automatic adjustment of display-monitor and CTV.

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM

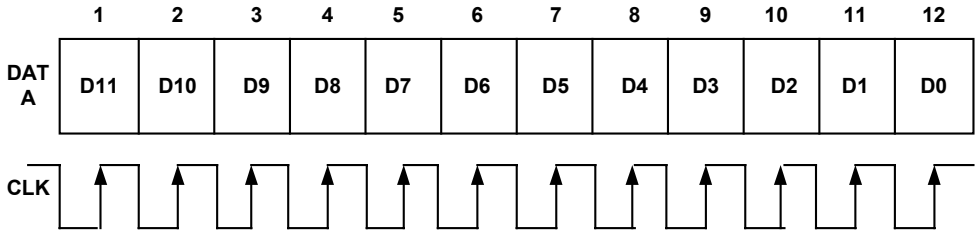


EXPLANATION OF TERMINALS

PIN No.	Symbol	Function
8	DI	Serial data input
17	Do	Serial data output
7	CLK	Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge of the clock
6	LD	A low state enables data loading to the 12-bit shift register. During a rising edge of LD, the data will be loaded to the output register
19	$\overline{\text{RESET}}$	Reset 8-bit latches
2	V_{OUT1}	D/A Converter Output with 8-bit resolution
3	V_{OUT2}	
10	V_{OUT3}	
11	V_{OUT4}	
14	V_{OUT5}	
15	V_{OUT6}	
22	V_{OUT7}	
23	V_{OUT8}	
5	V_{DD}	Power Supply
20	GND	Ground
1	V_{IN1}	D/A Converter Input
4	V_{IN2}	
9	V_{IN3}	
12	V_{IN4}	
13	V_{IN5}	
16	V_{IN6}	
21	V_{IN7}	
24	V_{IN8}	
18	VDAref	D/A Converter Reference Voltage Input

DIGITAL FORMAT

***12BIT SERIAL DATA** (LSB)



***DATA ASSIGNMENT**

D0	D1	D2	D3	D4	D5	D6	D7	:DAC DATA

(LSB) (MSB)

D8	D9	D10	D11	:DAC SELECT DATA

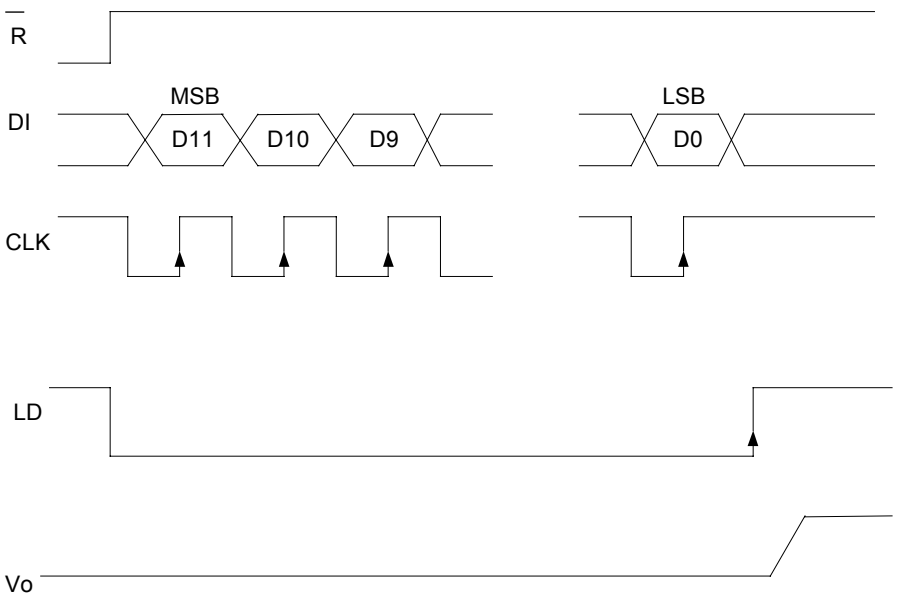
Dac Select Data

D8	D9	D10	D11	Dac Selection
0	0	0	0	Don't Care
0	0	0	1	V_{OUT1} Selection
0	0	1	0	V_{OUT2} Selection
0	0	1	1	V_{OUT3} Selection
0	1	0	0	V_{OUT4} Selection
0	1	0	1	V_{OUT5} Selection
0	1	1	0	V_{OUT6} Selection
0	1	1	1	V_{OUT7} Selection
1	0	0	0	V_{OUT8} Selection
1	0	0	1	Don't Care
1	0	1	0	Don't Care
1	0	1	1	Don't Care
1	1	0	0	Don't Care
1	1	0	1	Don't Care
1	1	1	0	Don't Care
1	1	1	1	Don't Care

*Digital Data Format

D0	D1	D2	D3	D4	D5	D6	D7	DAC OUTPUT
0	0	0	0	0	0	0	0	VDAref
1	0	0	0	0	0	0	0	(VIN-VDAref)/256x1+VDAref
0	1	0	0	0	0	0	0	(VIN-VDAref)/256x2+VDAref
1	1	0	0	0	0	0	0	(VIN-VDAref)/256x3+VDAref
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	1	1	1	1	(VIN-VDAref)/256x255+VDAref

TIMING CHART



*Input data carried out LD signal Low besides CLK signal positive edge.
CLK,LD is keep generally HIGH level.

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	MEASUREMENT CONDITION	VALUE	UNIT
Supply Voltage	V_{DD}		-0.3 ~ +7.0	V
Digital Input Voltage	V_{IND}		-0.3 ~ +7.0	V
Analog Input Voltage	V_{IN}		-0.3 ~ VDD+0.3	V
Analog Output Voltage	V_{OUT}		-0.3 ~ VDD+0.3	V
D-A Reference Voltage	V_{DAref}		-0.3 ~ VDD+0.3	V
Operating Temperature	T_{opr}		-20 ~ +75	°C
Storage Temperature	T_{stg}		-40 ~ +125	°C

ELECTRICAL CHARACTERISTICS

< Ana/Dig Common Part > (V_{DD}=5V±10% , $V_{DD}\geq V_{IN}$,GND,V_{DAref}=0V,Ta=-20~85°C unless otherwise noted)

PARAMETER	SYMBOL	MEASUREMENT CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Supply Current	I_{DD}	CLK=1MHz,Vcc=3V,IAO=0μ A			3.5	mA

< Digital Part > (V_{DD}=5V±10% , $V_{DD}\geq V_{IN}$,GND,V_{DAref}=0V,Ta=-20~85°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Input Leak Current	I_{ILK}	V_{IN}=0 ~V_{DD}	-10		10	μ A
Digital Input “Low” Voltage	I_{IL}				0.2 V_{DD}	V
Digital Input “High” Voltage	I_{IH}		0.8V_{DD}			V
Do Terminal Output “Low” Voltage	V_{OL}	IOL=2.5mA			0.4	V
Do Terminal Output “High” Voltage	V_{OH}	IOH=-400μ A	$V_{DD-0.4}$			V

< Analog Part > (V_{DD}=5V±10% , $V_{DD}\geq V_{IN}$,GND,V_{DAref}=0V,Ta=-20~85°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Input Current	I_{IN}	V_{IN}=3V,VDAref=0V, *Proportional to max. input current condition(V_{IN}-VDAref) and digital data of each channels.			0.18	mA
D-A Reference Input Current	I_{DAref}	V_{IN}=3V,VDAref=0V, *Proportional to max. input current condition(V_{IN}-VDAref) and digital data of each channels	-1.44			mA
Resolution	RES	V_{DD}=2.61V,VDAref=0.050V (10mV/1LSB) Without Load(I_{AO}=±0)		8		bit
Differential Nonlinearity	DNL		-1		1	LSB
Nonlinearity	NL		-1.5		1.5	LSB
Buffer Amplifier Output Voltage Range	V_{AO}	I_{AO}=±100μ A	0.1		Vcc-0.1	V
		I_{AO}=±500μ A	0.2		Vcc-0.2	
Buffer Amplifier Output Current Range	I_{AO}	Upper Saturation Voltage=0.4V Lower Saturation Voltage=0.4V	-1		1	mA

PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
utput Capacitative Load	Co				0.1	μ F
Buffer Amplifier Output Impedance	Ro			5		Ω

< AC Characteristics > (V_{DD}=5V±10% , $V_{DD}\geq V_{IN}$,GND,V_{DAref}=0V,Ta=-20~85°C unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDUCTION	LIMIT			UNIT
			MIN	TYP	MAX	
Clock “L” Pulse Width	t_{CKL}		200			ns
Clock “H” Pulse Width	t_{CKH}		200			ns
Clock Rise Time	t_{CR}				200	ns
Clock Fall Time	t_{CF}					
Data Set Up Time	t_{DCH}		60			ns
Data Hold Time	t_{CHD}		100			ns
LD Set Up Time	t_{CHL}		200			ns
LD Hold Time	t_{LDC}		100			ns
LD “H” Pulse Duration Time	t_{LDH}		100			ns
Data Output Delay Time	t_{Do}	C_L=100pF	70		350	ns
D-A Output Setting Time	t_{LDD}	$C_L\leq$ 100pF,V_{AO}:0.1 < = > 2.6V This Time Until The Output Becomes The final Value Of 1/2 LSB			300	μ s

TIMING CHART