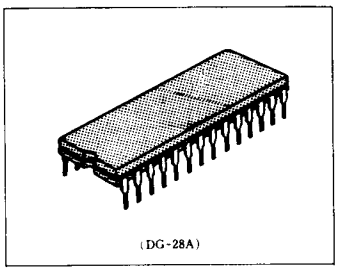
4096-wrod x 4-bit Fully Decoded Random Access Memory

The HM100484 is ECL 100k compatible, 4096-words by 4-bits read/write random access memory developed for high speed systems such as acratch pads and control/buffer storage.



Features

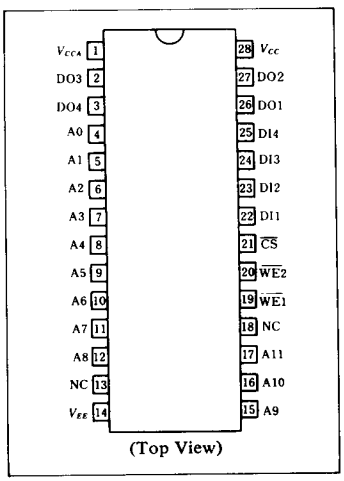
- 4096-word x 4-bits organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 7ns (min)
- Power dissipation: 630mW
- Output obtainable by wired-OR

Function Table

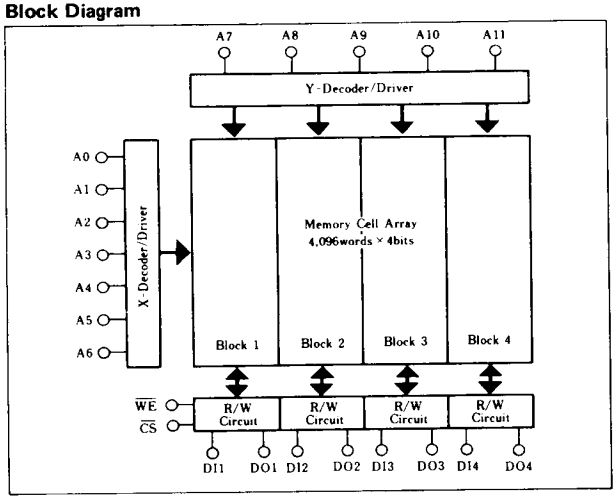
Input			Output	Mode
$\overline{CS}$	$\overline{WE}$	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

Notes) × : Irrelevant
*: Read Out Nonivert

Pin Arrangement



Block Diagram



Note) **The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.**

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to −7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	−30	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Storage Temperature	T_{stg}(Bias)*	−55 to +125	°C

* Under Bias

Electrical Characteristics

DC Characteristics (V_{EE} = −4.5V, R_L = 50Ω to −2.0V, Ta = 0 to +85°C, air flow exceeding 2m/sec)

item	Symbol	min(B)	typ	max(A)	Unit	Test Condition
Output Voltage	V_{OH}	−1025	−955	−880	mV	V_{in} = V_{IHA} or V_{ILB}
	V_{OL}	−1810	−1715	−1620	mV	
Output Threshold Voltage	V_{OHC}	−1035	—	—	mV	V_{in} = V_{IHB} or V_{ILA}
	V_{OLC}	—	—	−1610	mV	
Input Voltage	V_{IH}	−1165	—	−880	mV	Guaranteed Inputs Voltage
	V_{IL}	−1810	—	−1475	mV	High/Low for All Inputs
Input Current	I_{IH}	—	—	220	μA	V_{in} = V_{IHA}
	I_{IL}	0.5	—	170	μA	$\overline{CS}$ — V_{in} = V_{ILB}
		−50	—	—		Others
Supply Current	I_{EE}	−180	—	—	mA	All Inputs and Outputs Open

AC Characteristics (V_{EE} = −4.5V ±5%, Ta = 0 to +85°C, air flow exceeding 2m/sec)

Read Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Chip Select Access Time	t_{ACS}	—	—	6	ns	
Chip Select Recovery Time	t_{RCS}	—	—	6	ns	
Address Access Time	t_{AA}	—	—	10	ns	

Write Mode

Item	Symbol	min	typ	max	Unit	Test Condition
Write Pulse Width	t_W	7	—	—	ns	t_{WSA} = t_{WSA} min
Data Setup Time	t_{WSD}	1	—	—	ns	
Data Hold Time	t_{WHD}	2	—	—	ns	
Address Setup Time	t_{WSA}	1	—	—	ns	t_W = t_W min
Address Hold Time	t_{WHA}	2	—	—	ns	
Chip Select Setup Time	t_{WSCS}	1	—	—	ns	
Chip Select Hold Time	t_{WHCS}	2	—	—	ns	
Write Disable Time	t_{WS}	—	—	6	ns	
Write Recovery Time	t_{WR}	—	—	12	ns	

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Rise/Fall Time

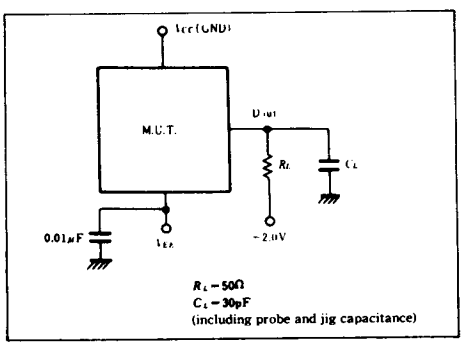
Item	Symbol	min	typ	max	Unit	Test Condition
Output Rise Time	t_r	—	2	—	ns	
Output Fall Time	t_f	—	2	—	ns	

Capacitance

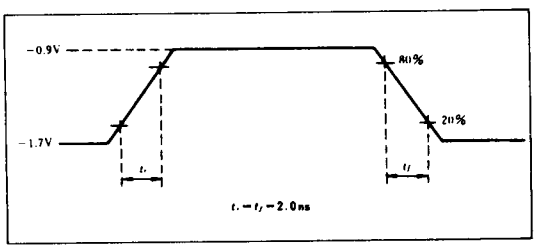
Item	Symbol	min	typ	max	Unit	Test Condition
Input Capacitance	Cin	—	3	—	pF	
Output Capacitance	Cout	—	5	—	pF	

Test Circuit and Waveforms

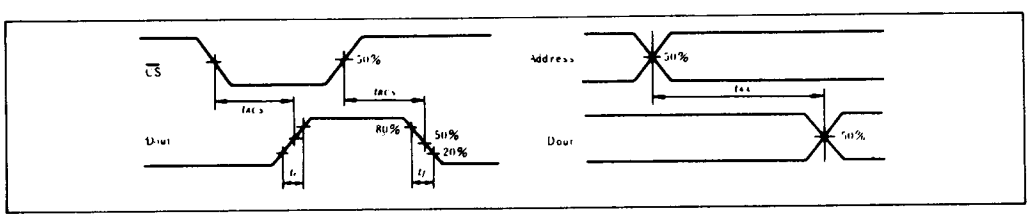
Loading Condition



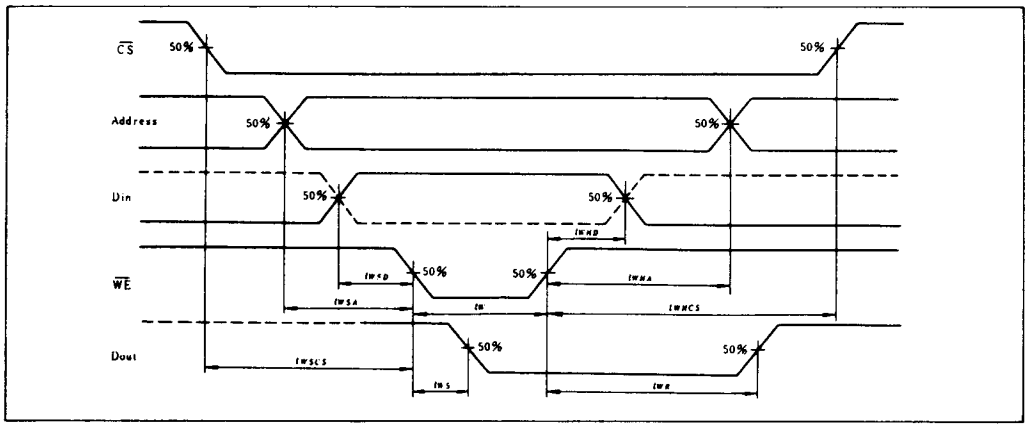
Input Pulse



Read Mode



Write Mode



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