
HD74HC590

8-bit Binary Counter/Register (with 3-state outputs)

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Description

This device each contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{\text{CCLR}}$ and a count enable input $\overline{\text{CCKEN}}$. For cascading a ripple carry output $\overline{\text{RCO}}$ is provided. Expansion is easily accomplished by tying $\overline{\text{RCO}}$ of the first stage to $\overline{\text{CCKEN}}$ of the second stage, etc.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register, Internal circuitry prevents clocking from the clock enable.





Features

- High Speed Operation: t_{pd} (RCK to Q) = 18.5 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max ($T_a = 25^\circ\text{C}$)

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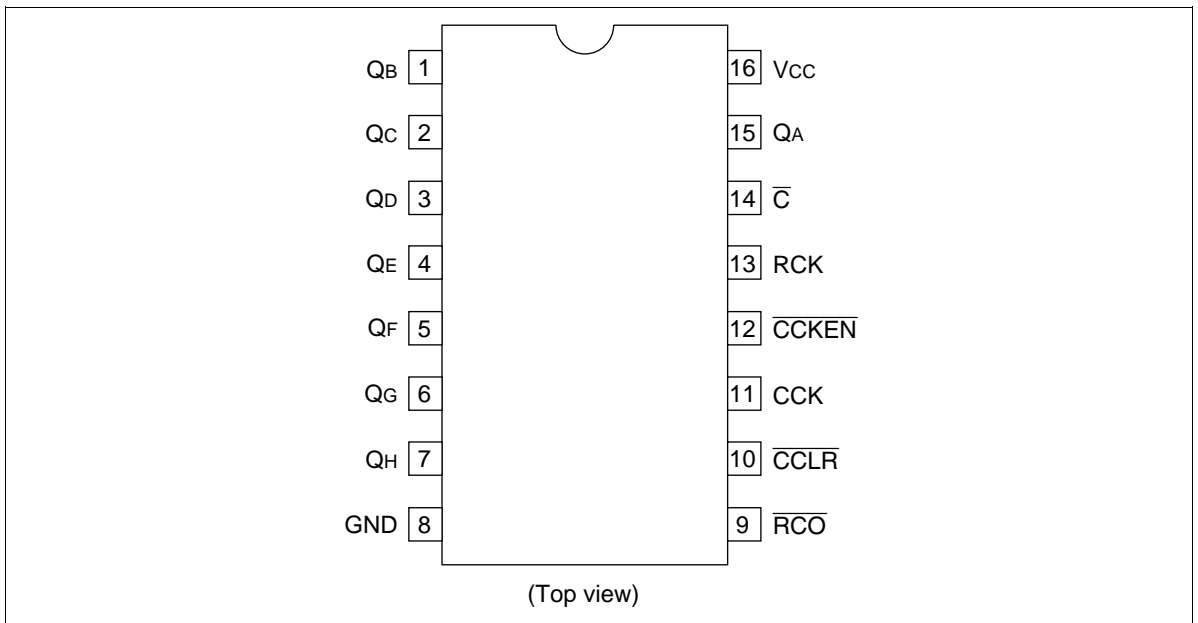
Function Table

Inputs

\overline{G}	RCK	\overline{CCLR}	\overline{CCKEN}	CCK	Function
H	X	X	X	X	Q output disabled
L	X	X	X	X	Q output enabled
X		X	X	X	Contents of counter stored to register
X		X	X	X	No change in register
X	X	L	X	X	Counter clear
X	X	H	L		Count up
X	X	H	L		No count
X	X	H	H	X	No count

$$\overline{RCO} = QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH' \cdot (\overline{CCKEN}) \quad (QA' \text{ to } QH': \text{ Output of Internal Counter})$$

Pin Arrangement

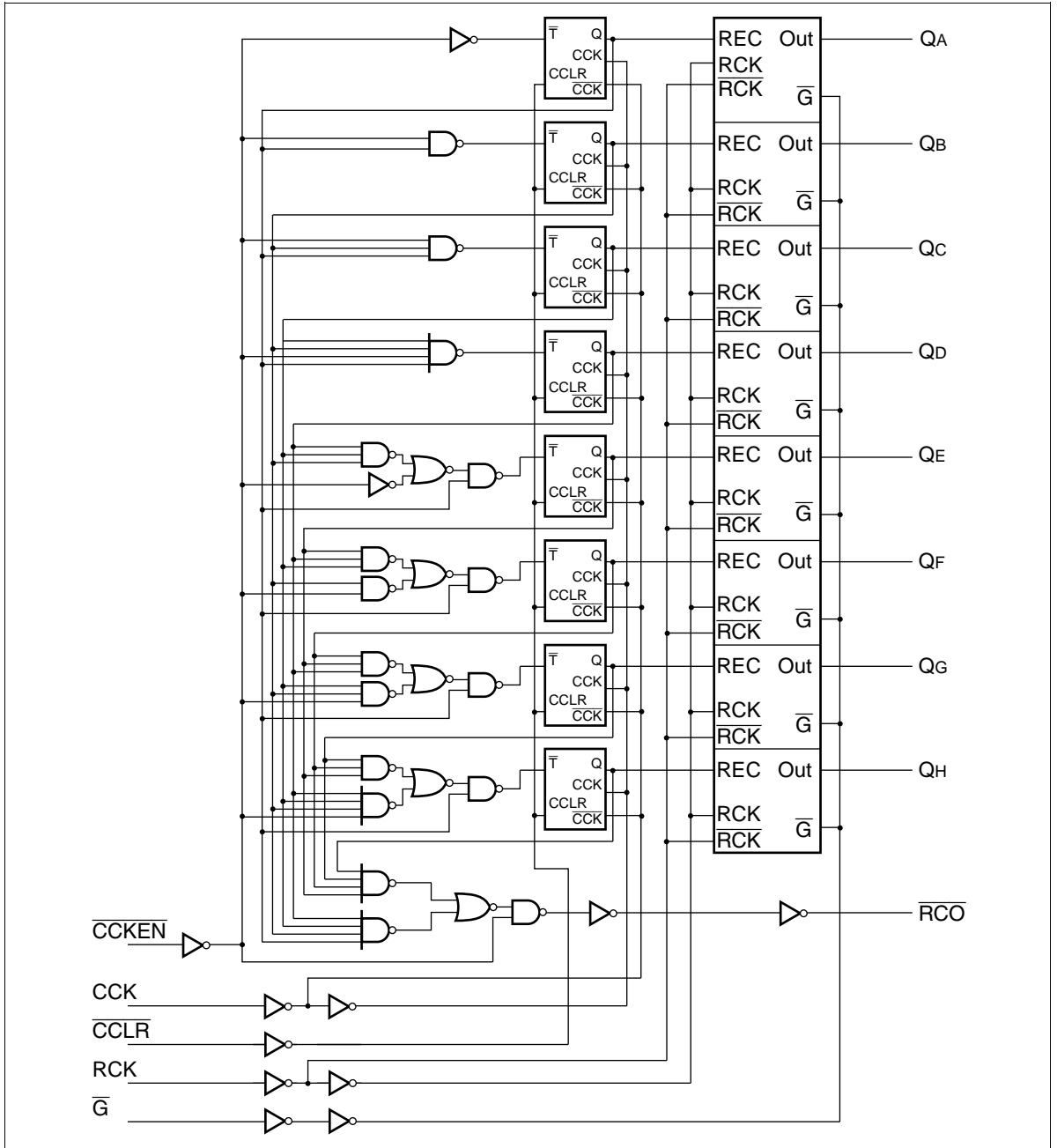


Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Output current	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power Dissipation per package	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

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Logic Diagram



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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V _{IL}	2.0	—	—	0.5	—	0.5	V			
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Q _A to Q _H V _{in} = V _{IH} or V _{IL}	I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—				
		6.0	5.9	6.0	—	5.9	—				
		4.5	4.18	—	—	4.13	—				I _{OH} = -6 mA
		6.0	5.68	—	—	5.63	—				I _{OH} = -7.8 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Q _A to Q _H V _{in} = V _{IH} or V _{IL}	I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33				I _{OL} = 6 mA
		6.0	—	—	0.26	—	0.33				I _{OL} = 7.8 mA
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	\overline{RCO} V _{in} = V _{IH} or V _{IL}	I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—				
		6.0	5.9	6.0	—	5.9	—				
		4.5	4.18	—	—	4.13	—				I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—				I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	\overline{RCO} V _{in} = V _{IH} or V _{IL}	I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33				I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33				I _{OL} = 5.2 mA
Off-state output current	I _{OZ}	6.0	—	—	±0.5	—	±5.0	μA	V _{in} = V _{IH} or V _{IL} , V _{out} = V _{CC} or GND		
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	V _{in} = V _{CC} or GND		
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	V _{in} = V _{CC} or GND, I _{out} = 0 μA		

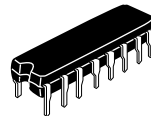
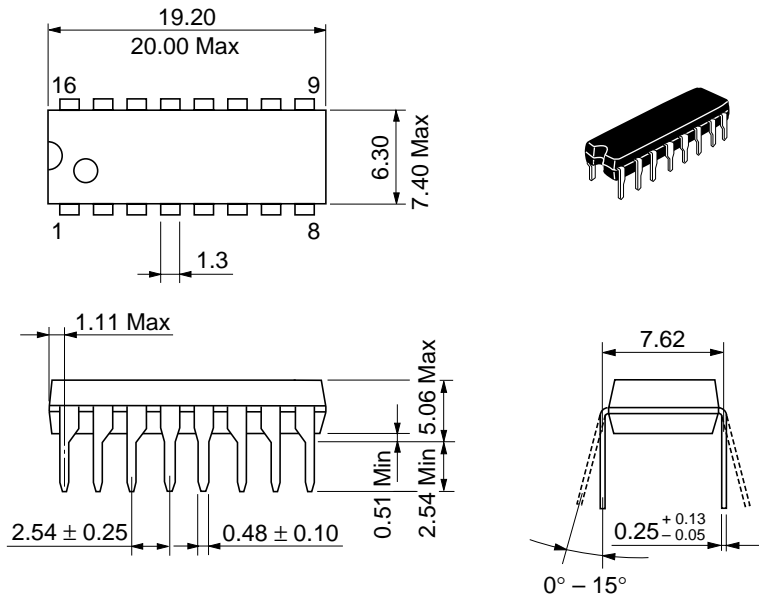
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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

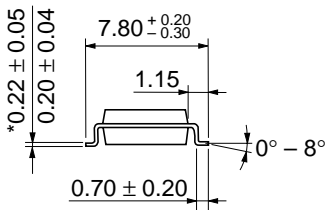
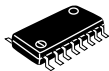
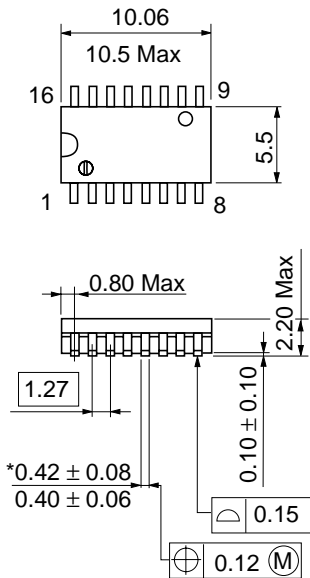
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz		
		4.5	—	—	25	—	20			
		6.0	—	—	29	—	24			
Propagation delay time	t_{PLH}	2.0	—	—	200	—	250	ns	$\overline{\text{CCK}}$ to $\overline{\text{RCO}}$	
		4.5	—	18	40	—	50			
		6.0	—	—	34	—	43			
	t_{PLH}	2.0	—	—	250	—	315	ns	$\overline{\text{CCLR}}$ to $\overline{\text{RCO}}$	
		4.5	—	17	50	—	63			
		6.0	—	—	43	—	54			
	t_{PLH}	2.0	—	—	200	—	250	ns	RCK to Q	
		4.5	—	18	40	—	50			
		6.0	—	—	34	—	43			
	Output enable time	t_{ZL}	2.0	—	—	150	—	190	ns	
			4.5	—	16	30	—	39		
			6.0	—	—	26	—	33		
Output disable time	t_{LZ}	2.0	—	—	150	—	190	ns		
		4.5	—	17	30	—	38			
		6.0	—	—	26	—	33			
Pulse width	t_w	2.0	80	—	—	100	—	ns		
		4.5	16	6	—	20	—			
		6.0	14	—	—	17	—			
Removal time	t_{rem}	2.0	5	—	—	5	—	ns	$\overline{\text{CCLR}}$ to CCK	
		4.5	5	—	—	5	—			
		6.0	5	—	—	5	—			
Setup time	t_{su}	2.0	100	—	—	125	—	ns	$\overline{\text{CCKEN}}$ to CCK	
		4.5	20	-3	—	25	—			
		6.0	17	—	—	21	—			
	t_{su}	2.0	200	—	—	250	—	ns	CCK to RCK	
		4.5	40	10	—	50	—			
		6.0	34	—	—	43	—			

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns) (cont)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Hold time	t_h	2.0	5	—	—	5	—	ns	$\overline{\text{CCKEN}}$ to CCK
		4.5	5	—	—	5	—		CCK to RCK
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns	Q
	t_{THL}	4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
	t_{TLH}	2.0	—	—	75	—	95	ns	$\overline{\text{RCO}}$
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

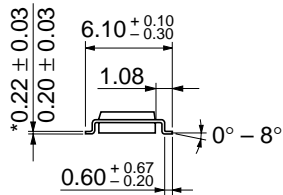
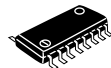
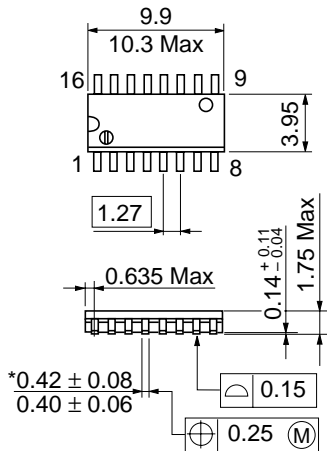


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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