EXAR

XR-16C452

T-75-37-05

Dual Universal Asynchronous Receiver and Transmitter with Parallel Printer Port

GENERAL DESCRIPTION

The XR-16C452 is a dual universal asynchronous receiver and transmitter with a bidirectional CENTRONICS type parallel printer port. An internal programmable baud rate generator is provided to select transmit and receive clock rates from 50Hz to 448kHz. The XR-16C452 is fabricated on an advanced 1.2µm CMOS process to achieve low power consumption and high speed operation.

FEATURES

Pin-to-pin and functionally compatible to VL16C452
Fully compatible with all new bidirectional PS/2 printer port registers
Modem control signals (CTS~, RTS~, DSR~, DTR~, RI~, CD~)
Programmable character lengths (5, 6, 7, 8)
Even, odd, or no parity bit generation and detection
Status report register
Independent transmit and receive control
TTL compatible inputs, outputs
Direct replacement of logic for PC/XT/AT
High data transfer rate 448 kHz transmit/receive operation with 7.372MHz external clock source
Bidirectional CENTRONICS printer port
Enhanced current drive capability on all I/O ports

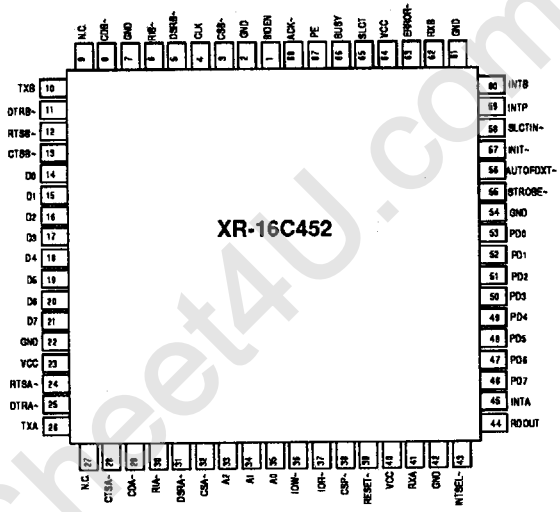
APPLICATIONS

Dual RS232 receiver and/or transmitter
Serial to parallel / parallel to serial converter Modem handshaking
CENTRONICS printer port
IBM PS/2 bidirectional printer port
External bidirectional I/O
IBM PC/XT/AT upgrade printer port

ABSOLUTE MAXIMUM RATINGS

Operating Supply Range	5 Volts ± 5%
Voltage at any Pin	GND-0.3 V to VCC+0.3 V
Operating Temperature	0° C to +70° C
Storage Temperature	-40° C to +150° C
Package Dissipation	500 mW

PIN ASSIGNMENT



ORDERING INFORMATION

Part number	Package	Operating Temperature
XR-16C452CJ	PLCC	0° C to +70° C

SYSTEM DESCRIPTION

The XR-16C452 is an improved version of the VL16C452 with higher operating speed and lower access time. The XR-16C452 performs the parallel to serial/serial to parallel conversion on the data characters received from the CPU or the MODEM. The XR-16C452 also provides the user with a bidirectional parallel data port that fully supports the parallel CENTRONICS type printer. The on chip status registers will provide the error conditions, as well as the type and status of the transfer operations being performed. The XR-16C452 also has a complete MODEM control capability, and a processor interrupt system. The latter may be software tailored to the user's requirements there-by allowing the user to minimize the computing time required to service the communications link. The XR-16C452 can interface easily to most popular microprocessors and communications link faults can be detected with an internal loop-back capability.

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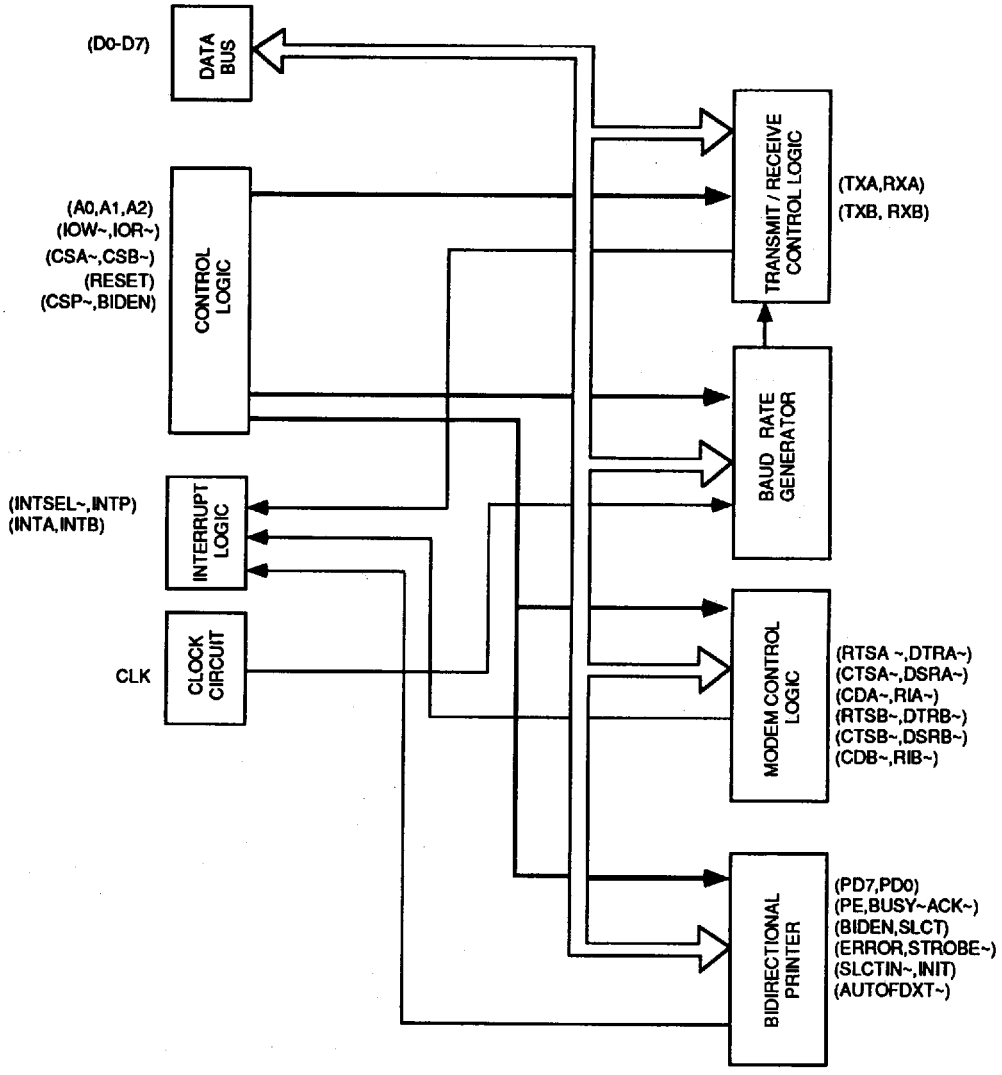

Figure 1. Block Diagram

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25° C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
VILCK	Clock input low level	-0.5		0.6	V	
VIHCK	Clock input high level	3.0		VCC	V	
VIL	Input low level	-0.5		0.8	V	
VIH	Input high level	2.2		VCC	V	
VOL	Output low level			0.4	V	IOL= 6.0 mA D7-D0 IOL= 20.0 mA PD7-PD0 IOL= 10 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ IOL= 6.0 mA on all other outputs
VOH	Output high level	2.4			V	IOH= -6.0 mA D7-D0 IOH= -12.0 mA PD7-PD0 IOH= -0.2 mA SLCTIN~, INIT~,STROBE~, AUTOFDXT~ IOH= -6.0 mA on all other outputs
ICC	Avg power supply current			12	mA	
IIL	Input leakage			±10	µA	
ICL	Clock leakage			±10	µA	

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AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
T1	Clock high pulse duration	55			ns	
T2	Clock low pulse duration	55			ns	External clock
T3	Clock rise/fall time					
T12	Address hold time from IOW~	20			ns	
T13	IOW~ delay from address	25			ns	
T14	IOW~ delay from chip select	10			ns	
T15	IOW~ strobe width	50			ns	
T16	Chip select hold time from IOW~	5			ns	
T17	Write cycle delay	55			ns	
TW	Write cycle=T15+T17	135			ns	
T18	Data setup time	20			ns	
T19	Data hold time	25			ns	
T20	Address hold time from IOR~	0			ns	
T21	IOR~ delay from address	10			ns	
T22	IOR~ delay from chip select	10			ns	
T23	IOR~ strobe width	75			ns	
T24	Chip select hold time from IOR~	0			ns	
T25	Read cycle delay	50			ns	
TR	Read cycle=T23+T25	135			ns	
T26	Delay from IOR~ to data			75	ns	100 pF load
T27	IOR~ to floating data delay	0		50	ns	100 pF load

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AC ELECTRICAL CHARACTERISTICS

Test Conditions: TA=25°C, VCC=5.0 V ±5% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		min	typ	max		
MODEM CONTROL						
T28	Delay from IOW~ to output			50	ns	100 pF load
T29	Delay to set interrupt from MODEM input			70	ns	100 pF load
T30	Delay to reset interrupt from IOR			70	ns	100 pF load
RECEIVER						
T31	Delay from stop to set interrupt			1 Rclk	ns	100 pF load
T32	Delay from IOR~ to reset interrupt			200	ns	100 pF load
TRANSMITTER						
T33	Delay from initial INT reset to transmit start	8		24		
T34	Delay from stop to interrupt			100	ns	
T35	Delay from IOW~ to reset interrupt			125	ns	
T36	Delay from initial Write to interrupt	16		24		
T37	Delay from IOR~ to reset interrupt			75	ns	100 pF load
PRINTER PORT						
T38	Delay from rising IOW~ to output data.	5			ns	
T39	ACK~ pulse width	75			ns	
T40	PD7 - PD0 setup time	10			ns	
T41	PD7 - PD0 hold time	25			ns	
T42	Delay from ACK~ low to interrupt high.	5			ns	
T43	Delay from IOR~ to reset interrupt	5			ns	

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PIN DESCRIPTION

Pin#	Symbol	Type	Description
1	BIDEN	I	**Printer Direction Select.** A high puts the parallel port in the software controlled mode (input / output). A low puts the parallel port in the out mode.
3	CSB~	I	**Chip Select B (active low).** A low at this pin (while CSA~ and CSP~ =1) will enable the UARTB / CPU data transfer operation.
4	CLK	I	**External Clock Input.** An external clock can be used to clock the internal circuit and the baud rate generator for custom and standard transmission rates.
5	DSRB~	I	**Data Set Ready B (active low).** A low on this pin indicates that MODEM B is ready to exchange data with UARTB.
6	RIB~	I	**Ring Detect B Indicator (active low).** A low on this pin indicates that MODEM B has received a ringing signal from the telephone line.
8	CDB~	I	**Carrier Detect B (active low).** A low on this pin indicates that carrier has been detected by the MODEM B.
10	TXB	O	**Serial Data Output B.** The serial data is transmitted via this pin with additional start , stop and parity bits. The TXB will be held in mark (high) state during reset, local loop-back mode or when the transmitter is disabled.
11	DTRB~	O	**Data Terminal Ready B (active low).** To indicate that XR-16C452 is ready to receive data. This pin can be controlled via the modem control register (MCRB bit-0). Writing a "1" at the MCRB bit-0 will set the DTRB~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
12	RTSB~	O	**Request to Send B (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRB bit-1) will set this pin to low state. After the reset this pin will be set to high.
13	CTSB~	I	**Clear to Send B (active low).** The CTSB~ signal is a MODEM control function input whose conditions can be tested by reading the MSRB BIT-4. CTSB~ has no effect on the transmitter output.
14-21	D0-D7	I/O	**Bidirectional Data Bus.** Eight bit, three state data bus to transfer information to or from the CPU. D0 is the least significant bit (lsb) of the data bus and the first serial data bit to be received or transmitted.
24	RTSA~	O	**Request to Send A (active low).** To indicate that transmitter has data ready to send. Writing a "1" in the modem control register (MCRA bit-1) will set this pin to low state. After the reset this pin will be set to high.

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Pin#	Symbol	Type	Description
25	DTRA~	O	**Data Terminal Ready A (active low).** To indicate that XR-16C452 is ready to receive data. This pin can be controlled via the modem control register (MCRA bit-0). Writing a "1" at the MCRA bit-0 will set the DTRA~ output to low. This pin will be set to high state after writing a "0" to that register or after the reset .
26	TXA	O	**Serial Data Output A.** The serial data is transmitted via this pin with additional start, stop and parity bits. The TXA will be held in mark (high) state during reset, local loop-back mode or when the transmitter is disabled.
28	CTSA~	I	**Clear to Send A (active low).** The CTSA~ signal is a MODEM control function input whose conditions can be tested by reading the MSRA BIT-4. CTSA~ has no effect on the transmitter output.
29	CDA~	I	**Carrier Detect A (active low).** A low on this pin indicates that carrier has been detected by the MODEM A.
30	RIA~	I	**Ring Detect A indicator (active low).** A low on this pin indicates that MODEM A has received a ringing signal from the telephone line.
31	DSRA~	I	**Data Set Ready A (active low).** A low on this pin indicates that MODEM A ready to exchange data with UART A.
32	CSA~	I	**Chip Select A (active low).** A low at this pin (while CSB~ and CSP~ =1) will enable the UARTA / CPU data transfer operation.
33	A2	I	**Address Line 2.** To select internal registers.
34	A1	I	**Address Line 1.** To select internal registers.
35	A0	I	**Address Line 0.** To select internal registers.
36	IOW~	I	**Write Strobe (active low).** A low on this pin will transfer the contents of the CPU data bus to the addressed register.
37	IOR~	I	**Read Strobe (active low).** A low level on this pin will transfer the contents of the XR-16C452 data bus to the CPU.
38	CSP~	I	**Chip Select P (active low).** To enable the XR-16C452 printer operation, this pin has to go low while CSA~ and CSB~ are high.
39	RESET~	I	**Master Reset (active low).** A low on this pin will reset all the outputs and internal registers. The parallel port of the XR-16C452 will be set to mode, the transmitter output and the output receiver input will be disabled during reset time.

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Pin#	Symbol	Type	Description
41	RXA	I	**Serial Data Input A.** The serial information (data) received from MODEM or RS232 to XR-16C452 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode RXA input is disabled from external connection and connected to the TXA output internally.
43	INTSEL~	I	**Interrupt Select (active low).** The external ACK~ can be selected as an interrupt source by tying this pin to GND. Tying this pin to VCC, will set the internal interrupt logic to the latched state, reading the STATUS register will reset the INTP output.
44	RDOUT	O	**Read Select Out.** A high on this pin indicates that the chip is being read by the CPU.
45	INTA	O	**UART A Interrupt Output (three state).** This pin goes high (when enabled by MCRA BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
46-53	PD7-PD0	I/O	**Bidirectional Parallel Ports (three state).** To transfer data in or out of the XR-16C452 parallel port. PD7-PD0 are latched during output mode.
55	STROBE~	I/O	**General Purpose I/O or Strobe Output (open drain, active low).** To transfer latched data to the external peripheral or printer.
56	AUTOFDXT~	I/O	**General Purpose I/O or Line Printer Autofeed (open drain, active low).** To signal the printer for continuous form feed.
57	INIT~	I/O	**General Purpose I/O or Line Printer Initialize (open drain, active low).** To signal the line printer to enter internal initialization routine.
58	SLCTIN~	I/O	**General Purpose I/O or Line Printer Select (open drain, active low).** To select the line printer.
59	INTP	O	**Printer Interrupt Output (active high).** To signal the state of the printer port.
60	INTB	O	**UART B Interrupt Output (three state).** This pin goes high (when enabled by MCRB BIT-3) whenever a receiver error, receiver data available, transmitter empty or modem status condition flag is detected.
62	RXB	I	**Serial Data Input B.** The serial information (data) received from MODEM or RS232 to XR-16C452 receive circuit. A mark (high) is logic one and a space (low) is logic zero. During the local loopback mode the RXB input is disabled from external connection and connected to the TXB output internally.
63	ERROR~	I	**General Purpose Input or Line Printer Error (active low).** This is an output from the printer to indicate an error by holding it low during error condition.

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Pin#	Symbol	Type	Description
65	SLCT	I	**General Purpose Input or Line Printer Selected (active high).** This is an output from the printer to indicate that the line printer has been selected.
66	BUSY	I	**General Purpose Input or Line Printer Busy (active high).** An output from the printer to indicate printer is not ready to accept data.
67	PE	I	**General Purpose Input or Line Printer Paper Empty (active high).** An output from the printer to indicate out of paper.
68	ACK~	I	**General Purpose Input or Line Printer Acknowledge (active low).** An output from the printer to indicate that data has been accepted successfully.
2,7,22 42,54,61	GND	O	**Signal and Power Ground.** All pins must be tied to ground.
23,40, 64	VCC	I	**Power Supply Input.** All pins must be tied to supply voltage.

PROGRAMMING TABLE

CSB	CSA	DLAB	A2	A1	A0	READ MODE	WRITE MODE
1	0	0	0	0	0	Receive Holding Register A	Transmit Holding Register A
1	0	0	0	0	1		Interrupt Enable Register A
1	0	x	0	1	0	Interrupt Status Register A	
1	0	x	0	1	1		Line Control Register A
1	0	x	1	0	0		Modem Control Register A
1	0	x	1	0	1	Line Status Register A	
1	0	x	1	1	0	Modem Status Register A	
1	0	x	1	1	1	Scratchpad Register A	Scratchpad Register A
1	0	1	0	0	0		LSB of Divisor Latch A
1	0	1	0	0	1		MSB of Divisor Latch A
0	1	0	0	0	0	Receive Holding Register B	Transmit Holding Register B
0	1	0	0	0	1		Interrupt Enable Register B
0	1	x	0	1	0	Interrupt Status Register B	
0	1	x	0	1	1		Line Control Register B
0	1	x	1	0	0		Modem Control Register B
0	1	x	1	0	1	Line Status Register B	
0	1	x	1	1	0	Modem Status Register B	
0	1	x	1	1	1	Scratchpad Register B	Scratchpad Register B
0	1	1	0	0	0		LSB of Divisor Latch B
0	1	1	0	0	1		MSB of Divisor Latch B

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REGISTER FUNCTIONAL DESCRIPTIONS

Transmit and Receive Holding Register

The serial transmitter section consists of a Transmit Hold Register A/B and Transmit Shift Register A/B. The status of the transmit hold register is provided in the Line Status Register A/B. Writing to this register will transfer the contents of the data bus (D7-D0) to the transmit holding register A/B whenever the transmitter holding register A/B or transmitter shift register A/B is empty. The transmit holding register empty A/B flag will be set to "1" when the transmitter is empty or data is transferred to the transmit shift register A/B. Note that a write operation should be performed when the transmit holding register empty flag is set.

On the falling edge of the start bit, the receiver internal counter will start to count 7 1/2 clocks (16x clock) which is the center of the start bit. The start bit is valid if the RXA/B is still low at the mid-bit sample of the start bit. Verifying the start bit prevents the receiver from assembling a false data character due to a low going noise spike on the RXA/B input. Receiver status codes will be posted in the Line Status Register A/B.

INTERRUPT ENABLE REGISTER

The Interrupt Enable Register A/B masks the incoming interrupts from receiver ready, transmitter empty, line status and modem status registers to the INTA/B output pin.

IER BIT-0:
0=disable receiver ready interrupt
1=enable receiver ready interrupt

IER BIT-1:
0=disable transmitter empty interrupt
1=enable transmitter empty interrupt

IER BIT-2:
0=disable receiver line status interrupt
1=enable receiver line status interrupt

IER BIT-3:
0=disable modem status register interrupt
1=enable modem status register interrupt

IER BIT 7-4:
All these bits are set to logic zero.

INTERRUPT STATUS REGISTER

The XR-16C452 provides four level prioritized interrupt conditions to minimize software overhead during data character transfers. The Interrupt Status Register A/B provides the source of the interrupt in prioritized manner. During the read cycle, the XR-16C452 provides the highest interrupt level to be serviced by the CPU. No other interrupts are acknowledged until the particular interrupt has been serviced. The following are the prioritized interrupt levels:

ISR BIT-0:
0=an interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine
1=no interrupt pending

ISR BIT 1-2:
Logical combination of these bits, provides the highest priority interrupt pending.

ISR BIT 3-7:
These bits are not used and are set to zero.

LINE CONTROL REGISTER

The Line Control Register is used to specify the asynchronous data communication format. The number of the word length, stop bits, and parity can be selected by writing appropriate bits in this register.

LCR BIT1-0:
These two bits specify the word length to be transmitted or received.
00=5 bits word length
01=6 bits word length
10=7 bits word length
11=8 bits word length

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LCR BIT-2:
The number of stop bits can be specified by this bit.
0=1 stop bit , when word length=5, 6, 7, 8 bits
1=1 and 1/2 stop bit , when word length=5 bits
1=2 stop bits, word length=6, 7, 8 bits

LCR BIT-3:
Parity or no parity can be selected via this bit.
0=no parity
1=a parity bit is generated during the transmission; receiver also checks for received parity

Priority level	Bit-2	Bit-1	Bit-0	Source of the interrupts
1	1	1	0	LSR A/B (Receiver Line Status Register)
2	1	0	0	RXRDY A/B (Received Data Ready)
3	0	1	0	TXRDY A/B (Transmitter holding register empty)
4	0	0	0	MSR A/B (Modem Status Register)
0	0	0	1	No interrupts

LCR BIT-4:
If the parity bit is enabled, LCR BIT-4 selects the even or odd parity format.
0=odd parity is generated by calculating odd number of 1's in the transmitted data; receiver also checks for same format.
1=an even parity bit is generated by calculating the number of even 1's in the transmitted or received data.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5=1 and LCR BIT-4=0 parity bit is forced to "1" in the transmitted and received data
LCR BIT-5=1 and LCR BIT-4=1 parity bit is forced to "0" in the transmitted and received data

LCR BIT-6:
Break control bit.
1=forces the transmitter output (TXA/B) to go low to alert the communication terminal
0=normal operating condition

LCR BIT-7:
The internal baud rate counter latch enable (DLAB).
0=normal operation
1=select divisor latch register

MODEM CONTROL REGISTER

This register controls the interface with the MODEM or a peripheral device (RS232).

MCR BIT-0:
0=force DTR~ output to high
1=force DTR~ output to low

MCR BIT-1:
0=force RTS~ output to high
1=force RTS~ output to low

MCR BIT-2:
Not used.

MCR BIT -3:
INTA/B output control.
0=INTA/B outputs disabled
1=INTA/B outputs enabled

MCR BIT -4:
0=normal operating mode
1=enable local loop-back mode (diagnostics). The transmitter output (TXA/B) is set high (Mark condition), the Receiver inputs (RXA/B , CTSA/B~, DSRA/B~, CDA/B~, and RIA/B~) are disabled. Internally, the transmitter output is connected to the receiver input and DTRA/B~, RTSA/B~ are connected to modem control inputs. In this mode , the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupt sources are now the lower four bits of the Modem Control Register instead of the four Modem Control Inputs. The interrupts are still controlled by the IERA/B.

MCR BIT 5-7:
Not used. Are set to zero permanently.

LINE STATUS REGISTER

This register provides the status of data transfer to CPU.

LSR BIT-0:
0=no data in receive holding register
1=a data has been received and saved in the receive holding register

LSR BIT-1:
0=no overrun error (normal)
1=overrun error, next character arrived before receive holding register was empty

LSR BIT-2:
0=no parity error (normal)
1=parity error, received data does not have correct parity information

LSR BIT-3:
0=no framing error (normal)
1=framing error received, received data did not have a valid stop bit

LSR BIT-4:
0=no break condition (normal)
1=receiver received a break signal (RX was low for one character time frame)

LSR BIT-5:
0=transmit holding register is full. XR-16C452 will not accept any data for transmission.
1=transmit holding register is empty. CPU can load the next character.

LSR BIT-6:
0=transmitter holding and shift registers are full
1=transmitter holding and shift registers are empty

LSR BIT-7:
Not used. Set to zero permanently.

MODEM STATUS REGISTER

This register provides the current state of the control lines from the modem or peripheral to the CPU. Four bits of this register are used to indicate the changed information. These bits are set to "1" whenever a control input from the MODEM changes state. They are set to "0" whenever the CPU reads this register.

MSR BIT-0:
Indicates that the CTS~ input to the XR-16C452 has changed state since the last time it was read.

MSR BIT-1:
Indicates that the DSR~ input to the XR-16C452 has changed state since the last time it was read.

MSR BIT-2:
Indicates that the RI~ input to the XR-16C452 has changed from a low to a high state.

MSR BIT-3:
Indicates that the CD~ input to the XR-16C452 has changed state since the last time it was read.

MSR BIT-4:
This bit is the compliment of the CTS~ input. It is equivalent to RTS in the MCR during loop-back mode.

MSR BIT-5:
This bit is the compliment of the DSR~ input. It is equivalent to DTR in the MCR during loop-back mode.

MSR BIT-6:
This bit is the compliment of the RI~ input.

MSR BIT-7:
This bit is the compliment to the CD~ input.

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SCRATCHPAD REGISTER

XR-16C452 provides a temporary data register to store 8 bits of information for variable use.

BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

BAUD RATE	16 x CLOCK DIVISOR	% ERROR
50	2304	
75	1536	
110	1047	0.026
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.69
2400	48	
3600	36	
4800	24	
7200	16	
9600	12	
19.2K	6	
38.4K	3	
56K	2	2.86
112K	1	

The XR-16C452 contains a programmable Baud Rate Generator that is capable of taking any clock input from DC to 16 MHz and dividing it by any divisor from 2 to 2^{16}-1. Customized Baud Rates can be achieved by selecting proper divisor values for MSB and LSB of the Baud Rate Generator.

$$\text{divisor value (decimal)} = \frac{\text{input frequency}}{\text{baud rate X 16}}$$

$$\text{EXAMPLE: } \frac{1.8432 \times 10^6}{1200 \text{ (baud)}} = 96 \text{ (decimal)}$$

96 decimal = 0060 HEX
Divisor MSB = 00
Divisor LSR = 60

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XR-16C452 ACCESSIBLE REGISTERS

A2	A1	A0	Register	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
0	0	0	RHR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	THR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	IER	0	0	0	0	modem status interrupt	receive line status	transmit holding register	receive holding register
0	1	0	ISR	0	0	0	0	0	int priority bit-1	int priority bit-0	int status
0	1	1	LCR	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1	0	0	MCR	0	0	0	loop back	OP2~	OP1~	RTS~	DTR~
1	0	1	LSR	0	trans. empty	trans. holding empty	break interrupt	framing error	parity error	overrun error	receive data ready
1	1	0	MSR	CD	RI	DSR	CTS	delta CD~	delta RI~	delta DSR~	delta CTS~
1	1	1	SPR	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	0	DLL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0	0	1	DLM	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

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PRINTER PORT PROGRAMMING TABLE:

A1	A0	IOW~	IOR~
0	0	PORT REGISTER	PORT REGISTER
0	1	(PS/2 only) I/O SELECT REGISTER*	STATUS REGISTER *
1	0	CONTROL REGISTER	COMMAND REGISTER

** Reading the status register will reset the INTP output.*

PARALLEL PORT DIRECTION SELECT REGISTER (WRITE ONLY)

CONTROL REGISTER (D5)	BIDEN	I/O SELECT REGISTER (D7-D0)	PORT MODE
X	0	xxxxxxxx exp. AA Hex	OUTPUT
X	0	10101010	INPUT
0	1	xxxxxxxx	OUTPUT
1	1	xxxxxxxx	INPUT

PORT REGISTER

Bidirectional printer port.
Writing to this register during output mode will transfer the contents of the data bus to the PD7-PD0 ports . Reading this register during input mode will transfer the states of the PD7-PD0 to the data bus. This register will be set to the output mode after reset.

PR BIT 7-0:
PD7-PD0 bidirectional I/O ports.

STATUS REGISTER

This register provides the state of the printer outputs and the interrupt condition.

SR BIT 1-0:
Not used. Are set to "1" permanently.

SR BIT-2:
Interrupt condition.
0= an interrupt is pending
This bit will be set to "0" at the falling edge of the ACK~ input.
1= no interrupt is pending
Reading the STATUS REGISTER will set this bit to "1".

SR BIT-3:
ERROR~ input state.
0= ERROR~ input is in low state
1= ERROR~ input is in high state

SR BIT-4:
SLCT input state.
0= SLCT input is in low state
1= SLCT input is in high state

SR BIT-5:
PE input state.
0= PE input is in low state
1= PE input is in high state

SR BIT-6:
ACK~ input state.
0= ACK~ input is in low state
1= ACK~ input is in high state

SR BIT-7:
BUSY input state.
0= BUSY input is in high state
1= BUSY input is in low state

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COMMAND REGISTER

The state of the STROBE~, AUTOFDXT~, INIT, SLCTIN~ pins, and interrupt enable bit can be read by this register regardless of the I/O direction.

COM BIT-0:
STROBE~ input pin.
0= STROBE~ pin is in high state
1= STROBE~ pin is in low state

COM BIT-1:
AUTOFDXT~ input pin.
0= AUTOFDXT~ pin is in high state
1= AUTOFDXT~ pin is in low state

COM BIT-2:
INIT input pin.
0= INIT pin is in low state
1= INIT pin is in high state

COM BIT-3:
SLCTIN~ input pin.
0= SLCTIN~ pin is in high state
1= SLCTIN~ pin is in low state

COM BIT-4:
Interrupt mask.
0= Interrupt (INTP output) is disabled
1= Interrupt (INTP output) is enabled

COM BIT 7-5:
Not used. Are set to "1" permanently.

CONTROL REGISTER.

Writing to this register will set the state of the STROBE~, AUTOFDXT~, INIT, SLCTIN pins, and interrupt mask register.

CON BIT-0:
STROBE~ output control bit.
0= STROBE~ output is set to high state
1= STROBE~ output is set to low state

CON BIT-1:
AUTOFDXT~ output control bit.
0= AUTOFDXT~ output is set to high state
1= AUTOFDXT~ output is set to low state

CON BIT-2:
INIT output control bit.
0= INIT output is set to low state
1= INIT output is set to high state

CON BIT-3:
SLCTIN~ output control bit.
0= SLCTIN~ output is set to high state
1= SLCTIN~ output is set to low state

CON BIT-4:
Interrupt output control bit.
0= INTP output is disabled
1= INTP output is enabled

CON BIT-5 (PS/2 only):
I/O select. Direction of the PD7-PD0 can be selected by setting or clearing this bit.
0= PD7-PD0 are set for output mode
1= PD7-PD0 are set for input mode

CON BIT 7-6:
Not used.

I/O SELECT REGISTER (PS/2 only)

Software controlled I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in high state and setting CON BIT-5 to "zero or one"

Hardware/software I/O select.
Bidirectional mode can be selected by keeping the BIDEN input in low state and setting I/O SELECT register to "AA" Hex for input or any other value for output.

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XR-16C452 EXTERNAL RESET CONDITION TABLE:

REGISTERS	RESET STATE
IERA/B IERA/B	BITS 0-7=0
ISRA/B ISRA/B	BIT 0=1, ISRA/B BITS 1-7=0
LCRA/B	LCRA/B BITS 0-7=0
MCRA/B	MCRA/B BITS 0-7=0
LSRA/B	LSRA/B BITS 0-4=0, LSRA/B BITS 5-6=1, LSRA/B BIT 7=0
MSRA/B	MSRA/B BITS 0-3=0, MSRA/B BITS 4-7=input signals
CR	CR BIT 4=0

SIGNALS	RESET STATE
TXA/B	High
RTSA/B~	High
DTRA/B~	High
INTA/B	Three state
INTP	Three state
PD7-PD0	Output mode, PD7-PD0=0
STROBE~	Output mode, high
AUTOFDXT~	Output mode, high
INIT	Output mode, low
SLCTIN~	Output mode, high

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XR-16C452 PRINTER PORT REGISTER CONFIGURATIONS

PORT REGISTER (READ/WRITE)

D7	D6	D5	D4	D3	D2	D1	D0
PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

STATUS REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
BUSY~	ACK	PE	SLCT	ERROR STATE	IRQ	1	1
					1= No interrupt AT = only 0= Interrupt (PS/2 only)		

COMMAND REGISTER (READ ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	IRQ ENABLE	SLCTIN~	INIT FDXT~	AUTO-	STROBE~
			0= IRQ disabled 1= IRQ enabled				

CONTROL REGISTER (WRITE ONLY)

D7	D6	D5	D4	D3	D2	D1	D0
—	—	I/O SELECT	IRQ MASK	SLCTIN~	INIT	AUTO-FDXT~	STROBE~
		0=Output (PS/2 only) 1=Input X=AT only	0=INTP output disabled 1=INTP output enabled				

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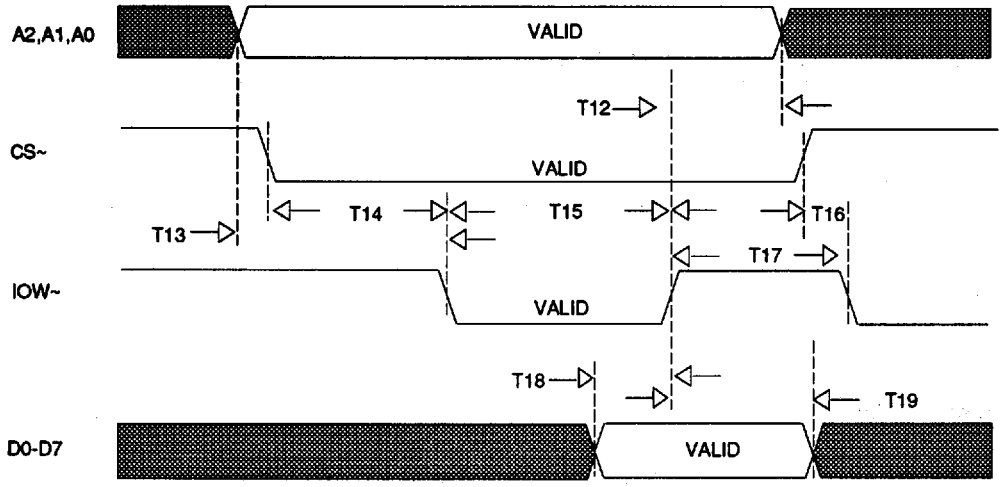
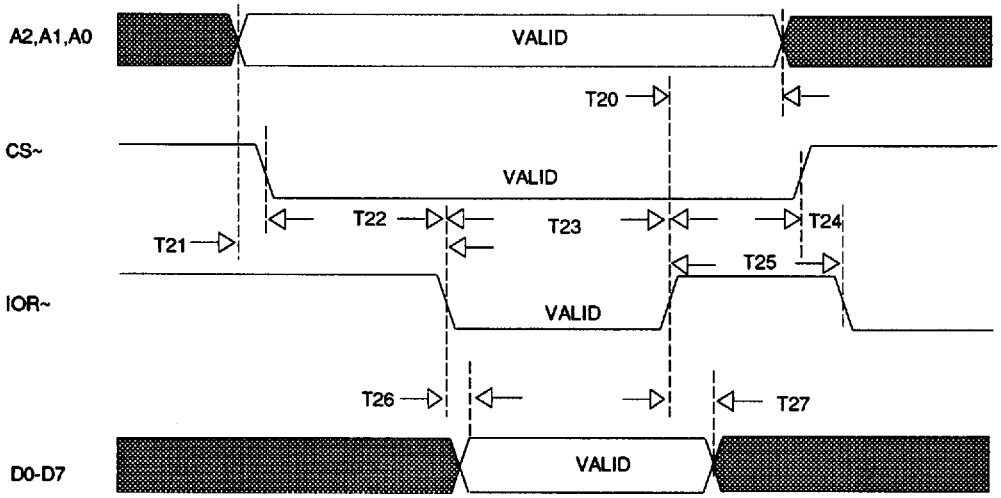
TIMING DIAGRAM

WRITE CYCLE TIMING



READ CYCLE TIMING



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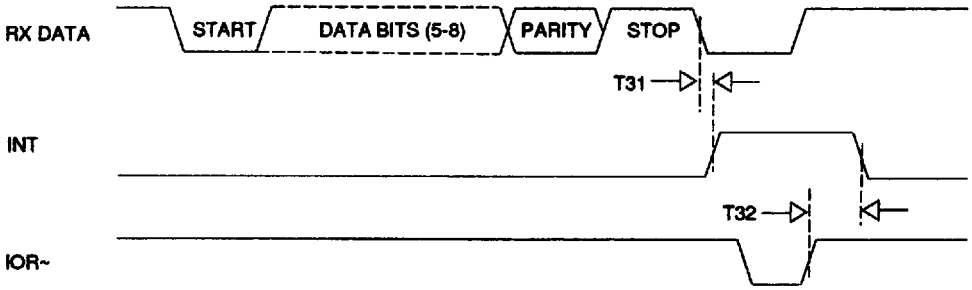
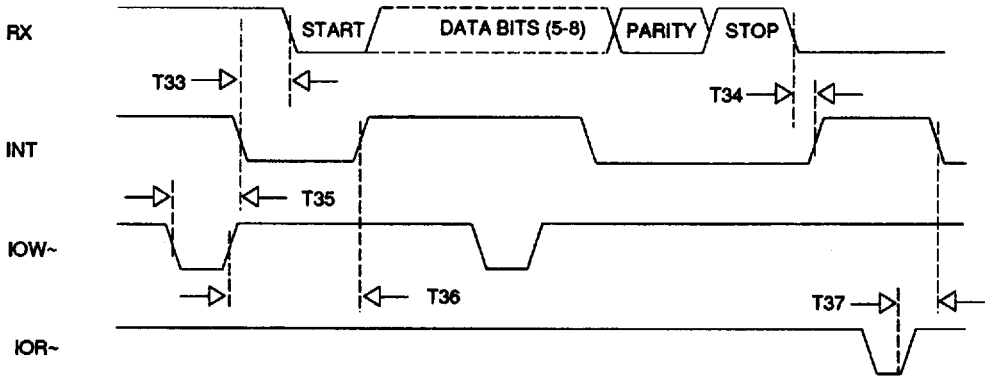
TIMING DIAGRAM

RECEIVER TIMING



TRANSMITTER TIMING



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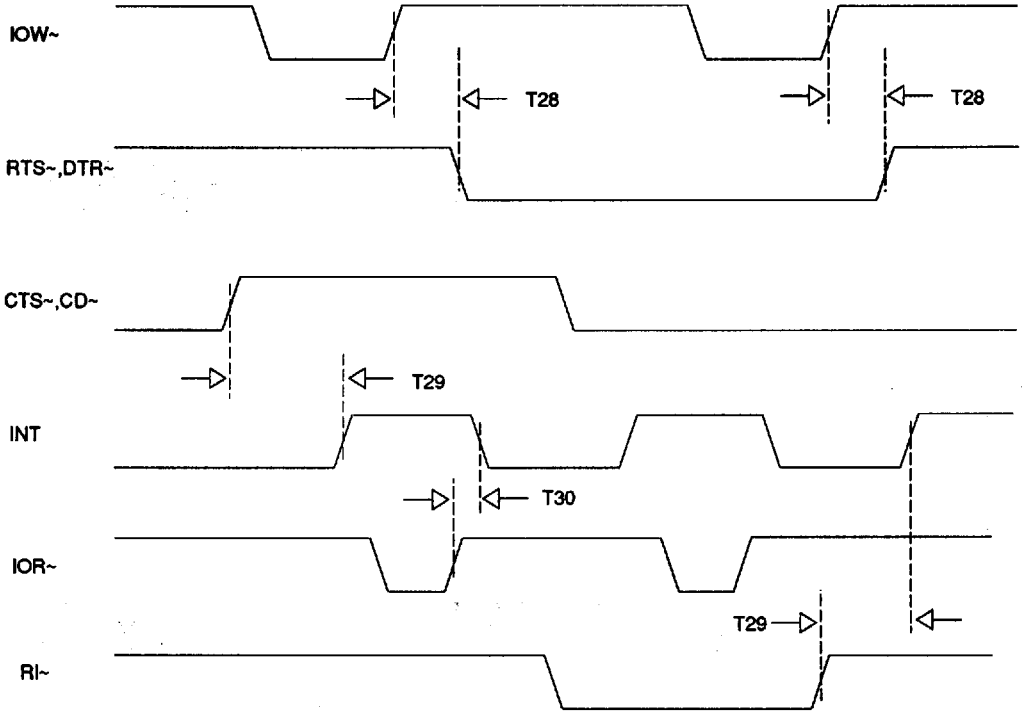
TIMING DIAGRAM

MODEM TIMING



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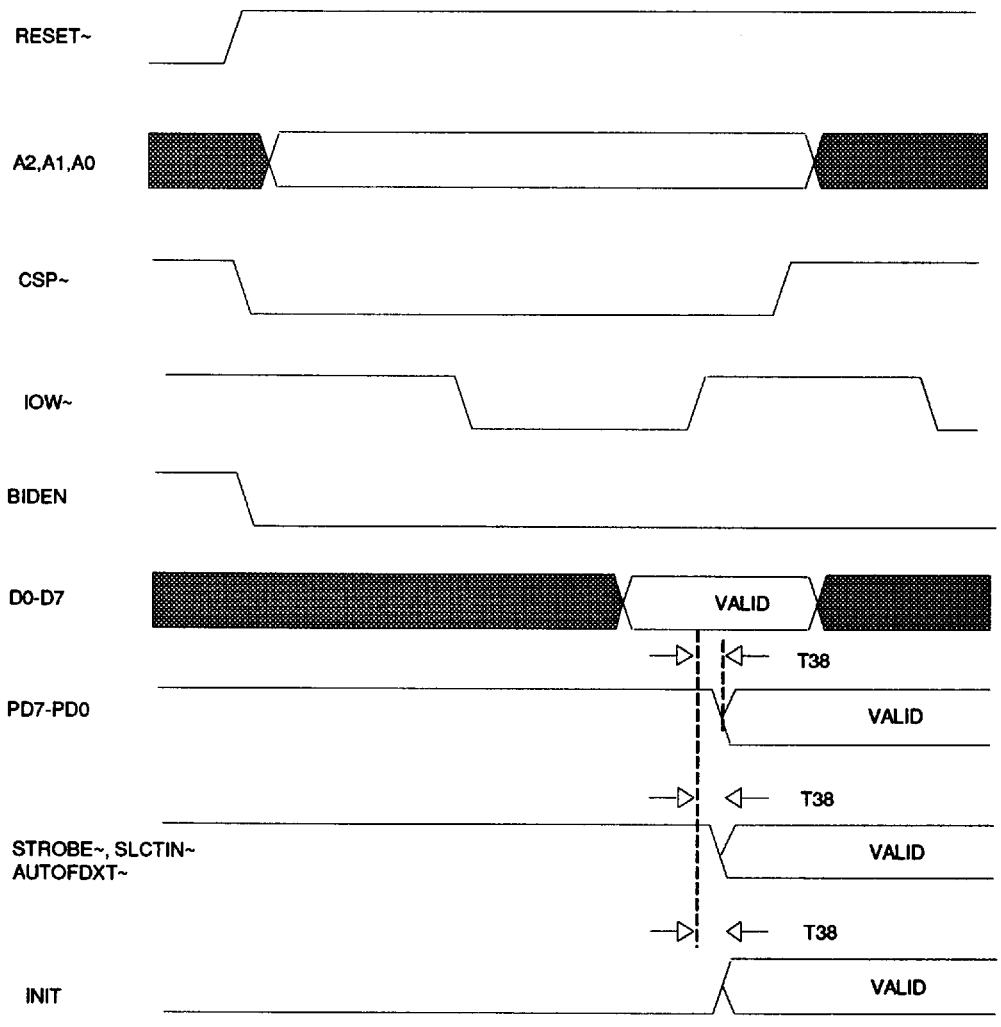
TIMING DIAGRAM

PRINTER WRITE OPERATION



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TIMING DIAGRAM

PRINTER READ OPERATION