NEC

MOS INTEGRATED CIRCUIT

μPD75512(A)

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75512(A) is a 4-bit single-chip microcomputer which employs 75X series architecture, and its performance is comparable to that of an 8-bit microcomputer.

In addition to its high-speed processing capabilities, the μPD75512(A) is also capable of processing data in units of 1, 4, or in 8-bits. With its internally provided A/D converter and serial interface, the μPD75512(A) provides the highest performance in its class.

Detailed functions are described in the following user's manual. Be sure to read it for designing.

μPD75516 User's Maual: IEM-5049

FEATURES

- Higher reliability than μPD75512
- Adequate I/O lines: 64
  (can be provided with pull-up/pull-down resistors: 47)
- Built-in 8-bit serial interface: 2-ch
  NEC standard serial bus interface (SBI) internally provided
- Built-in 8-bit A/D converter: 8-ch
- Variable instruction execution time function which is convenient for high-speed operation and power saving
  - 0.95 μs/1.95 μs/15.3 μs (at 4.19 MHz operation),
  - 122 μs (at 32.768 kHz operation)
- Program memory (ROM) size: 12,160 × 8 bits
- Data memory (RAM) size: 512 × 4 bits
- High-performance timer function: 4-ch
  - 8-bit timer/event counter
  - Watch timer
  - 8-bit basic interval timer
  - Timer/pulse generator: Capable of outputting 14-bit PWM
- Clock operation for reduced power consumption possible
  (5 μA TYP. at 3 V operation)
- PROM version (μPD75P516) available

APPLICATIONS

Switable for automotive and transportation equipments, etc.

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Date Published January 1994 P
Printed in Japan

The mark ★ shows major revised points.

ORDERING INFORMATION

Part Number	Package	Quality Grade
μPD75512GF(A)-xxx-3B9	80-pin plastic QFP (14 × 20mm)	Special

Remarks: xxx is ROM code number.

Please refer to "Quality Grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

Difference between μPD75512(A) and μPD75512

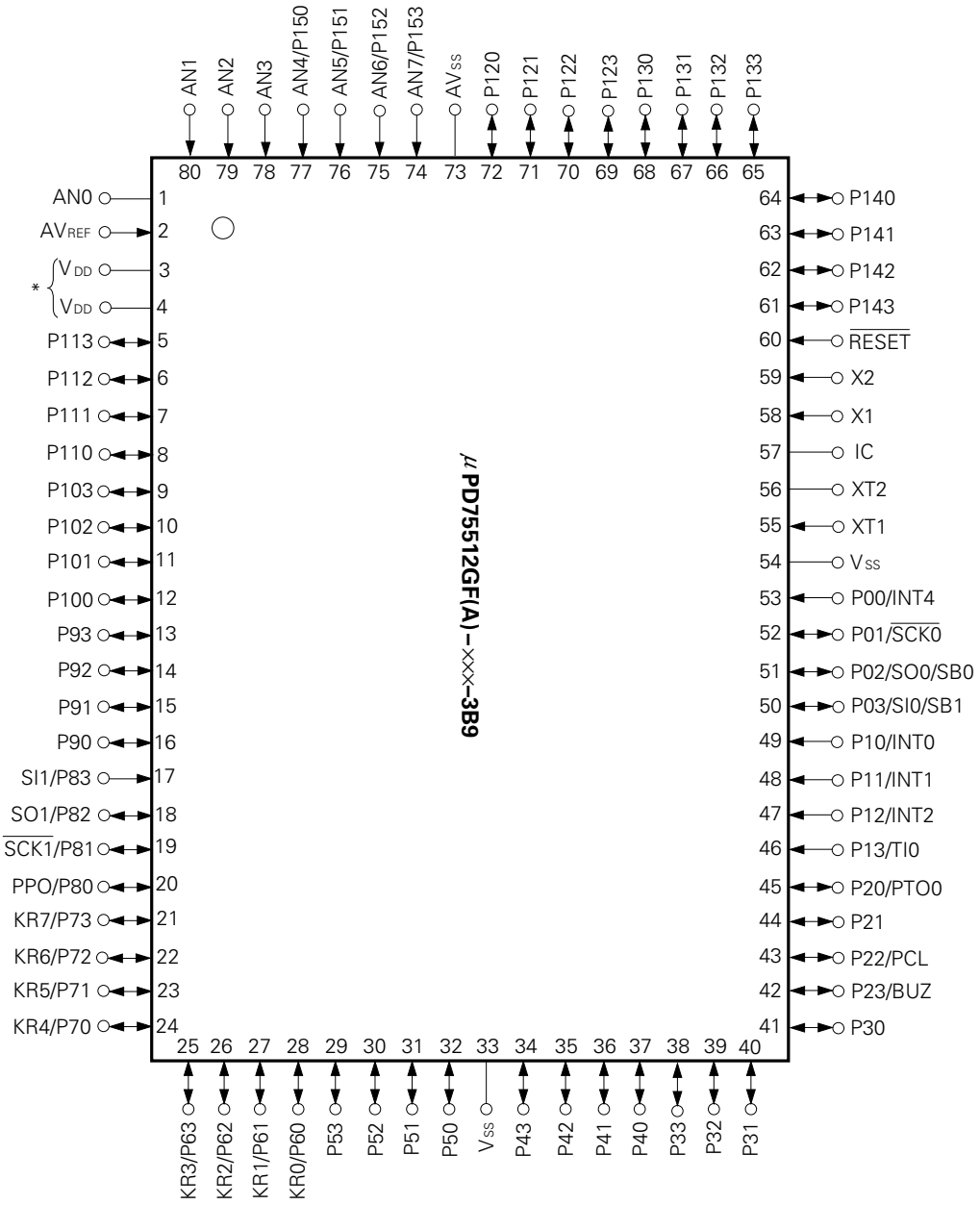
Item \ Product		μPD75512(A)	μPD75512
Quality Grade		Special	Standard
Electrical Specifications	Absolute Maximum Ratings	Differ in high-level and low-level output current	
	DC Characteristics	Differ in low-level output voltage	
	A/D Converter Characteristics	Differ in ambient temperature range and absolute accuracy	

μPD75512(A) FUNCTIONS ★

Item			Function
Internal Memory Size		ROM	12160 × 8 bits
		RAM	512 × 4 bits
Genearl-Purpose Register			(4 bits × 8 or 8 bits × 4) × 4 banks
Instruction Cycle			• 0.95 μs/1.91 μs/15.3 μs (Main system clock: at 4.19 MHz) • 122 μs (Subsystem clock: at 32.768 kHz)
Input/ Output Ports		Total	64 lines
		CMOS Inputs	16 lines (also serve as INT, SIO, PPO, analog input; can be pulled up by software: 7 lines)
		CMOS Input/Outputs	28 lines • Can be pulled up by software: 16 lines • Can be pulled down by mask option: 4 lines
		N-ch Open-Drain Input/Outputs	20 lines (10 V withstand voltage; pins that can be pulled up by mask option: 20)
A/D Converter			8-bit resolution × 8 channels (successive approxmation type) • Operation voltage: V_{DD} = 3.5 to 6.0 V
Timer/Counter			4 channels { • Timer/event counter • Basic interval timer • Timer/pulse generator (capable of outputting 14-bit PWM) • Watch timer
Serial Interface			2 channels { • NEC standard serial bus interface (SBI)/3-line SIO: 1 channel • Normal clock synchronized serial interface (3-line SIO): 1 channel
Vector Interrupt			External: 3, Internal: 4
Test Input			External: 1, Internal: 1
Instruction Set			• Bit data set/reset/test/boolean operation instruction • 4-bit data transfer/operation/increment/decrement /compare instructions • 8-bit data transfer/operation/increment/decrement /compare instructions
System Clock Generator			• Ceramic/crystal oscillator for main system clock: 4.19 MHz • Crystal oscillator for subsystem clock: 32.768 kHz
Operation Voltage			V_{DD} = 2.7 V to 6.0 V
Package			80-pin plastic QFP (14 × 20mm)

CONTENTS

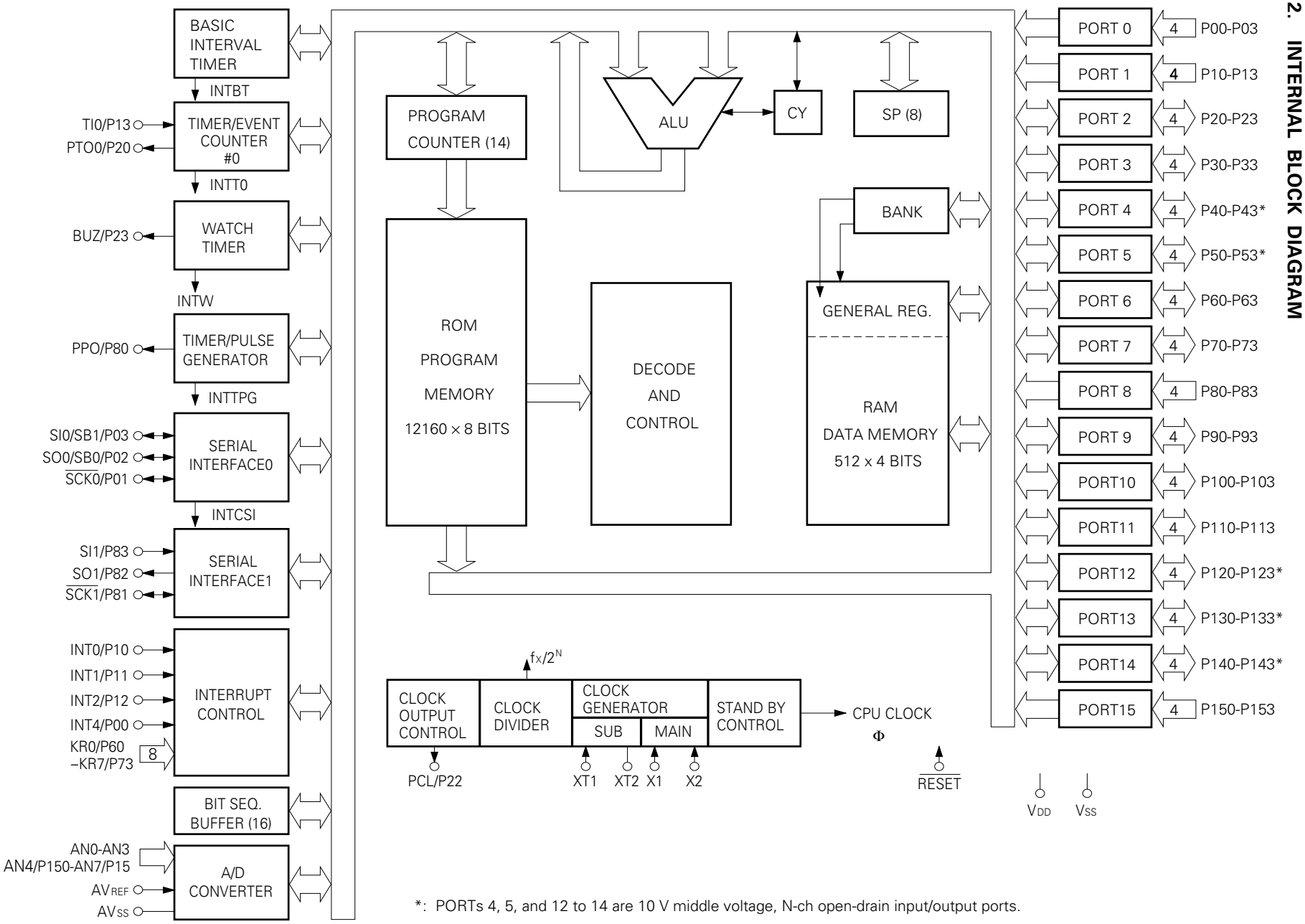
1. PIN CONFIGURATION



IC: Internally Connected (Connect directly to V_{SS})

*: Power must be supplied to both V_{DD} pins.

2. INTERNAL BLOCK DIAGRAM



*: PORTs 4, 5, and 12 to 14 are 10 V middle voltage, N-ch open-drain input/output ports.

3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin Name	Input/ Output	Shared Pin	Function	8-bit I/O	When Reset	Input/ Output Circuit Type*
P00	Input	INT4	4-bit input port (PORT0). For P01 to P03, built-in pull-up resistors can be specified in 3-bit units by software.	x	Input	Ⓑ
P01		$\overline{SCK0}$				Ⓕ-A
P02		SO0/SB0				Ⓕ-B
P03		SI0/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	x	Input	Ⓑ-C
P11		INT1				
P12		INT2	4-bit input port (PORT1). Built-in pull-up resistors can be specified by software in 4-bit units.			
P13		TI0				
P20	Input/ output	PTO0	4-bit input/output port (PORT2). Built-in pull-up resistors can be specified by software in 4-bit units.	x	Input	E-B
P21		—				
P22		PCL				
P23		BUZ				
P30	Input/ output	—	Programmable 4-bit input/output port (PORT3). Input/output can be specified in bit units. Built-in pull-up resistors can be specified by software in 4-bit unit.	x	Input	E-C
P31		—				
P32		—				
P33		—				
P40 to P43	Input/ output	—	N-ch open-drain 4-bit input/output port (PORT4). A pull-up resistor can be provided in bit units (mask option). 10V withstanding voltage in the open-drain mode.	O	High level (when pull-up resistor is provided) or high impedance	M
P50 to P53	Input/ output	—	N-ch open-drain 4-bit input/output port (PORT5). A pull-up resistor can be provided in bit units (mask option). 10V withstanding voltage in the open-drain mode.		High level (when pull-up resistor is provided) or high impedance	M
P60	Input/ output	KR0	Programmable 4-bit input/ output port (PORT6). Input/output can be specified in bit units. Built-in pull-up resistors can be specified by software in 4-bit units.	O	Input	Ⓕ-C
P61		KR1				
P62		KR2				
P63		KR3				

*: The number enclosed with a circle indicates Schmitt trigger input.

3.1 PORT PINS (2/2)

Pin Name	Input/ Output	Shared Pin	Function	8-bit I/O	When Reset	Input/ Output Circuit Type*
P70	Input/ output	KR4	4-bit input/output port (PORT7). Built-in pull-up resistor can be specified in 4-bit units by software.	O	Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80	Input	PPO	4-bit input port (PORT8).	x	Input	E
P81		$\overline{\text{SCK1}}$				Ⓕ
P82		SO1				E
P83		SI1				Ⓑ
P90 to P93	Input/ output	—	4-bit input/output port (PORT9). Built-in pull-up resistors can be specified in bit units by mask option.	x	Low level (when pull-down resistor is provided) or high impedance	V
P100 to P103	Input/ output	—	4-bit input/output port (PORT10).	x	Input	E
P110 to P113	Input/ output	—	4-bit input/output port (PORT11).		Input	E
P120 to P123	Input/ output	—	N-ch open-drain 4-bit input/output port (PORT12). A pull-up resistor can be provided in bit units (mask option). 10V withstanding voltage in the open-drain mode.	x	High level (when pull-up resistor is provided) or high impedance	M
P130 to P133	Input/ output	—	N-ch open-drain 4-bit input/output port (PORT13). A pull-up resistor can be provided in bit units (mask option). 10V withstanding voltage in the open-drain mode.	x	High level (when pull-up resistor is provided) or high impedance	M
P140 to P143	Input/ output	—	N-ch open-drain 4-bit input/output port (PORT14). A pull-up resistor can be provided in bit units (mask option). 10V withstanding voltage in the open-drain mode.	x	High level (when pull-up resistor is provided) or high impedance	M
P150 to P153	Input	AN4 to AN7	4-bit input port (PORT15).	x	Input	Y-A

*: The number enclosed with a circle indicates Schmitt trigger input.

3.2 NON-PORT PINS

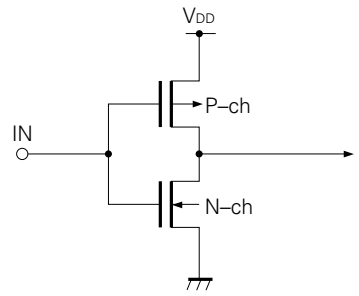
Pin Name	Input/ Output	Shared Pin	Function		When Reset	Input/ Output Circuit Type*
TI0	Input	P13	The external event pulse input for the timer/event counter.		—	Ⓑ-C
PTO0	Output	P20	Timer/event counter output		Input	E-B
PCL	Output	P22	Clock output		Input	E-B
BUZ	Output	P23	Fixed frequency output (for buzzer output or system clock trimming)		Input	E-B
$\overline{SCK0}$	Input/ output	P01	Serial clock input/output		Input	Ⓕ-A
SO0/SB0	Input/ output	P02	Serial data output Serial bus input/output		Input	Ⓕ-B
SI0/SB1	Input/ output	P03	Serial data input Serial bus input/output		Input	Ⓜ-C
INT4	Input	P00	Edge detection vector interrupt input (both rising edge and falling edge detection)		—	Ⓑ
INT0	Input	P10	Edge detection vector interrupt input (detection edge selectable)	Synchronized with clock	—	Ⓑ-C
INT1		P11		Asynchronous		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Asynchronous	—	Ⓑ-C
KR0-KR3	Input	P60-P63	Parallel falling edge detection testable input		Input	Ⓕ-C
KR4-KR7	Input	P70-P73	Parallel falling edge detection testable input		Input	Ⓕ-A
$\overline{SCK1}$	Input/ output	P81	Serial clock input/output		Input	Ⓕ
SO1	Output	P82	Serial data output		Input	E
SI1	Input	P83	Serial data input		Input	Ⓑ
AN0-AN3	Input	—	A/D converter analog input		—	Y
AN4-AN7		P150-P153				Y-A
AV_{REF}	Input	—	A/C converter reference voltage input		—	Z
AV_{SS}	—	—	A/D converter reference ground		—	—
X1, X2	Input	—	Pins for connecting the crystal ceramic oscillator to the main system clock generator. When inputting the external clock, input the external clock to pin X1, and the reverse phase of the external clock to pin X2.		—	—
XT1	Input	—	Pins for connecting the crystal oscillator to the subsystem clock generator. When the external clock is used, inputs the external clock to pin XT1. In this case, pin XT2 must be left open.		—	—
XT2	—					
$\overline{RESET}$	Input	—	System reset input		—	Ⓑ
PPO	Output	P80	Timer/pulse generator pulse output		Input	E
IC	—	—	Internally Connected. Connect directly to V_{SS}.		—	—
V_{DD}	—	—	Positive power supply		—	—
V_{SS}	—	—	GND		—	—

*: The number enclosed with a circle indicates Schmidt trigger input.

3.3 PIN INPUT/OUTPUT CIRCUITS

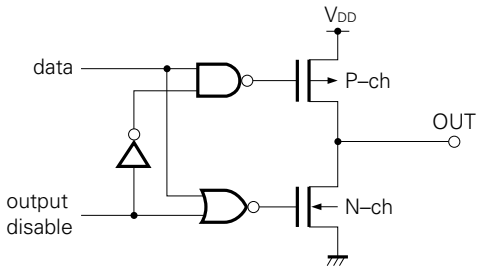
The following shows a simplified input/output circuit diagram for each pin of the μPD75512(A).

TYPE A



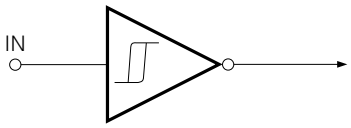
Input buffer of CMOS standard

TYPE D



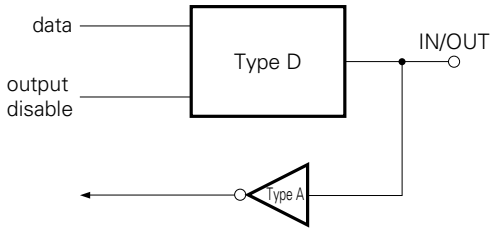
Push-pull output that can be set in a output high-impedance state (both P-ch and N-ch are off)

TYPE B



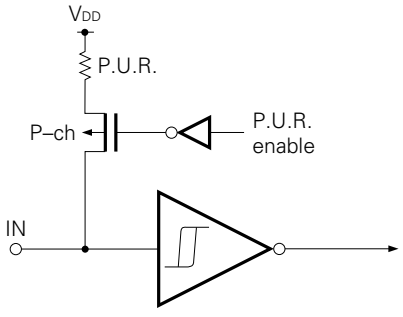
Schmitt trigger input with hysteresis characteristics

TYPE E



This input/output circuit consists of D-type push-pull outputs and Type A input buffers.

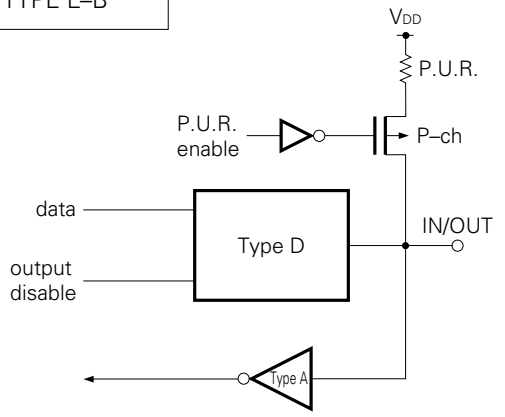
TYPE B–C



P.U.R. : Pull-Up Resistor

Schmitt trigger input with hysteresis characteristics

TYPE E–B



P.U.R. : Pull-Up Resistor

Fig. 3-1 Pin Input/Output Circuits (1/3)

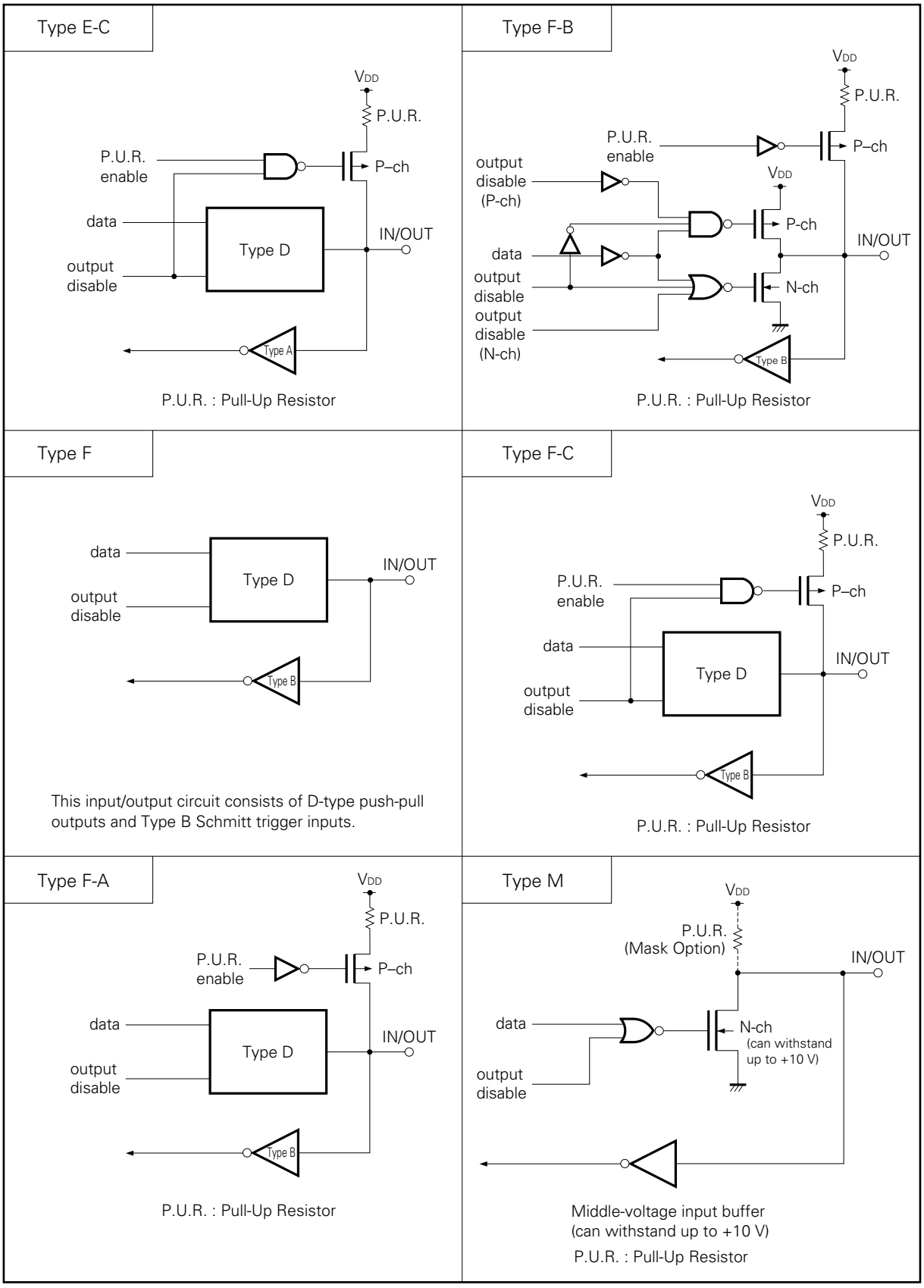


Fig. 3-1 Pin Input/Output Circuits (2/3)

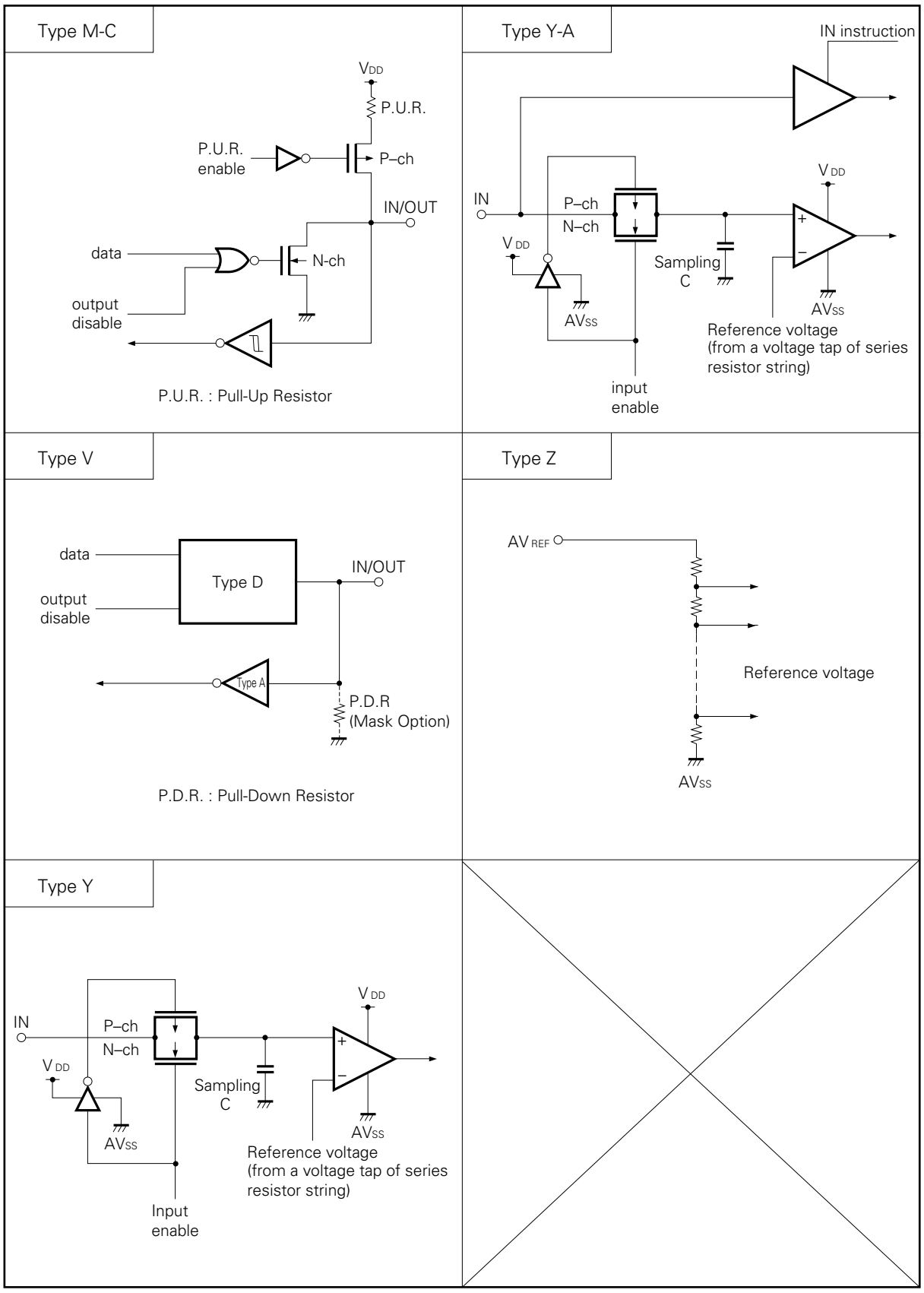


Fig. 3-1 Pin Input/Output Circuits (3/3)

★ 3.4 RECOMMENDED CONDITIONS FOR UNUSED PINS

Table 3-1 Recommended Conditions for Unused Pins

Pin	Recommended Conditions
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK0}$	Connect to V_{SS} or V_{DD}
P02/SO0/SB0	
P03/SI1/SB1	
P10/INT0-P12/INT2	Connect to V_{SS}
P13/TI0	
P20/PTO0	Input state: Connect to V_{SS} or V_{DD} Output state: Open
P21	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-P53	
P60/KR0-P63/KR3	
P70/KR4-P73/KR7	
P80/PPO	Connect to V_{SS} or V_{DD}
P81/$\overline{SCK1}$	
P82/SO1	
P83/SI1	
P90-P93	Input state: Connect to V_{SS} or V_{DD} Output state: Open
P100-P103	
P110-P113	
P120-P123	
P130-P133	
P140-P143	
P150/AN4-P153/AN7	Connect to V_{SS}
AN0-AN3	
XT1	Connect to V_{SS} or V_{DD}
XT2	Open
AV_{REF}	Connect to V_{SS}
AV_{SS}	
IC	Connect directly to V_{SS}

3.5 MASK OPTION SELECTION

The following mask options are provided with the pins.

(1) Pull-up/pull-down resistor selection

Table 3-2 Pull-up/Pull-down Resistor Selection

Pins	Mask Option	
P40-P43 P50-P53 P120-P123 P130-P133 P140-P143	(1) With pull-up resistor (Can be specified in bit units)	(2) Without pull-up resistor (Can be specified in bit units)
P90-P93	(1) With pull-down resistor (Can be specified in bit units)	(2) Without pull-down resistor (Can be specified in bit units)

(2) Feedback resistor selection for the subsystem clock oscillation ★

Table 3-3 Feedback Resistor Selection

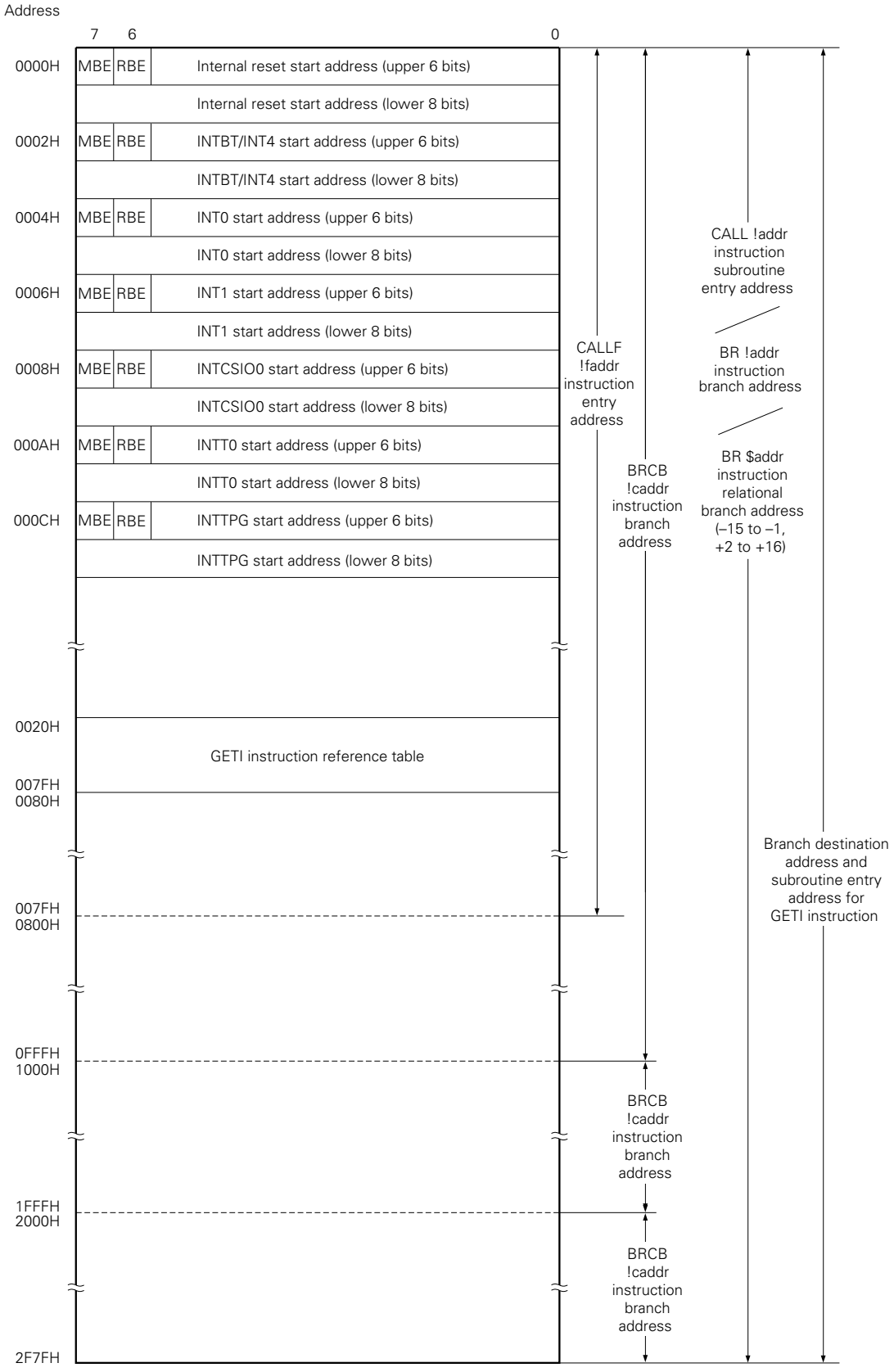
Pins	Mask Option	
XT1, XT2	(1) With feedback resistor (When the subsystem clock is used)	(2) Without feedback resistor (When the subsystem clock is not used)

Note: The operation is not affected if the feedback resistor is selected when the subsystem clock is not used. However, the supply current I_{DD} is increased.

★ 4. MEMORY CONFIGURATION

- Program memory (ROM) ... 12160 × 8 bits (0000H-2F7FH)
  - 0000H, 0001H : Vector table to which address from which program is started is written after reset
  - 0002H-000DH : Vector table to which address from which program is started is written after interrupt
  - 0020H-007FH: Table area referenced by GETI instruction

- Data memory
  - Data area .... 512 × 4 bits (000H–1FFH)
  - Peripheral hardware area .... 128 × 4 bits (F80H–FFFH)



Remarks: In addition to the above, branching to an address, for which only the lower 8 bits of the PC are modified, is possible by the BR PCDE and BR PCXA instructions.

Fig. 4-1 Program Memory Map

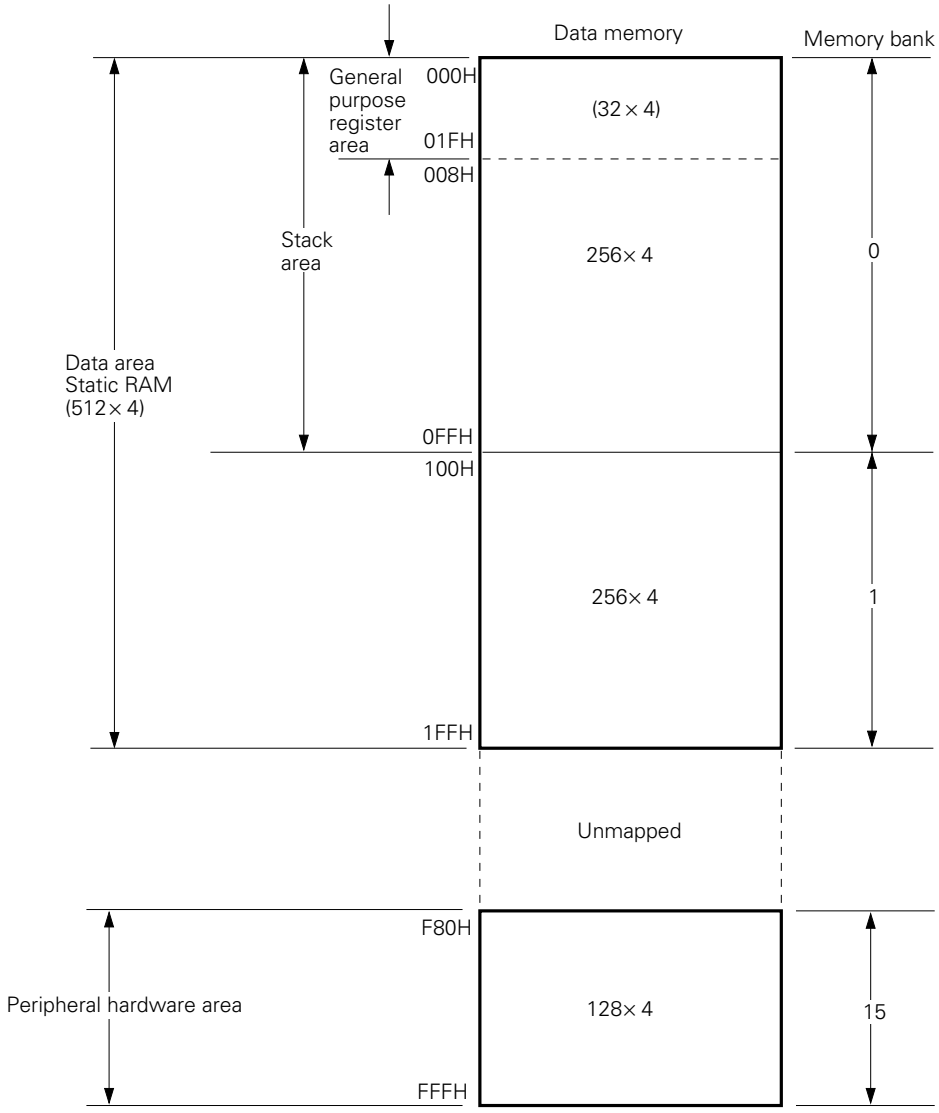


Fig. 4-2 Data Memory Map

5. PERIPHERAL HARDWARE FUNCTIONS ★

5.1 PORT

I/O ports are classified into following kinds:

- CMOS input (PORTS 0, 1, 8, 15) : 16
- CMOS input/output (PORTS 2, 3, 6, 7, 9, 10, 11) : 28
- N-ch open-drain input/output (PORTS 4, 5, 12, 13, 14) : 20

Total : 64

Table 5-1 Port Functions

Port (Pin Name)	Function	Operation/Feature		Remarks
PORT0	4-bit input	Can be read or tested regardless of the operation mode of the shared pin.		Also serves as the INT4, $\overline{SCK0}$, SO0/SB0, and SI0/SB1 pins
PORT1				Also serves as INT0 to 2, and TIO pins
PORT2	4-bit I/O	Can be specified for I/O in 4-bit units		Also serves as PTO0, PCL and BUZ pins.
PORT3		Can be specified for I/O in 1/4-bit units.		—
PORT4	4-bit I/O (N-ch open-drain, can sustain with 10V)	Can be specifiedfor I/O in 4-bit units	Ports 4 and 5 can be paired to I/O data in 8-bit units	Whether or not the internal pull-up resistor is provided can be specified for each bit by mask option
PORT5				
PORT6	4-bit I/O	Can be specified for I/O in 1/4-bit units	Ports 6 and 7 can be paired to I/O data in 8-bit units	Also serves as KR0-3.
PORT7		Can be specified I/O in 4-bit units		Also serves as KR4-7.
PORT8	4-bit input	Can be read or tested regardless of the operation mode of the shared pin.		Also serves as PPO, $\overline{SCK1}$, SO1, and SI1 pins.
PORT9	4-bit I/O	Can be specified for I/O in 4-bit units.		Whether or not the internal pull-up resistor is provided can be specified for each bit by mask option.
PORT10	4-bit I/O	Can be specified for I/O in 4-bit units.		—
PORT11				
PORT12	4-bit I/O (N-ch open-drain, can sustain with 10V)	Can be specified for I/O in 4-bit units.		Whether or not the internal pull-up resistor is provided can be specified for each bit by mask option.
PORT13				
PORT14				
PORT15	4-bit Input	Can be read or tested regardless of the operation mode of the shared pins		Also serves as AN4-7 pins.

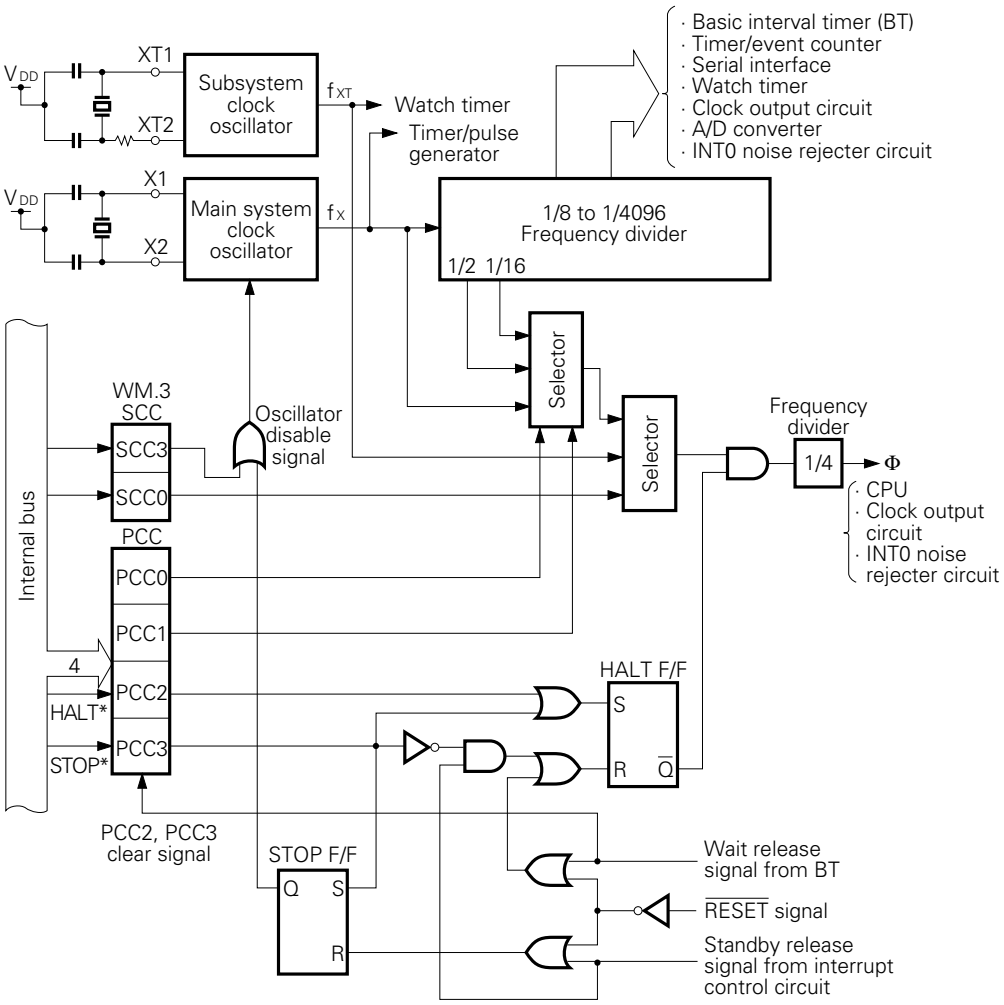
6.2 CLOCK GENERATOR CIRCUIT

The operation of the clock generator circuit is determined by the processor clock control regiser (PPC) and system clock control register (SCC).

This circuit can generate two types of clocks: main system clock and subsystem clock.

In addition, it can also change the instruction execution time.

- 0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)
- 122 μs (subsystem clock: 32.768 kHz)



*: instruction execution.

Remarks 1: f_X = Main system clock frequency

2: f_{XT} = Subsystem clock frequency

3: Φ = CPU clock

4: PCC: Processor clock control register

5: SCC: System clock control register

6: One clock cycle (t_{CY}) of Φ is one machine cycle of an instruction. For t_{CY}, refer to AC characteristics in 10. ELECTRICAL SPECIFICATIONS.

Fig. 5-1 Clock Generator Block Diagram

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs clock pulse from the P22/PCL pin. This clock pulse is used for the remote control output, peripheral LSIs, etc.

- Clock output (PCL): Φ, 524 kHz, 262 kHz, 65.5 kHz (operating at 4.19 MHz)

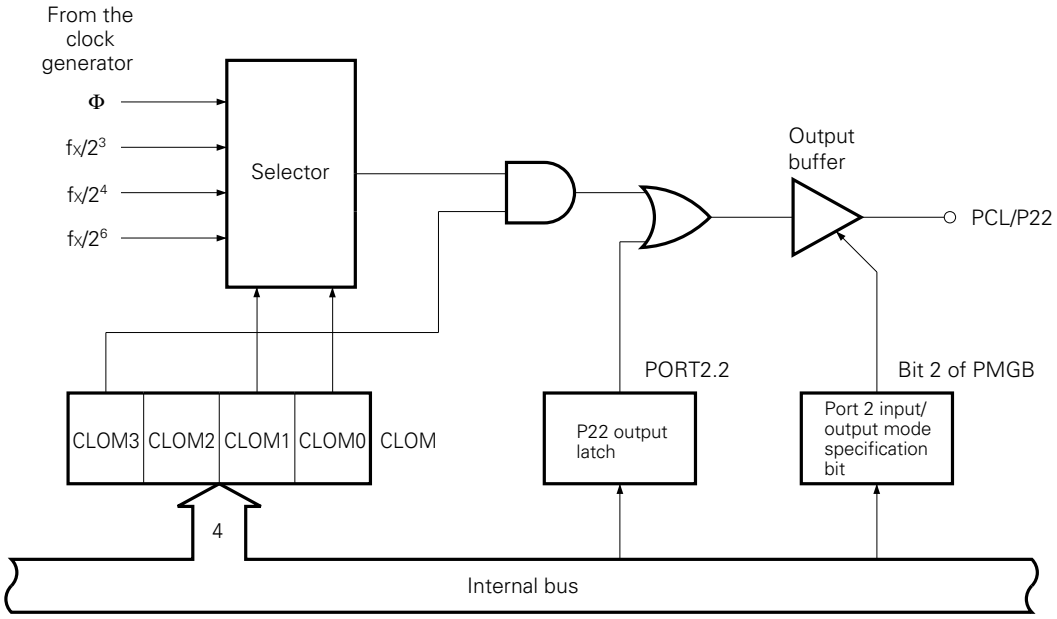


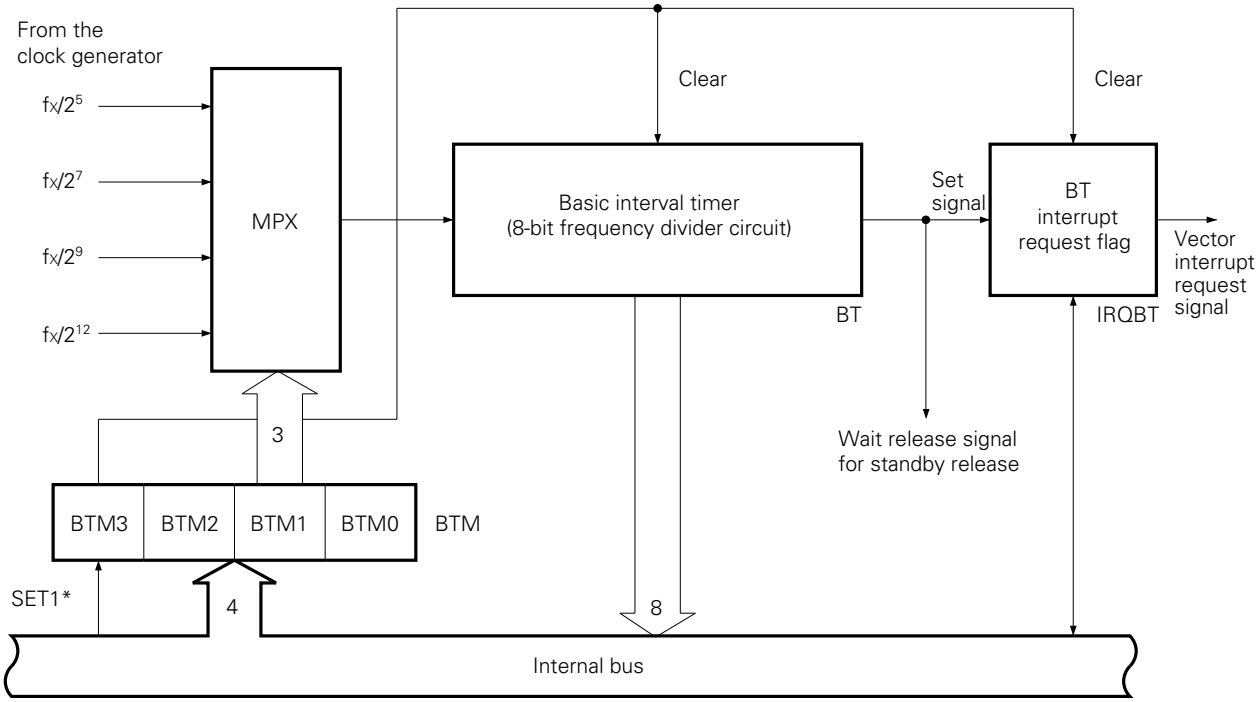
Fig. 5-2 Clock Output Circuit Configuration

Remarks: A measures to prevent outputting narrow width pulse when selecting clock output enable/ disable is taken.

5.4 BASIC INTERVAL TIMER

The basic interval timer has these functions:

- Interval timer operation which generates a reference time interrupt
- Watchdog timer application which detects a program runaway
- Selects the wait time for releasing the standby mode and counts the wait time
- Reads out the count value



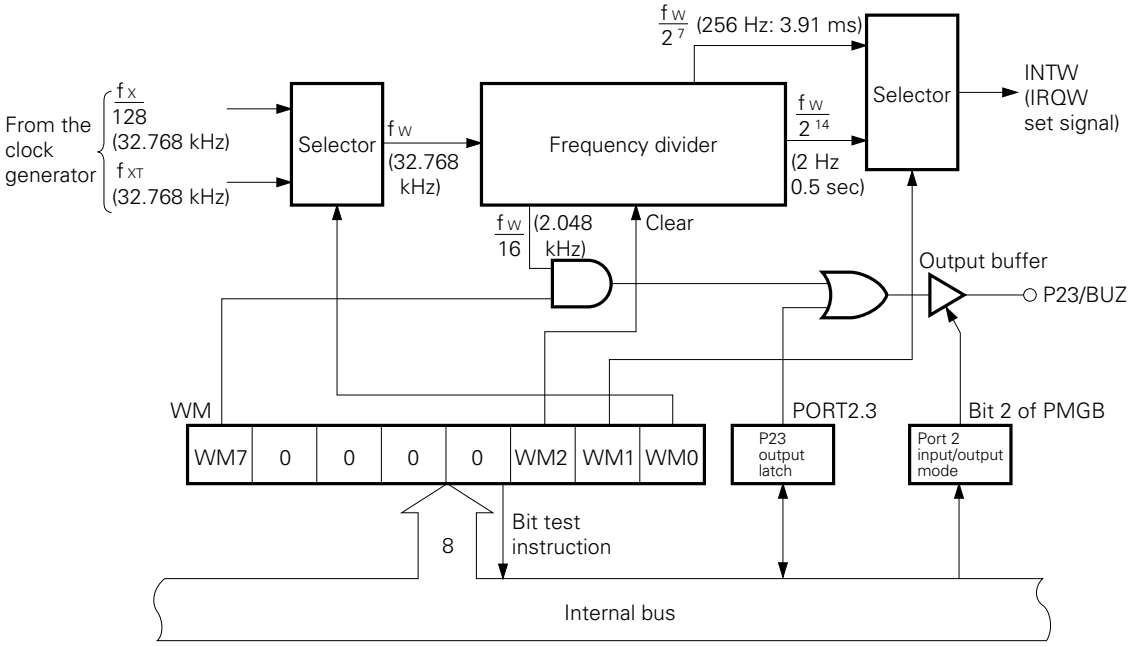
*: Instruction execution

Fig. 5-3 Basic Interval Timer Configuration

5.5 WATCH TIMER

The μPD75512(A) has a built-in 1-ch watch timer. The watch timer has these functions.

- Sets the test flag (IRQW) with 0.5 sec interval.
  The standby mode can be released by IRQW.
- 0.5 second interval can be generated either from the main system clock or subsystem clock.
- Time interval can be advanced to 128 times faster (3.91 ms) by setting the fast mode. This is convenient for program debugging, test, etc.
- Fixed frequency (2.048 kHz) can be output to the P23/BUZ pin. This can be used for beep and system clock frequency trimming.
- The frequency divider circuit can be cleared so that zero second watch start is possible.



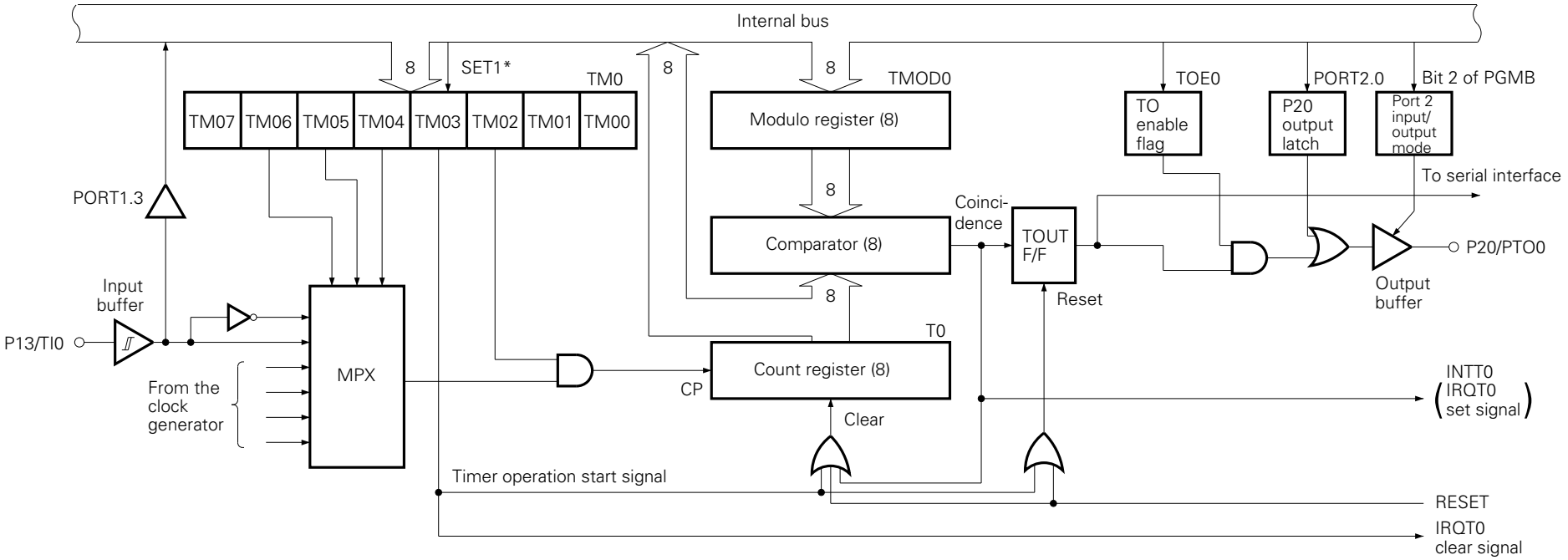
Remarks: ( ) is for fx = 4.194304 MHz, fxT = 32.768 kHz.

Fig. 5-4 Watch Timer Block Diagram

5.6 TIMER/EVENT COUNTER

The μPD75512(A) has a built-in 1-ch timer/event counter. The timer/event counter has these functions:

- Programmable interval timer operation
- Outputs square-wave signal of an arbitrary frequency to the PTO0 pin.
- Event counter operation
- Divides the TI0 pin input in N and outputs to the PTO0 pin (frequency divider operation).
- Supplies serial shift clock to the serial interface circuit.
- Count condition read out function



*:Instruction execution

Fig. 5-5 Timer/Event Counter Block Diagram

5.7 TIMER/PULSE GENERATOR

The μPD75512(A) contains a timer/pulse generator, that can be used as the timer or the pulse generator. Timer/pulse generator has the following functions.

(a) Function, when used in the timer mode
- 8-bit interval timer operation (IRQTPG generation), for which the clock source can be changed in 5 steps.
- Square waveform output to the PPO pin

(b) Function, when used in the PWM pulse generation mode
- 14-bit accuracy PWM pulse output to PPO pin (can be used as a D/A converter for electronics tuning).
- Fixed time interval interrupt generation (2^{15}/fx = 7.81ms: fx = 4.19 MHz)

When no pulse output is required, the PPO pin can be used as 1-bit output port.

Note: When setting the STOP mode, if the timer pulse generator is in operating mode, erroneous operation may occur. Therefore, the timer/pulse generator must be set in no-operation state by the mode register, before setting the STOP mode.

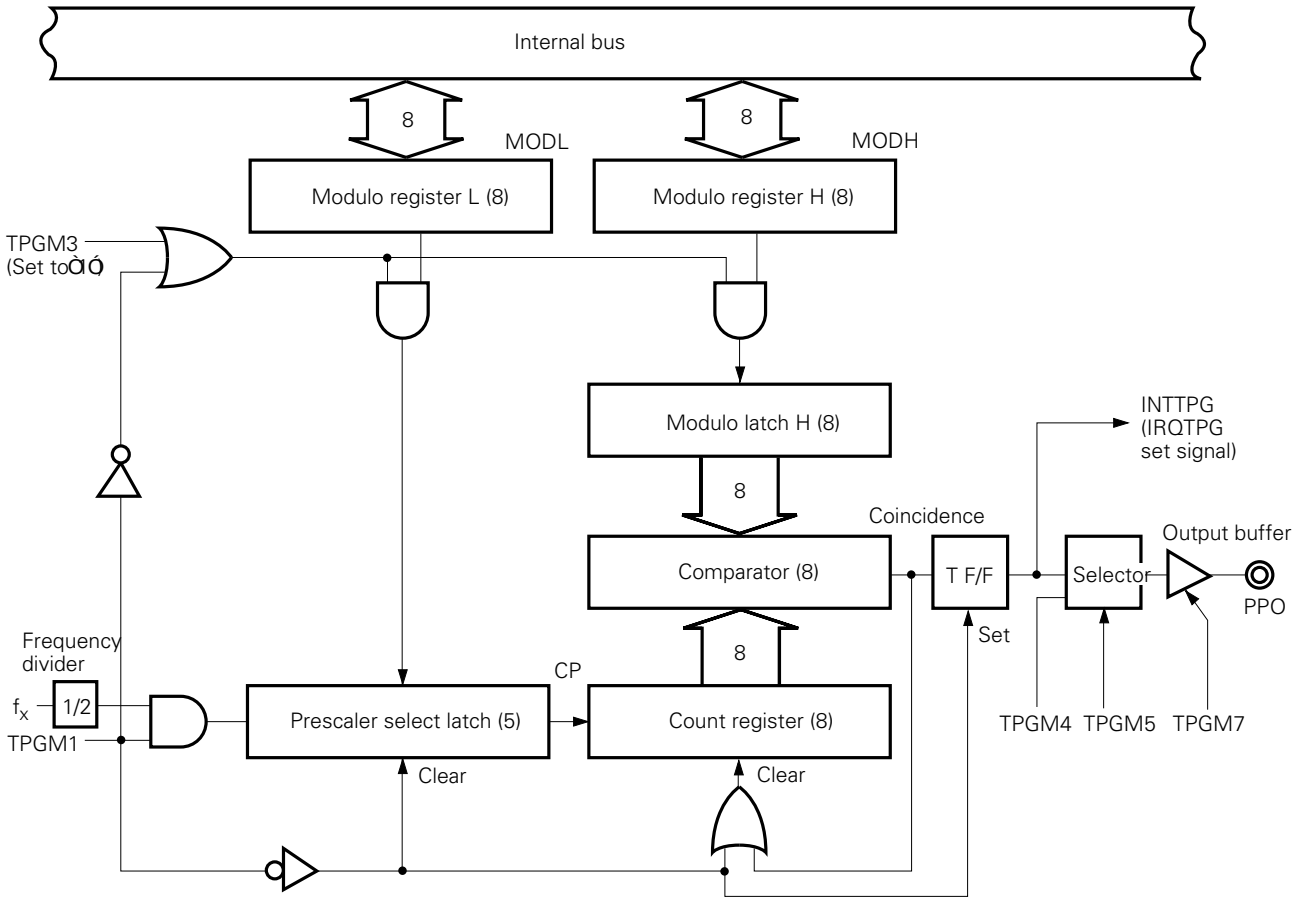


Fig. 5-6 Timer/Pulse Generator Block Diagram (Timer Mode)

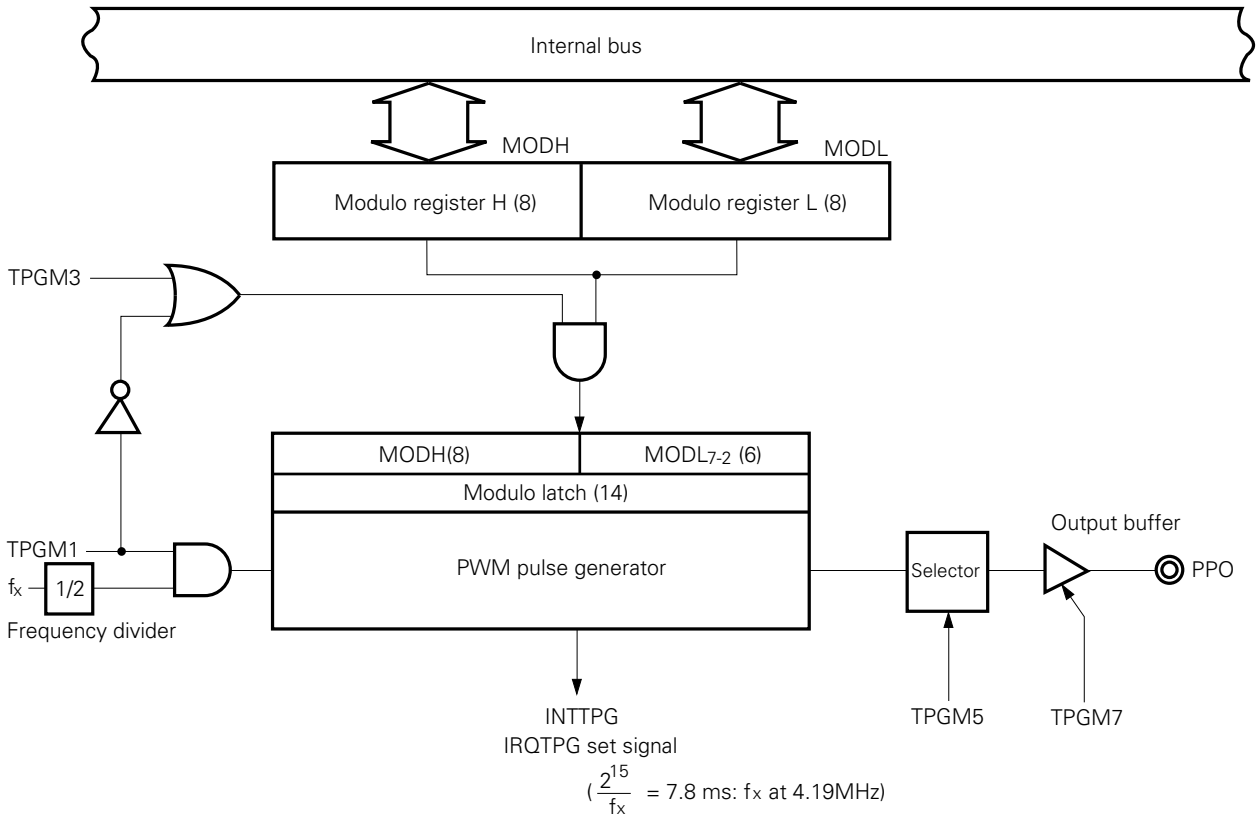


Fig. 5-7 Timer/Pulse Generator Block Diagram (PWM Pulse Generation Mode)

5.8 SERIAL INTERFACE

The μPD75512(A) is provided with two serial interface channels. Table 5-2 indicates differences between channel 0 and channel 1.

Table 5-2 Differences Between Channel 0 and Channel 1

Serial Transfer Mode, Funciton		Channel 0	Channel 1
3-Line Serial I/O	Clock Selection	$f_X/2^4$, $f_X/2^3$, TOUT F/F, external clock	$f_X/2^4$, $f_X/2^3$ external clock
	Transfer Method	MSB first/LSB first selectable	MSB first
	Transfer Completion Flag	Serial transfer completion interrupt request flag (IRQCSI0)	Serial transfer completion flag (EOT)
2-Line Serial I/O		Usable	Unprovided
Serial Bus Interface (SBI)			

(1) Serial interface function (Channel 0)

The μPD75512(A) is equipped with the following four modes:

- Operation stop mode
- Three-line serial I/O mode
- Two-line serial I/O mode
- SBI mode (serial bus interface mode)

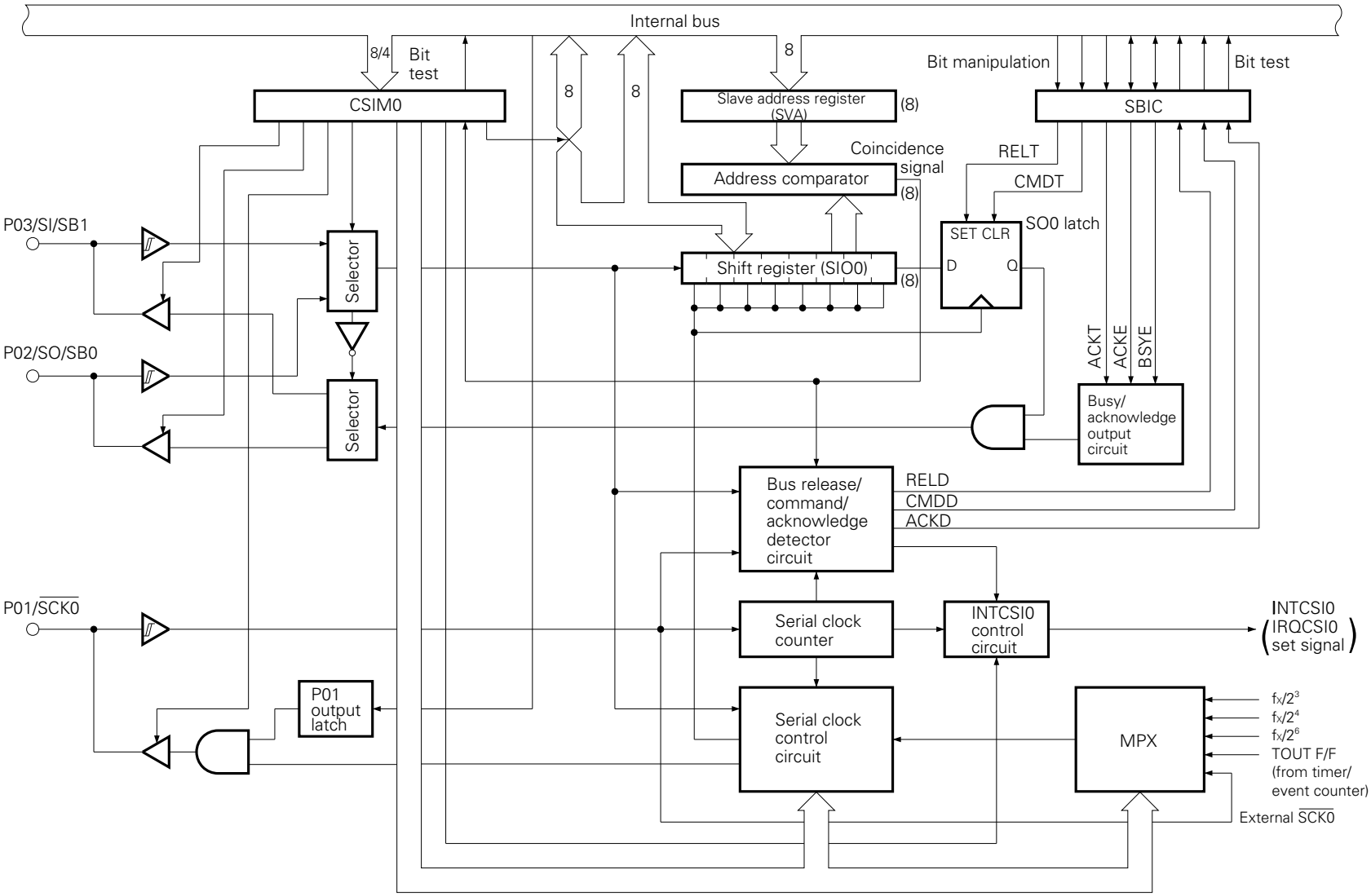


Fig. 5-8 Serial Interface (Channel 0) Block Diagram

(2) Serial interface (Channel 1) configuration

μPD75512(A) serial interface (channel 1) has following two modes.

- Operation stop mode
- 3-line serial I/O mode

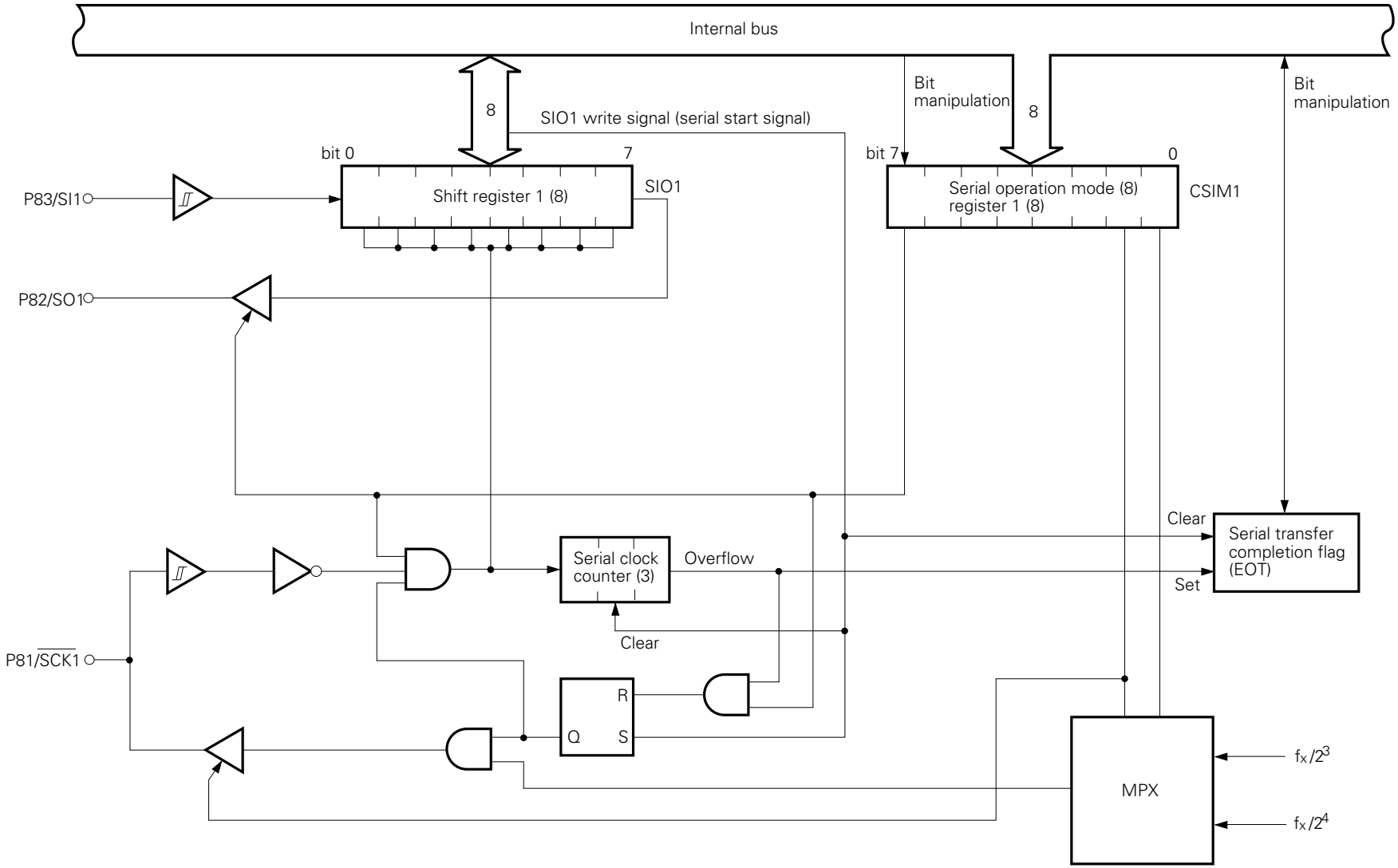


Fig. 5-9 Serial Interface (Channel 1) Block Diagram

5.9 A/D CONVERTER

The μPD75512(A) is provided with an 8-bit resolution analog-to-digital (A/D) converter with eight channels of analog inputs (AN0-AN7).

This A/D converter is of a successive approximation type.

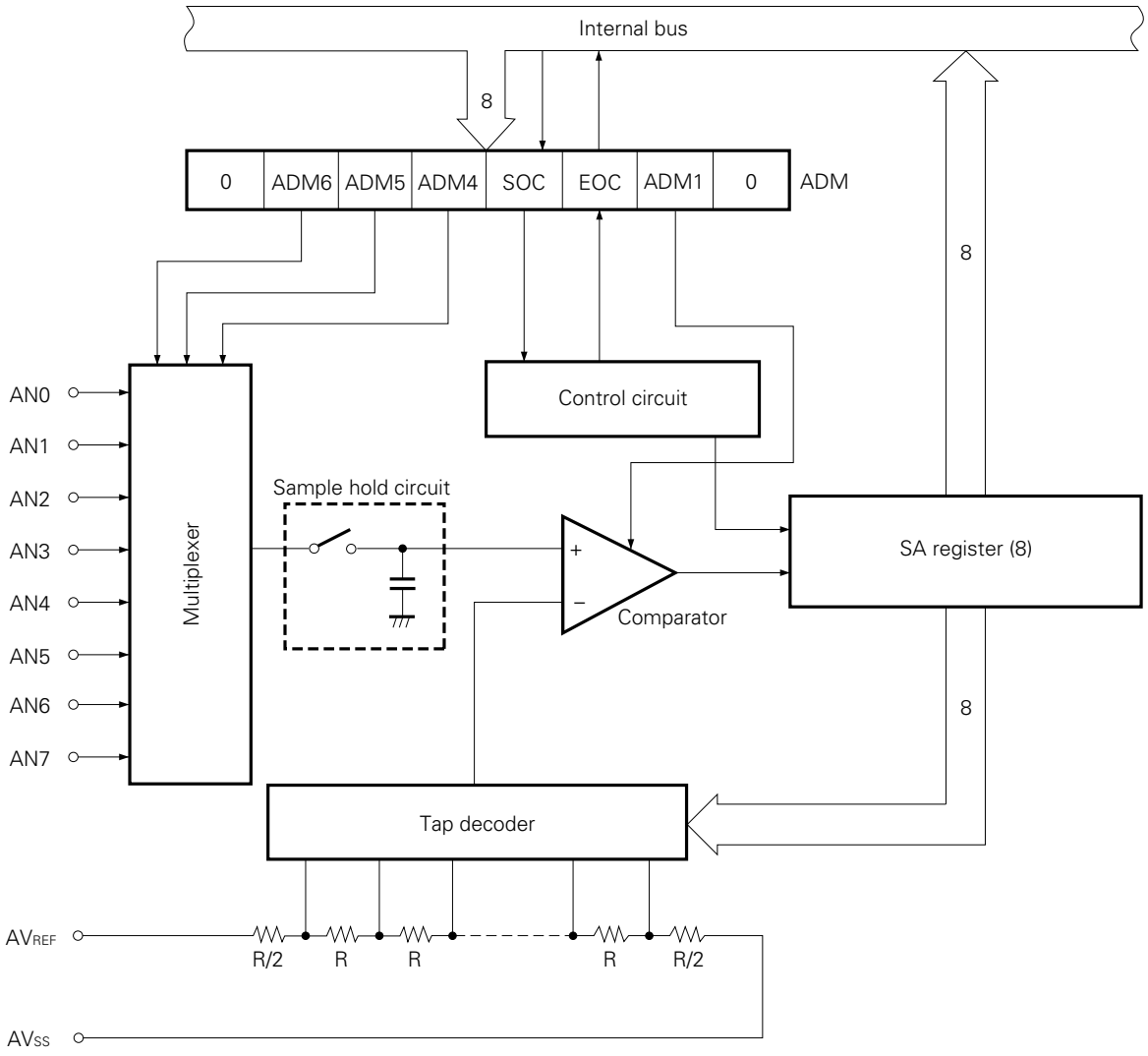
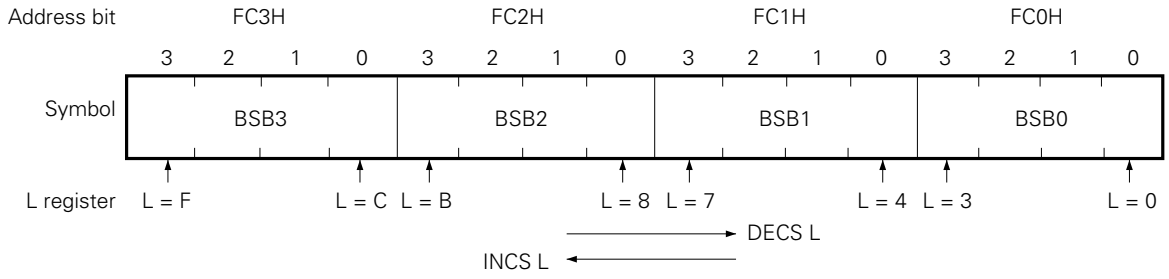


Fig. 5-10 Block Diagram of A/D Converter

5.10 BIT SEQUENTIAL BUFFER ..... 16 BITS

The bit sequential buffer is a data memory specifically provided for bit manipulation. With this buffer, addresses and bit specifications can be sequentially up-dated in bit manipulation operation. Therefore, this buffer is very useful for processing long data in bit units.



Remarks: For the pmem.@L addressing, the specification bit is shifted according to the L register.

Fig. 5-11 Bit Sequential Buffer Format

6. INTERRUPT FUNCTIONS

The μPD75512(A) has 7 different interrupt sources and multiplexed interrupt with priority order.

In addition to that, the μPD75512 is also provided with two types of test sources, of which INT2 has two types of edge detection testable inputs.

The interrupt control circuit of the μPD75512(A) has these functions:

- Hardware controlled vector interrupt function which can control whether or not to accept an interrupt by using the interrupt flag (IExxx) and interrupt master enable flag (IME).
- The interrupt start address can be arbitrarily set.
- Interrupt request flag (IRQxxx) test function (an interrupt generation can be confirmed by means of software).
- Standby mode release (Interrupts to be released can be selected by the interrupt enable flag).

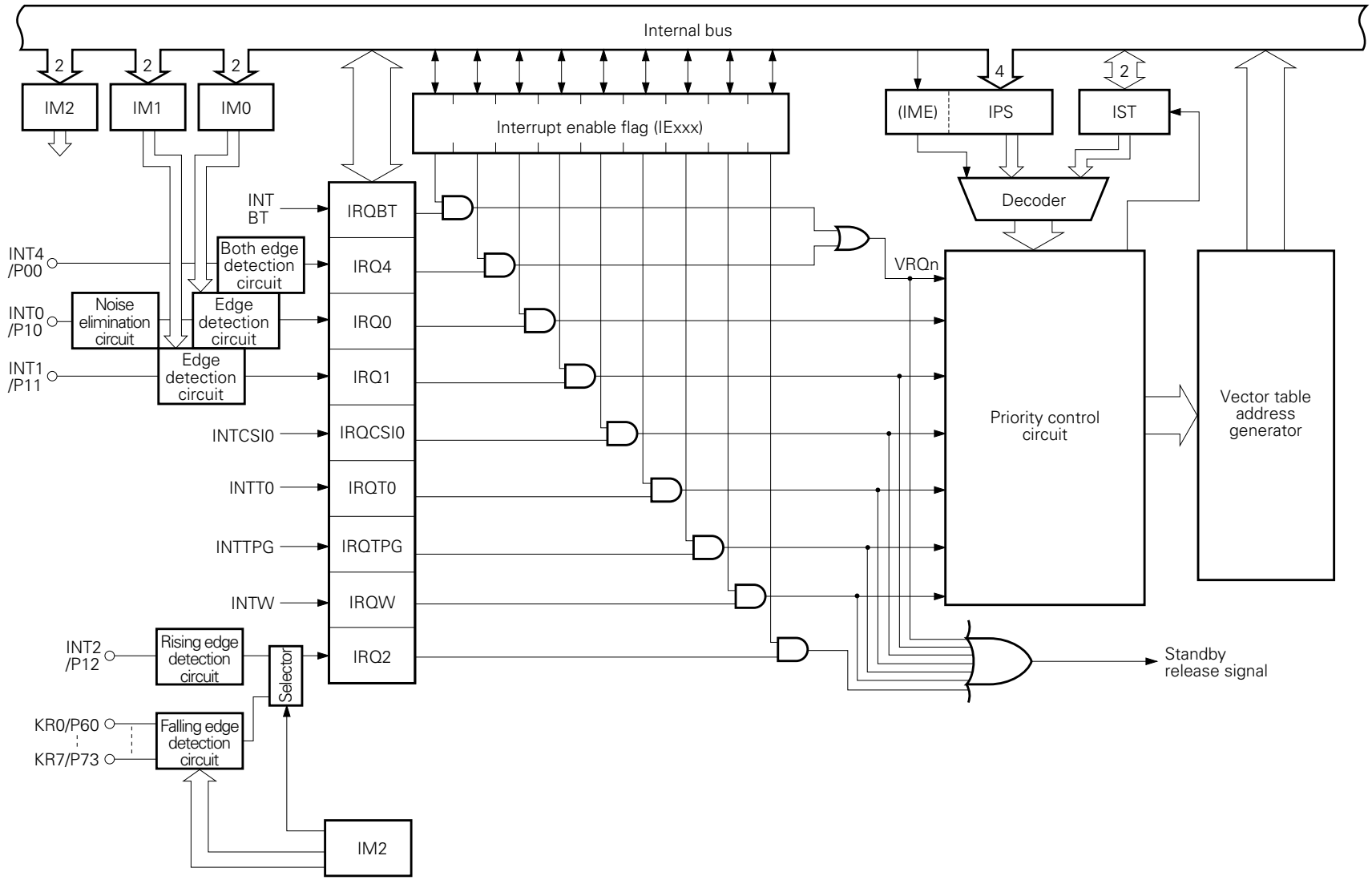


Fig. 6-1 Interrupt Control Block Diagram

7. STANDBY FUNCTIONS

In order to fully exploit the μPD75512(A) low power dissipation, CPU operation can be stopped by setting the unit to the standby mode, thus, further reducing power dissipation. The μPD75512(A) features two standby modes, a STOP mode and a HALT mode.

Table 7-1 Status in Standby Mode

Item \ Mode		STOP Mode	HALT Mode
Instruction for Setting		STOP instrtuction	HALT instruction
System Clock at the Time of Setting		Can be set only when operating on the main system clock	Can be set when operating either on the main system clock or the subsystem clock
Operation Status	Clock Oscillator	Only the main system clock can stop its operation.	Only the CPU clock Φ stops its operation. (oscillation continues)
	Basic Interval Timer	Does not operate	Operates (Sets IRQBT with the reference time interval)
	Serial Interface (Channel 0)	Can operate only when the external SCK0 input is selected as the serial clock	Operates when the timer system clock is operating or external SCK0 is selected
	Serial Interface (Channel 1)	Can operate only when the external SCK1 input is selected as the serial clock	Operates only when the main system clock is operating
	Timer/Event Counter	Can only operate when the TI0 pin input is selected as system clock	Operates only when the main system clock is operating
	Clock Timer	Operates when f_{XT} is selected as the count clock	Can operate
	A/D Converter	Does not operate	Operates only when the main system clock is operating
	Timer/Pulse Generator	Does not operate	Operates only when the main system clock is operating
	Timer/Pulse Generator	INT1, INT2, and INT4 can operate, but INT0 cannot operate	
	CPU	Does not operate	
Release Signal		An interrupt request signal from a piece of hardware, whose operation is enabled by the interrupt enable flag, or the RESET signal input	

8. RESET FUNCTIONS

When the $\overline{\text{RESET}}$ signal is input, the μPD75512(A) is reset and each hardware is initialized as indicated in Table 8-1. Fig. 8-1 shows the reset operation timing.

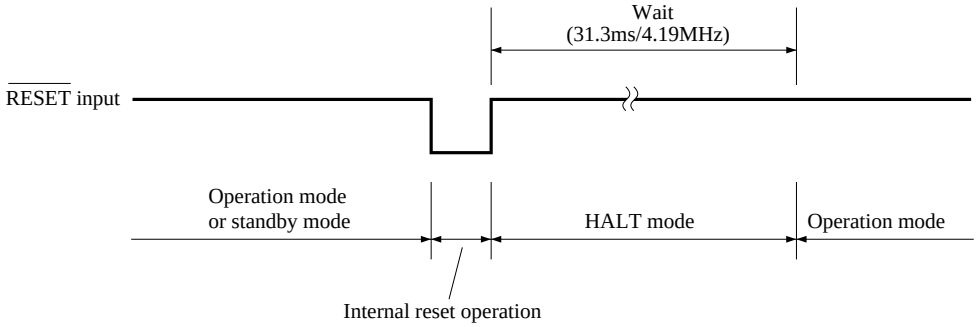


Fig. 8-1 Reset Operation by $\overline{\text{RESET}}$ Input

Table 8-1 Status of Each Hardware after Reset (1/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Program Counter (PC)		The contents of the lower 6 bits of address 0000H of the program memory are set to PC13-8, and the contents of address 0001H are set to PC7-0.	Same as left
PSW	Carry Flag (CY)	Retained	Undefined
	Skip Flag (SK0-2)	0	0
	Interrupt Status Flag (IST0, 1)	0	0
	Bank Enable Flag (MBE, RBE)	The contents of bit 6 of address 0000H of the program memory are set to RBE and those of bit 7 are set to MBE.	Same as left
Stack Pointer (SP)		Undefined	Undefined
Data Memory (RAM)		Retained *	Undefined
General-Purpose Register (X, A, H, L, D, E, B, C)		Retained	Undefined
Bank Selection Register (MBS, RBS)		0, 0	0, 0
Basic Interval Timer	Counter (BT)	Undefined	Undefined
	Mode Register (BTM)	0	0
Timer/Event Counter	Counter (T0)	0	0
	Modulo Register (TMOD0)	FFH	FFH
	Mode Register (TM0)	0	0
	TOE0, TOUT F/F	0, 0	0, 0
Timer/Pulse Generator	Modulo Register	Retained	Retained
	Mode Register	0	0
Watch Timer	Mode Register (WM)	0	0

*: Data of address 0F8H to 0FDH of the data memory becomes undefined when a $\overline{\text{RESET}}$ signal is input.

Table 8-1 Status of Each Hardware after Reset (2/2)

Hardware		$\overline{\text{RESET}}$ Input in Standby Mode	$\overline{\text{RESET}}$ Input during Operation
Serial Interface (Channel 0)	Shift Register (SIO0)	Retained	Undefined
	Operation Mode Register (CSIM0)	0	0
	SBI Control Register (SBIC)	0	0
	Slave Address Register (SVA)	Retained	Undefined
	P01/$\overline{\text{SCK0}}$ Output Latch	1	1
A/D Converter	Mode Regiseter (ADM), EOC	04H (EOC = 1)	04H (EOC = 1)
	SA Register	7FH	7FH
Clock Generator, Clock Output Circuit	Processor Clock Control Register (PCC)	0	0
	System Clock Control Register (SCC)	0	0
	Clock Output Mode Register (CLOM)	0	0
Serial Interface (Channel 1)	Shift Register (SIO1)	Retained	Undefined
	Operation Mode Register 1 (CSIM1)	0	0
	Serial Transfer End Flag (EOT)	0	0
Interrupt Function	Interrupt Request Flag (IRQxxx)	Reset (0)	Reset (0)
	Interrupt Enable Flag (IExxx)	0	0
	Interrupt Master Enable Flag (IME)	0	0
	INT0, INT1, INT2 Mode Registers (IM0, 1, 2)	0, 0, 0	0, 0, 0
Digital Port	Output Buffer	Off	Off
	Output Latch	Clear (0)	Clear (0)
	Input/Output Mode Register (PMGA, B, C)	0	0
	Pull-Up Resistor Specification Register (POGA)	0	0
Bit Sequential Buffer (BSB0-3)		Retained	Undefined

9. INSTRUCTION SET

(1) Operand representation and description

Describe one or more operands in the operand field of each instruction according to the operand representation and description methods of the instruction (for details, refer to RA75X Assembler Package User's Manual - Language (EEU-730)). With some instructions, only one operand should be selected from several operands. The uppercase characters, +, and – are keywords and must be described as is.

Describe an appropriate numeric value or label as immediate data.

Representation	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2 rp' rp'1	XA, BC, DE, HL BC, DE, HL BC, DE XA, BC, DE, HL, XA', BC', DE', HL' BC, DE, HL, XA', BC', DE', HL'
rpa rpa1	HL, HL+, HL–, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem bit	8-bit immediate data or label* 2-bit immediate data or label
fmem pmem	FB0H to FBFH,FF0H to FFFH immediate data or label FC0H to FFFH immediate data or label
addr caddr faddr	0000H to 2F7FH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H to 7FH immediate data (where bit0 = 0) or label
PORTn IExxx RBn MBn	PORT0 to PORT15 IEBT, IECSI0, IET0, IE0, IE1, IE2, IE4, IEW, IETPG RB0-RB3 MB0, MB1, MB15

*: Only even addresses can be described in mem when processing 8-bit data.

(2) Legend of operation field

A	:	A register; 4-bit accumulator
B	:	B register; 4-bit accumulator
C	:	C register; 4-bit accumulator
D	:	D register; 4-bit accumulator
E	:	E register; 4-bit accumulator
H	:	H register; 4-bit accumulator
L	:	L register; 4-bit accumulator
X	:	X register; 4-bit accumulator
XA	:	Register pair (XA); 8-bit accumulator
BC	:	Register pair (BC); 8-bit accumulator
DE	:	Register pair (DE); 8-bit accumulator
HL	:	Register pair (HL); 8-bit accumulator
XA'	:	Expanded register pair (XA')
BC'	:	Expanded register pair (BC')
DE'	:	Expanded register pair (DE')
HL'	:	Expanded register pair (HL')
PC	:	Program counter
SP	:	Stack pointer
CY	:	Carry flag; or bit accumulator
PSW	:	Program status word
MBE	:	Memory bank enable flag
RBE	:	Register bank enable flag
PORTn	:	Port n (n = 0 to 15)
IME	:	Interrupt mask enable flag
IPS	:	Interrupt priority selector register
IExxx	:	Interrupt enable flag
RBS	:	Memory bank selector register
MBS	:	Memory bank selector register
PCC	:	Processor clock control register
·	:	Delimiter of address and bit
(xx)	:	Contents addressed by xx
xxH	:	Hexadecimal data

(3) Symbols in addressing area field

*1	MB = MBE · MBS (MBS = 0, 1, 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H-FBFH, FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-2F7FH	Program memory addressing
*7	addr = (Current PC) – 15 to (Current PC) – 1 (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H-0FFFH ($PC_{13, 12}$ = 00B) or 1000H-1F7FH ($PC_{13, 12}$ = 01B) or 2000H-2F7FH ($PC_{13, 12}$ = 10B)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	

Remarks 1: MB indicates memory bank that can be accessed.

2: In *2, MB = 0 regardless of MBE and MBS.

3: In *4 and *5, MB = 15 regardless of MBE and MBS.

4: *6 to *10 indicate areas that can be addressed.

(4) Machine cycle field

In this field, S indicates the number of machine cycles required when an instruction having a skip function skips. The value of S varies as follows:

- When no instruction is skipped ..... S = 0
- When 1-byte or 2-byte instruction is skipped ..... S = 1
- When 3-byte instruction (BR ! addr or CALL ! addr) is skipped ..... S = 2

Note: The GETI instruction is skipped in one machine cycle.

One machine cycle equals to one cycle of the CPU clock Φ, (=t_{CY}), and can be changed in three steps depending on the setting of the processor clock control register (PCC).

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Transfer	MOV	A, #n4	1	1	A ← n4		String effect A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String effect A
		HL, #n8	2	2	HL ← n8		String effect B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @HL+	1	2+S	A ← (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ← (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A,mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg	2	2	A ← reg		
		XA, rp'	2	2	XA ← rp'		
		reg1, A	2	2	reg1 ← A		
		rp'1, XA	2	2	rp'1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @HL+	1	2+S	A ← (HL), then L ← L+1	*1	L = 0
		A, @HL–	1	2+S	A ← (HL), then L ← L–1	*1	L = FH
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp'	2	2	XA ↔ rp'		
Table Reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8}+XA)_{ROM}$		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Bit Transfer	MOV1	CY, fmem.bit	2	2	CY ← (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← (H+mem_{3-0}.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit) ← CY	*4	
		pmem.@L, CY	2	2	($pmem_{7-2}$+L_{3-2}.bit(L_{1-0})) ← CY	*5	
		@H+mem.bit, CY	2	2	(H+mem_{3-0}.bit) ← CY	*1	
Arithmetic Operation	ADDS	A,#n4	1	1+S	A ← A+n4		carry
		XA,#n8	2	2+S	XA ← XA+n8		carry
		A,@HL	1	1+S	A ← A+(HL)	*1	carry
		XA,rp'	2	2+S	XA ← XA+rp'		carry
		rp'1,XA	2	2+S	rp'1 ← rp'1+XA		carry
	ADDC	A,@HL	1	1	A,CY ← A+(HL)+CY	*1	
		XA,rp'	2	2	XA,CY ← XA+rp'+CY		
		rp'1,XA	2	2	rp'1,CY ← rp'1+XA+CY		
	SUBS	A,@HL	1	1+S	A ← A-(HL)	*1	borrow
		XA,rp'	2	2+S	XA ← XA-rp'		borrow
		rp'1,XA	2	2+S	rp'1 ← rp'1-XA		borrow
	SUBC	A,@HL	1	1	A,CY ← A-(HL)-CY	*1	
		XA,rp'	2	2	XA,CY ← XA-rp'-CY		
		rp'1,XA	2	2	rp'1,CY ← rp'1-XA-CY		
	AND	A,#n4	2	2	A ← A ∧ n4		
		A,@HL	1	1	A ← A ∧ (HL)	*1	
		XA,rp'	2	2	XA ← XA-rp'		
		rp'1,XA	2	2	rp'1 ← rp'1 ∧ XA		
	OR	A,#n4	2	2	A ← A ∨ n4		
		A,@HL	1	1	A ← A ∨ (HL)	*1	
		XA,rp'	2	2	XA ← XA ∨ rp'		
		rp'1,XA	2	2	rp'1 ← rp'1 ∨ XA		
	XOR	A,#n4	2	2	A ← A ⊻ n4		
		A,@HL	1	1	A ← A ⊻ (HL)	*1	
		XA,rp'	2	2	XA ← XA ⊻ rp'		
		rp'1,XA	2	2	rp'1 ← rp'1 ⊻ XA		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Accumulator Manipulation	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/ Decrement	INCS	reg	1	1+S	reg ← reg+1		reg = 0
		rp1	1	1+S	rp1 ← rp1+1		rp1 = 00H
		@HL	2	2+S	(HL) ← (HL)+1	*1	(HL) = 0
		mem	2	2+S	(mem) ← (mem)+1	*3	(mem) = 0
	DECS	reg	1	1+S	reg ← reg-1		reg = FH
		rp'	2	2+S	rp' ← rp'-1		rp' = FFH
Comparison	SKE	reg,#n4	2	2+S	Skip if reg = n4		reg = n4
		@HL,#n4	2	2+S	Skip if (HL) = n4	*1	(HL) = n4
		A,@HL	1	1+S	Skip if A = (HL)	*1	A = (HL)
		XA,@HL	2	2+S	Skip if XA = (HL)	*1	XA = (HL)
		A,reg	2	2+S	Skip if A = reg		A = reg
		XA,rp'	2	2+S	Skip if XA = rp'		XA = rp'
Carry Flag Manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1+S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Memory/ Bit Manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← 1	*5	
		@H+mem.bit	2	2	(H + mem_{3-0}.bit) ← 1	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0})) ← 0	*5	
		@H+mem.bit	2	2	(H+mem_{3-0}.bit) ← 0	*1	
	SKT	mem.bit	2	2+S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2+S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H + mem_{3-0}.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2+S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2+S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$ +L_{3-2}.bit (L_{1-0})) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2+S	Skip if (H + mem_{3-0}.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2+S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2+S	Skip if ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0})) = 1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2+S	Skip if (H+mem_{3-0}.bit) = 1 and clear	*1	(@H+mem.bit) = 1
	AND1	CY,fmem.bit	2	2	CY ← CY ∧ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∧ ($pmem_{7-2}$+L_{3-2}.bit(L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∧ (H+mem_{3-0}.bit)	*1	
	OR1	CY,fmem.bit	2	2	CY ← CY ∨ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ∨ ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ∨ (H+mem_{3-0}.bit)	*1	
	XOR1	CY,fmem.bit	2	2	CY ← CY ⊻ (fmem.bit)	*4	
		CY,pmem.@L	2	2	CY ← CY ⊻ ($pmem_{7-2}$+L_{3-2}.bit (L_{1-0}))	*5	
		CY,@H+mem.bit	2	2	CY ← CY ⊻ (H+mem_{3-0}.bit)	*1	
Branch	BR	addr	—	—	PC_{13-0} ← addr (The most suitable instruction is selectable from among BR !addr, BRCB !caddr, and BR $addr depending on the assembler.)	*6	
		!addr	3	3	PC_{13-0} ← addr	*6	
		$addr	1	2	PC_{13-0} ← addr	*7	
	BRCB	!caddr	2	2	PC_{13-0} ← $PC_{13,12}$+$caddr_{11-0}$	*8	
	BR	PCDE	2	3	PC_{13-0} ← PC_{13-8}+DE		
		PCXA	2	3	PC_{13-0} ← PC_{13-8}+XA		

Instructions	Mnemonics	Operand	Bytes	Machine Cycles	Operation	Addressing Area	Skip Conditions
Subroutine/ Stack Control	CALL	!addr	3	3	(SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, RBE, $PC_{13,12}$ PC_{13-0} ← addr, SP ← SP-4	*6	
	CALLF	!faddr	2	2	(SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, RBE, $PC_{13,12}$ PC_{13-0} ← 00, faddr, SP ← SP-4	*9	
	RET		1	3	MBE, RBE, $PC_{13,12}$ ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4		
	RETS		1	3+S	MBE, RBE, $PC_{13,12}$ ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) SP ← SP+4, then skip unconditionally		Undefined
	RETI		1	3	$PC_{13,12}$ ← (SP+1) PC_{11-0} ← (SP)(SP+3)(SP+2) PSW ← (SP+4)(SP+5), SP ← SP+6		
	PUSH	rp	1	1	(SP-1)(SP-2) ← rp, SP ← SP-2		
		BS	2	2	(SP-1) ← MBS, (SP-2) ← RBS, SP ← SP-2		
	POP	rp	1	1	rp ← (SP+1)(SP), SP ← SP+2		
		BS	2	2	MBS ← (SP+1), RBS ← (SP), SP ← SP+2		
Interrupt Control	EI		2	2	IME (IPS.3) ← 1		
		IExxx	2	2	IExxx ← 1		
	DI		2	2	IME (IPS.3) ← 0		
		IExxx	2	2	IExxx ← 0		
I/O	IN *1	A,PORTn	2	2	A ← $PORT_n$ (n = 0-15)		
		XA,PORTn	2	2	XA ← $PORT_{n+1}$,$PORT_n$ (n = 4, 6)		
	OUT *1	PORTn,A	2	2	$PORT_n$ ← A (n = 2-7, 9-14)		
		PORTn,XA	2	2	$PORT_{n+1}$,$PORT_n$ ← XA (n = 4, 6)		
CPU Control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS ← n (n = 0-3)		
		MBn	2	2	MBS ← n (n = 0, 1, 15)		
	GETI *2	taddr	1	3	· Where TBR instruction, PC_{13-0} ← $(taddr)_{4-0}$+(taddr+1)	*10	
					· Where TCALL instruction, (SP-4)(SP-1)(SP-2) ← PC_{11-0} (SP-3) ← MBE, RBE, $PC_{13,12}$ PC_{13-0} ← $(taddr)_{5-0}$+(taddr+1) SP ← SP-4		
					· Except for TBR and TCALL instructions, Instruction execution of (taddr)(taddr+1)		Depends on referenced instruction

*1: When executing the IN/OUT instruction, MBE = 0, or MBE = 1, and MBS = 15.

*2: The TBR, and TCALL instructions are the assembler pseudo-instructions for the table definition of GETI instruction.

10. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			-0.3 to +7.0	V
Input Voltage	V_{I1}	Other than ports 4, 5, 12-14		-0.3 to V_{DD}+0.3	V
	V_{I2}	Ports 4, 5, 12-14	w/pull-up resistor	-0.3 to V_{DD}+0.3	V
			Open drain	-0.3 to +11	V
Output Voltage	V_O			-0.3 to V_{DD}+0.3	V
High-Level Output Current	I_{OH}*	1 pin	Peak	-10	mA
			rms	-5	mA
		All pins	Peak	-30	mA
			rms	-15	mA
Low-Level Output Current	I_{OL}*	1 pin	Peak	10	mA
			rms	5	mA
		Total of ports 0, 2, 3, 4	Peak	100	mA
			rms	60	mA
		Total of ports 5-11	Peak	100	mA
			rms	60	mA
		Total of ports 12-14	Peak	40	mA
			rms	25	mA
Operating Temperature	T_{opt}			-40 to +85	°C
Storage Temperature	T_{stg}			-65 to +150	°C

*: rms = Peak value x $\sqrt{Duty}$

OPERATING SUPPLY VOLTAGE

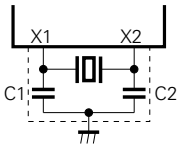
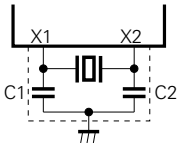
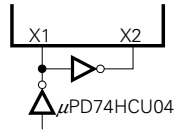
Parameter		Symbol	Conditions	MIN.	MAX.	Unit
A/D Converter	Supply voltage	V_{DD}		3.5	6.0	V
	Ambient temperature	T_a		-40	+85	°C
Timer/Pulse Generator	Supply voltage	V_{DD}		4.5	6.0	V
	Ambient temperatuare	T_a		-40	+85	°C
Other Circuits	Supply voltage	V_{DD}		2.7	6.0	V
	Ambient temperatuare	T_a		-40	+85	°C

CAPACITANCE (T_a = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_I	f = 1 MHz			15	pF
Output Capacitance	C_O	Pins other than thosemeasured are at 0 V			15	pF
Input/Output Capacitance	C_{IO}				15	pF

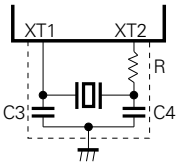
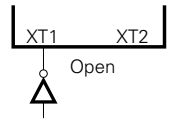
MAIN SYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic		Oscillation frequency(f_X)*1	V_{DD} = osccillation voltage range	1.0		5.0*3	MHz
		Oscillation stabilization time*2	After V_{DD} came to MIN. value of oscillation voltage range			4	ms
Crystal		Oscillation frequency (f_X)*1		1.0	4.19	5.0*3	MHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External Clock		X1 input frequency (f_X)*1		1.0		5.0*3	MHz
		X1 input high-, low-level widths (t_{XH}, t_{XL})		100		500	ns

SUBSYSTEM CLOCK OSCILLATOR CIRCUIT CHARACTERISTICS

(T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Oscillator	Recommended Constants	Item	Conditions	MIN.	TYP.	MAX.	Unit
Crystal		Oscillation*1 frequency (f_{XT})		32	32.768	35	kHz
		Oscillation stabilization time*2	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External Clock		XT1 input frequency (f_{XT})*1		32		100	kHz
		XT1 input high-, low-level widths (t_{XTH}, t_{XTL})		5		15	μs

*1: Only to express the characteristics of the oscillator circuit. For instruction execution time, refer to AC Characteristics.

2: Time required for oscillation to stabilize after V_{DD} reaches the minimum value of the oscillation voltage range or the STOP mode has been released.

3: When the oscillation frequency is 4.19 MHz < fx ≤ 5.0 MHz, do not select PCC = 0011 as the instruction execution time: otherwise, one machine cycle is set to less than 0.95 μs, falling short of the rated minimum value of 0.95 μs. ★

★ **Note:** When using the oscillation circuit of the main system clock and subsystem clock, wire the portion enclosed in dotted line in the figures as follows to avoid adverse influences on the wiring capacity:

- Keep the wiring length as short as possible.
- Do not cross the wiring over the other signal lines. Do not route the wiring in the vicinity of lines through which a high alternating current flows.
- Always keep the ground point of the capacitor of the oscillator circuit at the same potential as V_{SS}. Do not connect the ground pattern through which a high current flows.
- Do not extract signals from the oscillation circuit.

The amplification factor of the subsystem clock oscillation circuit is designed to be low to reduce the current dissipation and therefore, the subsystem clock oscillation circuit is influenced by noise more easily than the main system clock oscillation circuit. When using the subsystem clock, therefore, exercise utmost care in wiring the circuit.

DC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH1}	Ports 2, 3, 9-11, P80, P82		0.7V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7, 15, P81, P83, $\overline{RESET}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	Ports 4, 5, 12-14	w/pull-up resistor	0.7V_{DD}		V_{DD}	V
			Open-drain	0.7V_{DD}		10	V
	V_{IH4}	X1, X2, XT1		V_{DD}-0.5		V_{DD}	V
Low-level Input Voltage	V_{IL1}	Ports 2-5, 9-14, P80, P82		0		0.3V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7, 15, P81, P83, $\overline{RESET}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2, XT1		0		0.4	V
High-Level Output Voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = -1 mA		V_{DD}-1.0			V
		I_{OH} = -100 μA		V_{DD}-0.5			V
Low-Level Output Voltage	V_{OL}	Ports 3, 4, and 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 5 mA		0.2	1.0	V
		V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0, 1	Open-drain Pull-up resistor ≥ 1 kΩ			0.2V_{DD}	V
High-Level Input Leakage Current	I_{LIH1}	V_I = V_{DD}	Other than below			3	μA
	I_{LIH2}		X1, X2, XT1			20	μA
	I_{LIH3}	V_I = 9 V	Ports 4, 5, 12-14 (open-drain)			20	μA
Low-Level Input Leakage Current	I_{LIL1}	V_I = 0 V	Other than below			-3	μA
	I_{LIL2}		X1, X2, XT1			-20	μA
High-Level Output Leakage Current	I_{LOH1}	V_O = V_{DD}	Other than below			3	μA
	I_{LOH2}	V_O = 9 V	Ports 4, 5, 12-14 (open-drain)			20	μA
Low-Level Output Leakage Current	I_{LOL}	V_O = 0 V				-3	μA
Internal Pull-Up Resistor	R_{U1}	Ports 0, 1, 2, 3, 6, 7 (except P00) V_I = 0V	V_{DD} = 5.0 V±10%	15	40	80	kΩ
			V_{DD} = 3.0 V±10%	30		300	kΩ
	R_{U2}	Ports 4, 5, 12-14 V_O = V_{DD}-2.0 V	V_{DD} = 5.0 V±10%	15	40	70	kΩ
			V_{DD} = 3.0 V±10%	10		60	kΩ
Internal Pull-Down Resistor	R_D	V_O = 2 V	Port 9	20	70	140	kΩ

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply Current *1	I_{DD1}	4.19 MHz*2 crystal oscillator C1 = C2 = 22pF	Ooperation mode	V_{DD} = 5 V±10%*3		3	9	mA
				V_{DD} = 3 V±10%*4		0.55	1.5	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V±10%		600	1800	μA
				V_{DD} = 3 V±10%		200	600	μA
	I_{DD3}	32.768 kHz*5 crystal oscillator	Operation mode	V_{DD} = 3 V±10%		40	120	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V±10%		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V±10%			0.5	20	μA
			V_{DD} = 3 V±10%			0.3	10	μA
				T_a = 25°C			5	μA

*1: Currents for the built-in pull-up resistor are not included.

2: Including when the subsystem clock is operated.

3: When operand in the high-speed mode with the processor clock control register (PCC) set to 0011.

4: When operated in the low-speed mode with the PCC set to 0000.

5: When operated with the subsystem clock by setting the system clock control register (SCC) to 1001 to stop the main system clock operation.

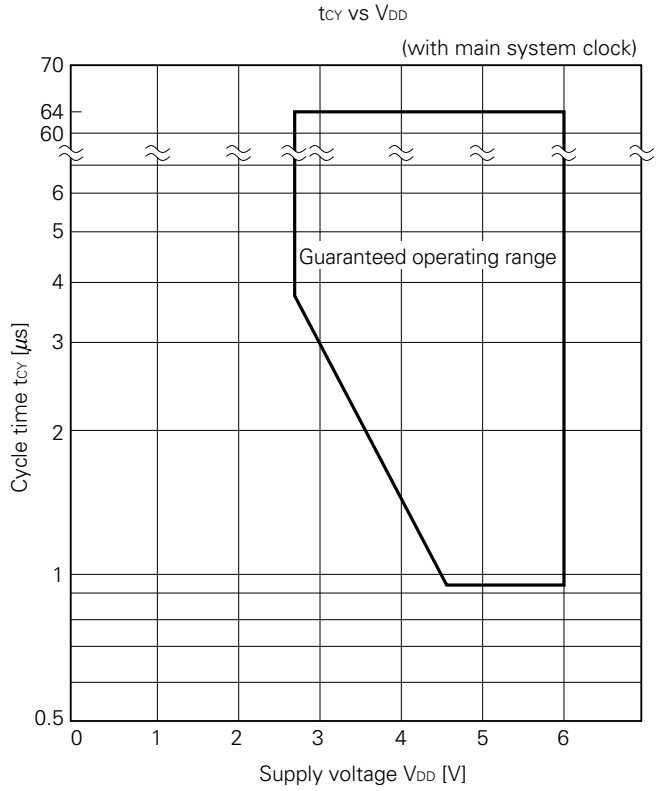
AC CHARACTERISTICS (T_a = -40 to +85°C, V_{DD} = 2.7 to 6.0 V)

(1) Basic Operation

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU Clock Cycle Time*1 (Minimum Instruction Execution Time = 1 Machine Cycle)	t_{CY}	w/main system clock	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		w/sub-system clock		114	122	125	μs
TI0 Input Frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 Input High-, Low-Level Widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt Input High-, Low-Level Widths	t_{INTH}, t_{INTL}	INT0		*2			μs
		INT1, 2, 4		10			μs
		KR0-7		10			μs
$\overline{RESET}$ Low-Level Width	t_{RSL}			10			μs

*1: The CPU clock (Φ) cycle time is determined by the oscillation frequency of the connected oscillator, system clock control register (SCC), and processor clock control register (PCC). The figure on the right is cycle time t_{CY} vs. supply voltage V_{DD} characteristics at the main system clock.

2: $2t_{CY}$ or $128/f_X$ depending on the setting of the interrupt mode register (IM0).



(2) Serial Transfer Operation

(a) Two-Line and Three-Line Serial I/O Modes ($\overline{SCK}$: internal clock output)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL1}	V_{DD} = 4.5 to 6.0 V		(t_{KCY1}/2)-50			ns
	t_{KH1}			(t_{KCY1}/2)-150			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK1}			150			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI1}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			250	ns
						1000	ns

*: R_L and C_L are load resistance and load capacitance of the SO output line.

(b) Two-Line and Three-Line Serial I/O Modes ($\overline{SCK}$: external clock input)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK2}			100			ns
SI Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI2}			400			ns
$\overline{SCK}$ ↓→ SO Output Delay Time	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

*: R_L and C_L are load resistance and load capacitance of the SO output line.

(c) SBI Mode ($\overline{SCK}$: internal clock output (master))

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V	1600			ns
			3800			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL3} t_{KH3}	V_{DD} = 4.5 to 6.0 V	t_{KCY3}/2-50			ns
			t_{KCY3}/2-150			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK3}		150			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI3}		t_{KCY3}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO3}	V_{DD} = 4.5 to 6.0 V	0		250	ns
			0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}		t_{KCY3}			ns
SB0,1 ↓→ $\overline{SCK}$	t_{SBK}		t_{KCY3}			ns
SB0, 1 Low-Level Width	t_{SBL}		t_{KCY3}			ns
SB0, 1 High-Level Width	t_{SBH}		t_{KCY3}			ns

(d) SBI Mode ($\overline{SCK}$: external clock input (slave))

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK}$ Cycle Time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ High-, Low-Level Widths	t_{KL4} t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
				1600			ns
SB0, 1 Set-Up Time (vs. $\overline{SCK}$ ↑)	t_{SIK4}			100			ns
SB0, 1 Hold Time (vs. $\overline{SCK}$ ↑)	t_{KSI4}			t_{KCY4}/2			ns
$\overline{SCK}$ ↓→ SB0, 1 Output Delay Time	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
$\overline{SCK}$ ↑→ SB0, 1 ↓	t_{KSB}			t_{KCY4}			ns
SB0,1 ↓→ $\overline{SCK}$ ↓	t_{SBK}			t_{KCY4}			ns
SB0, 1 Low-Level Width	t_{SBL}			t_{KCY4}			ns
SB0, 1 High-Level Width	t_{SBH}			t_{KCY4}			ns

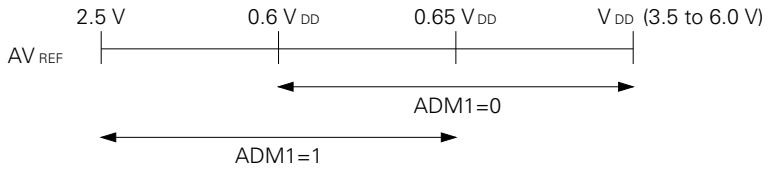
*: R_L and C_L are load resistance and load capacitance of the SO output line.

(3) A/D Converter (T_a = -40 to +85°C, V_{DD} = 3.5 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Absolute Accuracy*1		2.5 V ≤ AV_{REF} ≤ V_{DD}*2			±2.0	LSB
Conversion Time*3	t_{CONV}				168/f_X	μs
Sampling Time*4	t_{SAMP}				44/f_X	μs
Analog Input Voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Analog Input Impedance	R_{AN}			1000		MΩ
AV_{REF} Current	AI_{REF}			1.0	2.0	mA

*1: Absolute accuracy excluding quantization error ($\pm\frac{1}{2}$LSB)

2: Set ADM1 as follows, in respect to the reference voltage of the AD converter (AV_{REF}).

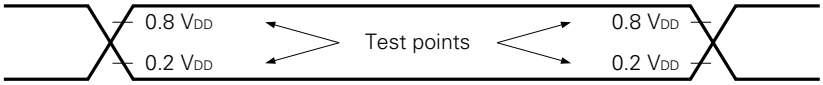


ADM1 can be set to either 0 or 1 when 0.6V_{DD} ≤ AV_{REF} ≤ 0.65V_{DD}

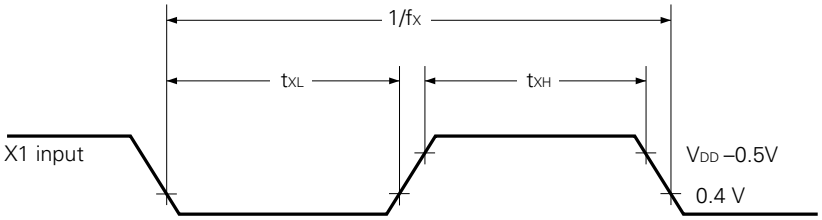
3: Time since execution of conversion start instruction until EOC = 1 (40.1 μs: f_X = 4.19 MHz)

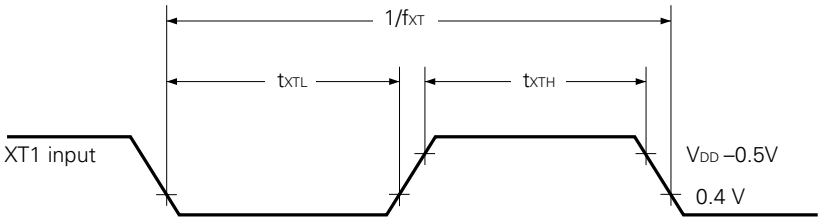
4: Time since execution of conversion start instruction until end of sampling (10.5 μs: f_X = 4.19 MHz)

AC TIMING TEST POINT (excluding X1 and XT1 inputs)

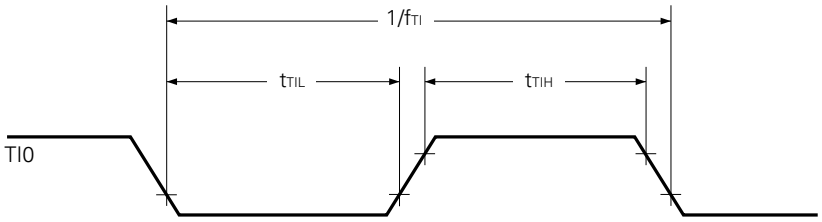


CLOCK TIMING



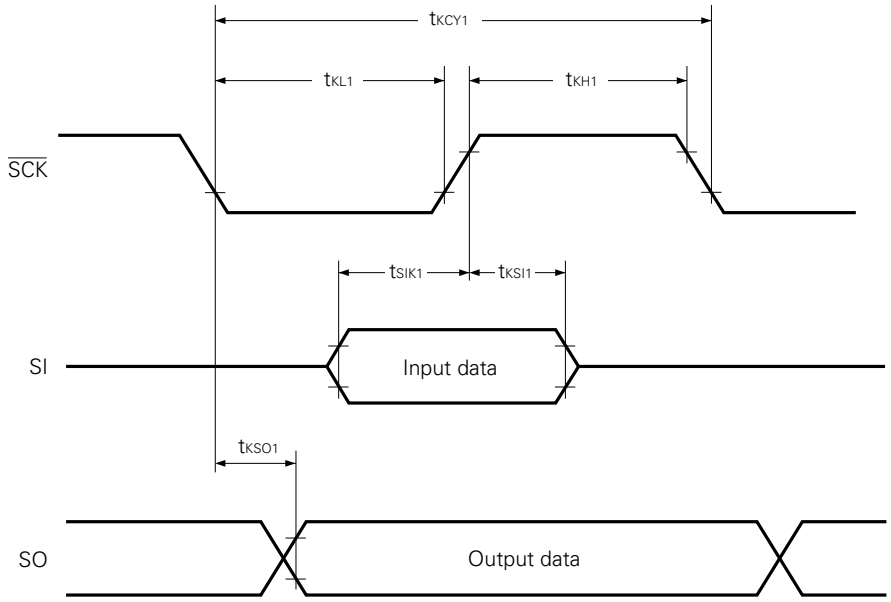


TI0 TIMING

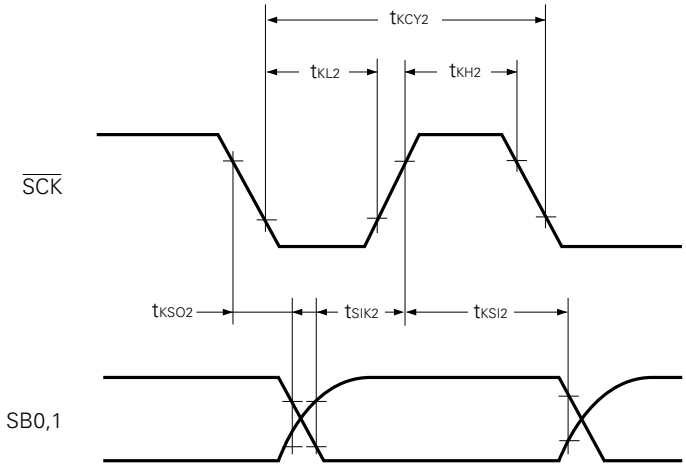


SERIAL TRANSFER TIMING

THREE-LINE SERIAL I/O MODE:

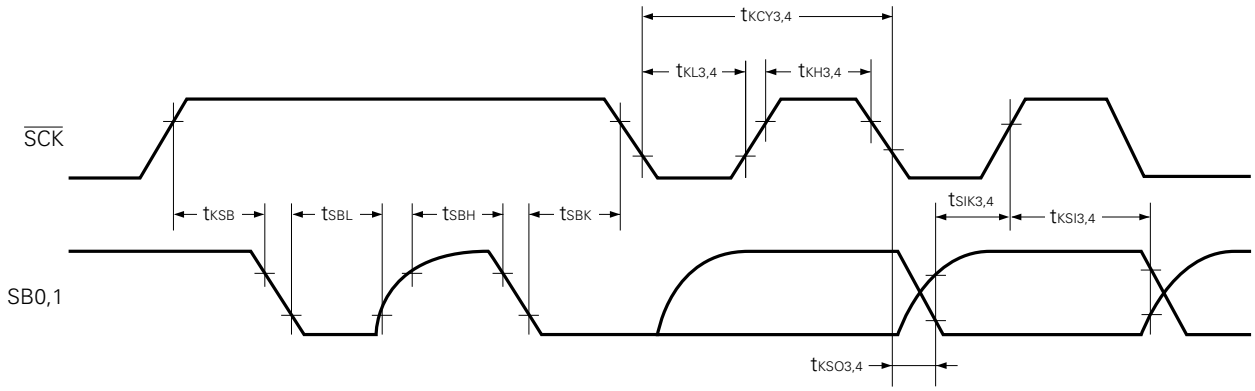


TWO-LINE SERIAL I/O MODE:

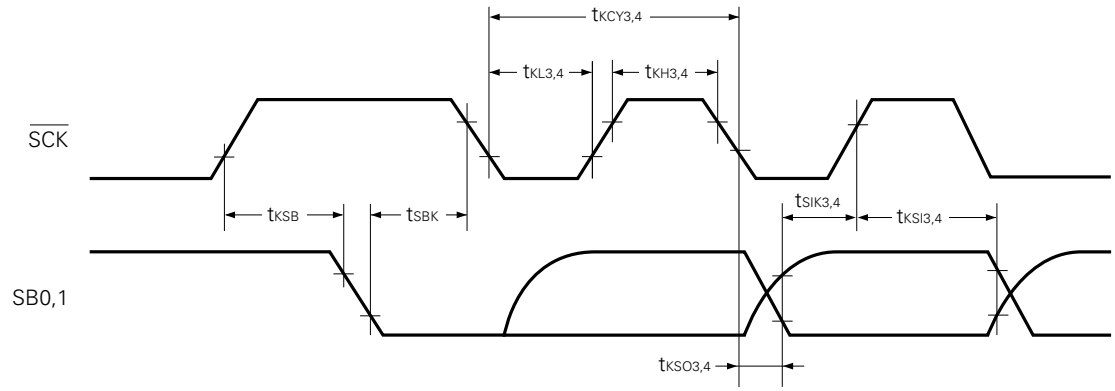


SERIAL TRANSFER TIMING

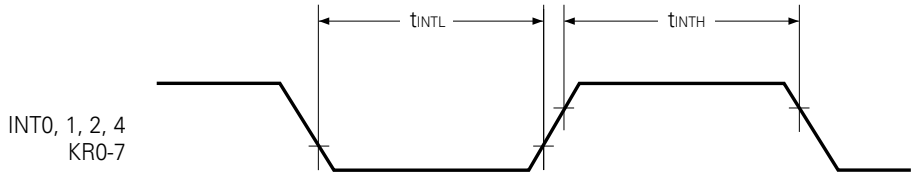
BUS RELEASE SIGNAL TRANSFER:



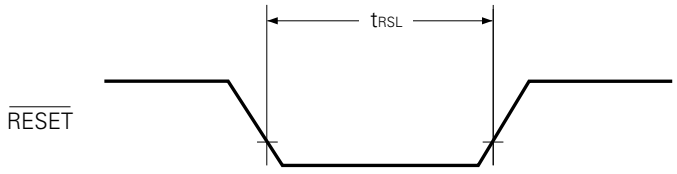
COMMAND SIGNAL TRANSFER:



INTERRUPT INPUT TIMING



RESET INPUT TIMING:



LOW-VOLTAGE DATA RETENTION CHARACTERISTICS OF DATA MEMORY IN STOP MODE

(T_a = −40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data Retention Supply Voltage	V_{DDDR}		2.0		6.0	V
Data Retention Supply Current*1	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release Signal Set Time	t_{SREL}		0			μs
Oscillation Stabilization Wait Time*2	t_{WAIT}	Released by $\overline{RESET}$		$2^{17}/f_X$		ms
		Released by interrupt		*3		ms

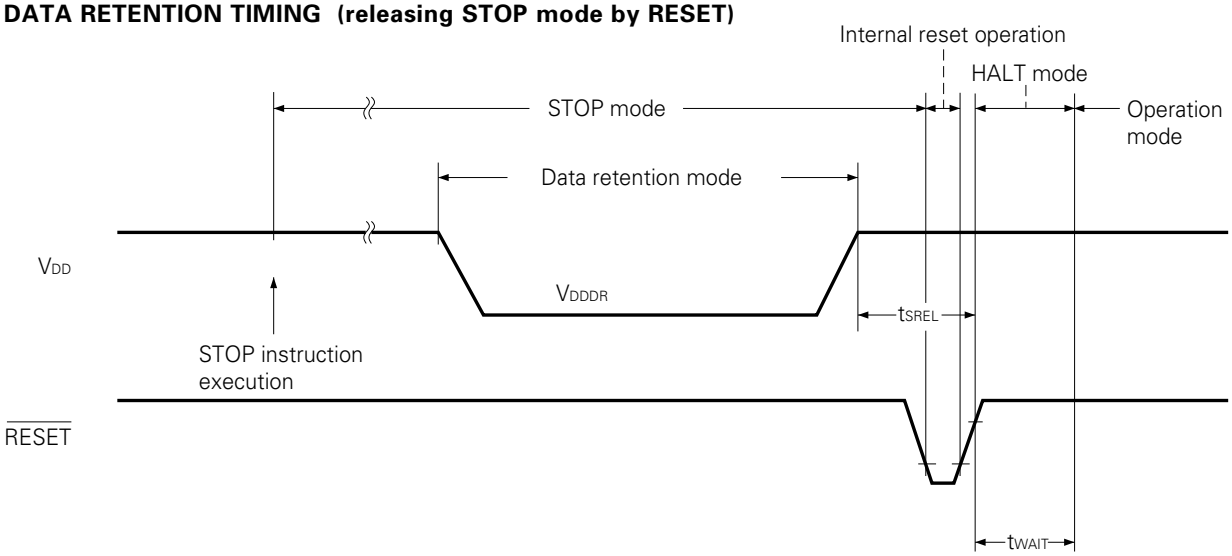
*1: Does not include current flowing through internal pull-up resistor

2: The oscillation stabilization wait time is the time during which the CPU is stopped to prevent unstable operation when oscillation is started.

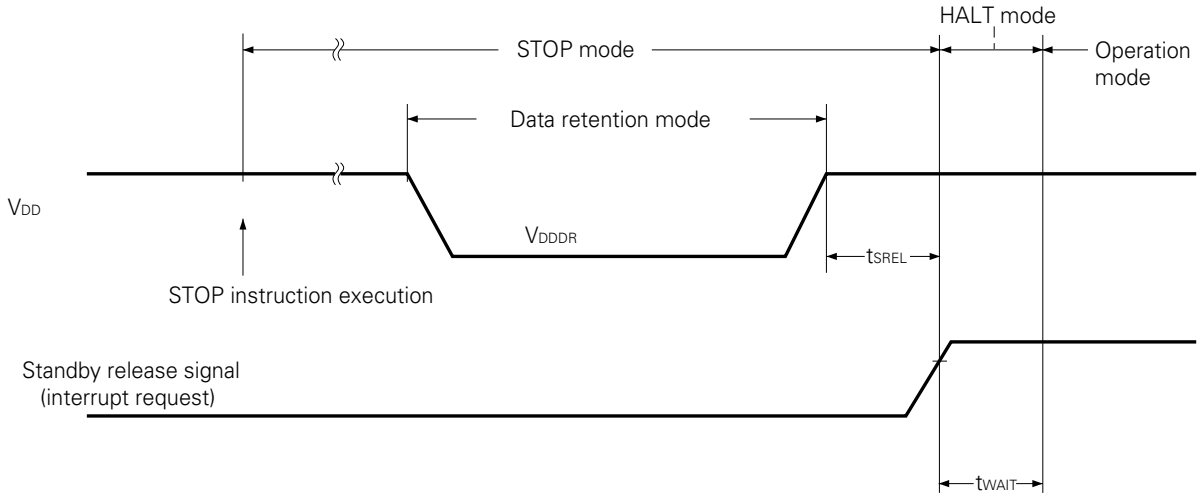
3: Depends on the setting of the basic interval timer mode register (BTM) as follows:

BTM3	BTM2	BTM1	BTM0	WAIT time ( ): f_X = 4.19 MHz
–	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
–	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
–	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
–	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

DATA RETENTION TIMING (releasing STOP mode by $\overline{RESET}$)

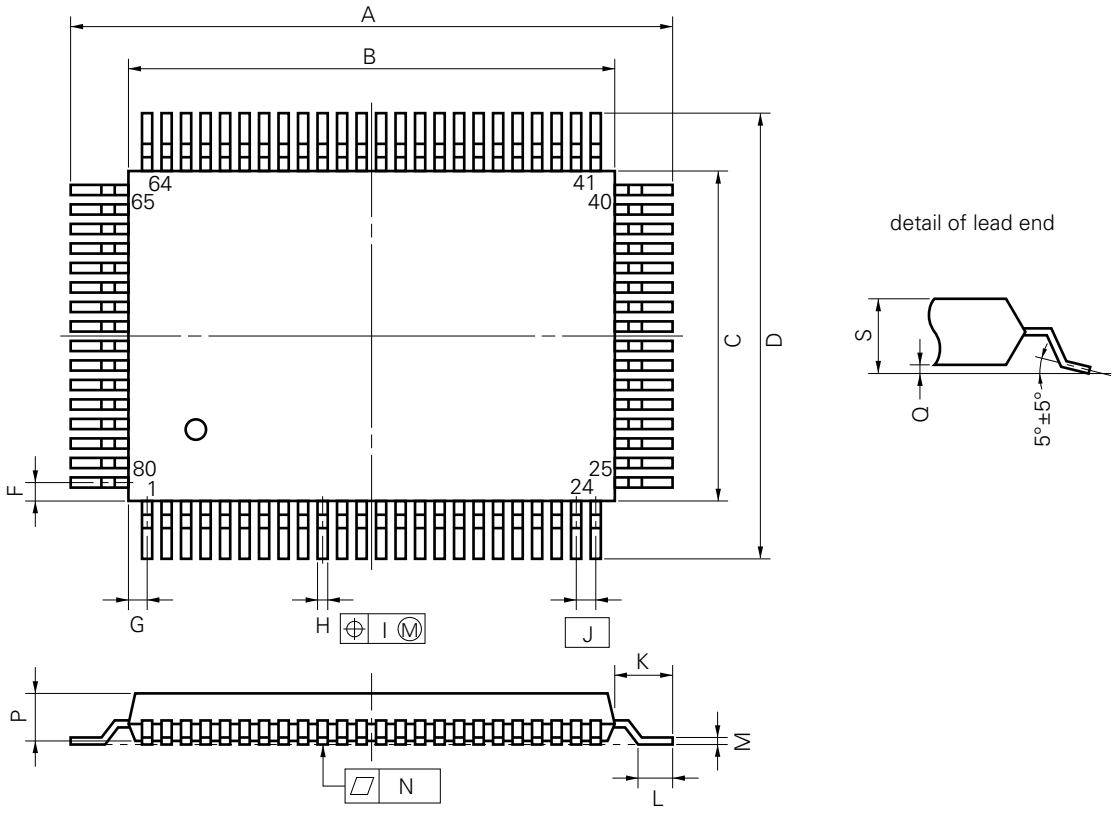


DATA RETENTION TIMING (standby release signal: releasing STOP mode by interrupt)



11. PACKAGE DRAWINGS

80 PIN PLASTIC QFP (14×20)



P80GF-80-3B9-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	0.8	0.031
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

12. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD75512(A) be soldered under the following conditions.

For details on the recommended soldering conditions, refer to Information Document "Semiconductor Devices Mounting Manual" (IEI-616).

For other soldering methods and conditions, consult NEC.

Table 12-1 Soldering Conditions of Surface Mount Type

μPD75512GF(A)-xxx-3B9: 80-pin plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared Reflow	Package peak temperature: 230°C, time: 30 seconds max. (210°C min.), number of times: 1	IR30-00-1
VPS	Package peak temperature: 215°C, time: 40 seconds max. (200°C min.), number of times: 1	VP15-00-1
Wave Soldering	Soldering bath temperature: 260°C max., time: 10 seconds max., number of times: 1, pre-heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Pin Partial Heating	Pin temperature: 300°C max., time: 3 seconds max. (per side)	—

Caution: Do not use two or more soldering methods in combination (except the pin partial heating method).

Notice

A model that can be soldered under the more stringent conditions (infrared reflow peak temperature: 235°C, number of times: 2, and an extended number of days) is also available. For details, consult NEC.

APPENDIX A. FUNCTIONAL DIFFERENCES AMONG μPD755XX(A) SERIES PRODUCTS

Item \ Product		μPD75512(A)	μPD75516(A)	μPD75P516
ROM Configuration		Mask ROM		EPROM/One-time PROM
ROM (Bit)		12160 x 8	16256 x 8	16256 x 8
RAM (Bit)		512 x 4		
Mask Option		• Ports 4, 5, 12, 14 are provided with internal pull-up resistors. • Port 9 is provided with an internal pull-down resistor.		Not provided
V_{PP}, PROM, Pins for programming		Not provided		Provided
LED Direct Drive		Not offered		Offered
Electrical Specifications	Supply Voltage Range	2.7 to 6.0 V		4.75 to 5.5 V
	Absolute Maximum Ratings	Differ in high-level / low-level output current		
	DC Characteristics	Differ in low-level output voltage		
	A/D Converter Characteristics	Differ in ambient temperature range and absolute accuracy		
Quality Grade		Special		Standard
Package		80-pin plastic QFP (14 x 20 mm)		• 80-pin plastic QFP (14 x 20 mm) • 80-pin ceramic WQFN

APPENDIX B. DEVELOPMENT TOOLS

The following development support tools are readily available to support development of systems using μPD75512(A):

Hardware	IE-75000-R *1 IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM *2	Emulation board for IE-75000-R and IE-75001-R
	EP-75516GF-R EV-9200G-80	Emulation prove for μPD75512(A), provided with 80-pin conversion socket EV-9200G-80.
	PG-1500	PROM programmer
	PA-75P516GF	PROM programmer adapter solely used for μPD75P516GF. It is connected to PG-1500.
Software	IE Control Program	Host machine PC-9800 series (MS-DOS™ Ver.3.30 to Ver.5.00A*3) IBM PC/AT™ (PC DOS™ Ver.3.1)
	PG-1500 Controller	
	RA75X Relocatable Assembler	

*1: Maintenance product

2: Not provided with IE-75001-R.

3: Ver.5.00/5.00A has a task swap function, but this function cannot be used with this software.

Remarks: For development tools from other companies, refer to 75X Series Selection Guide (IF-151).

APPENDIX C. RELATED DOCUMENTS ★

[MEMO]

GENERAL NOTES ON CMOS DEVICES

① STATIC ELECTRICITY (ALL MOS DEVICES)

Exercise care so that MOS devices are not adversely influenced by static electricity while being handled.

The insulation of the gates of the MOS device may be destroyed by a strong static charge. Therefore, when transporting or storing the MOS device, use a conductive tray, magazine case, or conductive buffer materials, or the metal case NEC uses for packaging and shipment, and use grounding when assembling the MOS device system. Do not leave the MOS device on a plastic plate and do not touch the pins of the device.

Handle boards on which MOS devices are mounted similarly .

② PROCESSING OF UNUSED PINS (CMOS DEVICES ONLY)

Fix the input level of CMOS devices.

Unlike bipolar or NMOS devices, if a CMOS device is operated with nothing connected to its input pin, intermediate level input may be generated due to noise, and an inrush current may flow through the device, causing the device to malfunction. Therefore, fix the input level of the device by using a pull-down or pull-up resistor. If there is a possibility that an unused pin serves as an output pin (whose timing is not specified), each pin should be connected to V_{DD} or GND through a resistor.

Refer to “Processing of Unused Pins” in the documents of each devices.

③ STATUS BEFORE INITIALIZATION (ALL MOS DEVICES)

The initial status of MOS devices is undefined upon power application.

Since the characteristics of an MOS device are determined by the quantity of injection at the molecular level, the initial status of the device is not controlled during the production process. The output status of pins, I/O setting, and register contents upon power application are not guaranteed. However, the items defined for reset operation and mode setting are subject to guarantee after the respective operations have been executed.

When using a device with a reset function, be sure to reset the device after power application.

[MEMO]

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