# Mobile Pentium® Processor Application Clock Generator with SSCG, USB and Power Management Support

## Product Features

- Supports clock requirements for Mobile Pentium® Processor
- 2 Host and 5 PCI clocks
- Separate supply pins for mixed (3.3/2.5V) voltage application.
- <175ps skew among CPU clocks.
- < 250ps skew among PCI clocks.
- 48mhz for USB.
- 28-pin SSOP package for minimum board space.
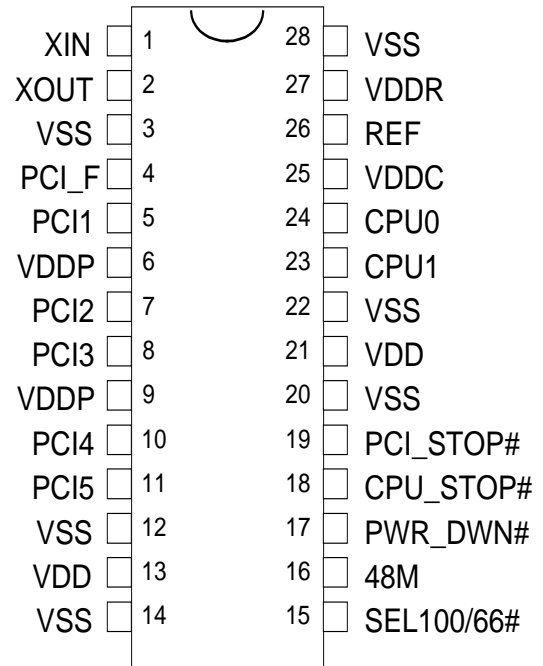- Power management capabilities

### Frequency Table

| SEL100/66# | CPU | PCI |
|---|---|---|
| 0 | 66.4 Mhz* | 33.3 Mhz |
| 1 | 99.8 Mhz** | 33.2 MHz |

*Down Spread 1.25% (total); **Down Spread .5% (total)

## Block Diagram
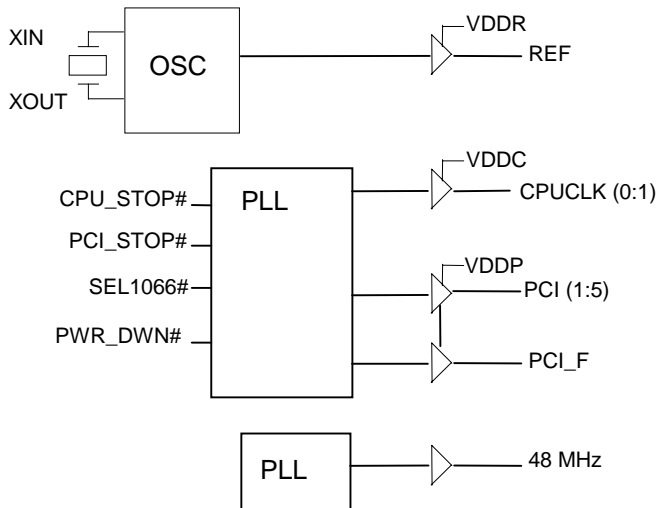


## Pin Configuration

## Mobile Pentium® Processor Application Clock Generator with SSCG, USB and Power Management Support

### Pin Description

| PIN No. | Pin Name | PWR | I/O | TYPE | Description |
|---|---|---|---|---|---|
| 1 | **XIN** | VDD | I | OSC1 | On-chip reference oscillator input pin. Requires either an external parallel resonant crystal (nominally 14.318 MHz) or externally generated reference signal |
| 2 | **XOUT** | VDD | O | OSC1 | On-chip reference oscillator output pin. Drives an external parallel resonant crystal. When an externally generated reference signal is used at Xin, this pin is left unconnected |
| 15 | **SEL100/66#** | - | I | PADI4 | Frequency select input pins.  See frequency select table on page 1. |
| 23, 24 | **CPUCLK (0:1)** | VDDC | O | BUF1 | Clock outputs. CPU frequency table specified on page 1. |
| 4 | **PCI_F** | VDDP | O | BUF4 | Free running PCI clock. When PCI_STP# = 0, this clock does NOT stop. |
| 16 | **48M** | VDD48 | O | BUF3 | 48 MHz fixed clock. |
| 5, 7, 8, 10, 11 | **PCI(1:5)** | VDDP | O | BUF4 | PCI bus clocks. See frequency select table on page 1. |
| 26 | **REF** | VDDR | O | BUF3 | Buffered outputs of on-chip reference oscillator. |
| 19 | **PCI_STOP#** | - | I | PAD PU | When driven to a logic low level, this pin will synchronously stop all PCI clocks (except PCI_F) at a logic low level. |
| 18 | **CPU_STOP#** | - | I | PAD PU | When driven to a logic low level, this pin will synchronously stop all CPU clocks at a logic low level. |
| 17 | **PWR_DWN#** | - | I | PAD PU | This pin is active low.  When asserted low, the device is in shutdown mode.  VCO's, Crystal, and outputs are turned off. |
| 13, 21 | **VDD** | - | P | - | 3.3 volt power supply for core logic. |
| 3, 12, 14, 20, 22, 28 | **VSS** | - | P | - | Ground pins for the device. |
| 9, 6 | **VDDP** | - | P | - | 3.3 Volt power supply pins for PCI (1:5) and PCI_F clock output buffers. |
| 25 | **VDDC** | - | P | - | 3.3 or 2.5 Volt power supply for CPUCLK (0:1) outputs. |
| 27 | **VDDR** | - | P | | 3.3 Volt power supply pins for reference clock output buffers and crystal circuit. |

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## Mobile Pentium® Processor Application Clock Generator with SSCG, USB and Power Management Support

## Power Management Functions

All PCI (excluding PCI_F) and CPU clocks can be enabled or stopped via the PCI_STOP# and CPU_STOP# input pins. All clocks are stopped in the low state. All clocks maintain a valid high period on transitions from running to stopped and on transitions from stopped to running when the chip was not powered down. On power up, the VCOs will stabilize to the correct pulse widths within 0.2 mS. The CPU and PCI clocks transition between running and stopped by waiting for one positive edge on PCI_F followed by a negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

| PWR_DWN# | CPU_STOP# | PCI_STOP# | CPUCLK | PCICLK | OTHER CLKs | XTAL & VCOs |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | LOW | LOW | RUNNING | RUNNING |
| 1 | 0 | 1 | LOW | RUNNING | RUNNING | RUNNING |
| 1 | 1 | 0 | RUNNING | LOW | RUNNING | RUNNING |
| 1 | 1 | 1 | RUNNING | RUNNING | RUNNING | RUNNING |
| 0 | x (don't care) | x (don'tcare) | LOW | LOW | LOW | OFF |

## Power Management Timing
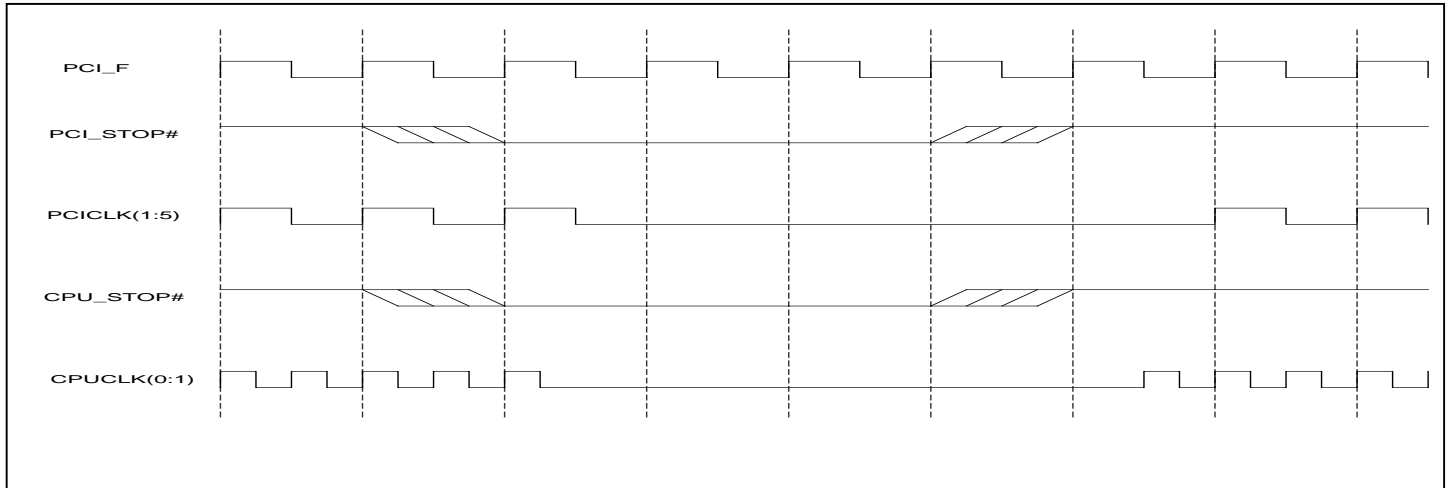


## Power Management Timing

| Signal | Signal State | Latency | |
|---|---|---|---|
| | | **No. of rising edges of free running PCICLK (PCIF)** | |
| CPU_ST0P# | 0 (disabled) | 1 | |
| | 1 (enabled) | 1 | |
| PCI_ST0P# | 0 (disabled) | 1 | |
| | 1 (enabled) | 1 | |

NOTES:
1. Clock on/off latency is defined in the number of rising edges of free running PCI CLOCK between the clock disable goes low/high to the first valid clock comes out of the device.

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## Spectrum Spread Clocking

### Down Spread
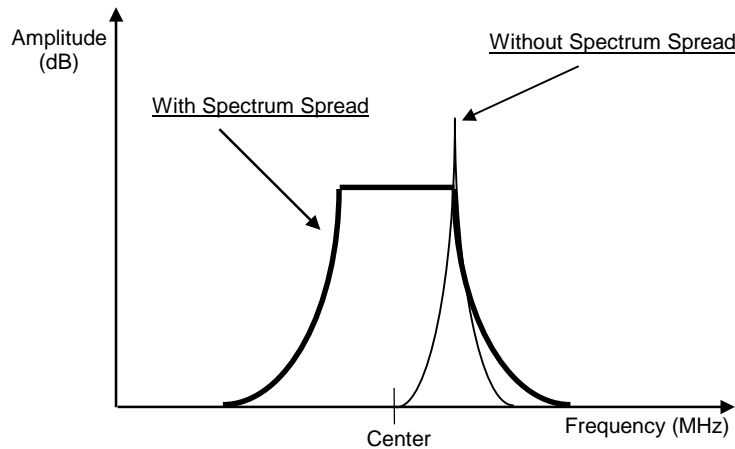


**Spectrum Analysis**

## Maximum Ratings

| | |
|---|---|
| Voltage Relative to VSS: | -0.3V |
| Voltage Relative to VDD: | 0.3V |
| Storage Temperature: | -65ºC to + 150ºC |
| Operating Temperature: | 0ºC to +70ºC |
| Maximum Power Supply: | 7V |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

$$VSS<(Vin \text{ or } Vout)<VDD$$

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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## Electrical Characteristics

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Input Low Voltage | VIL | - | - | 0.8 | Vdc | - |
| Input High Voltage | VIH | 2.0 | - | - | Vdc | - |
| Input Low Current | IIL | | | -66 | µA | |
| Input High Current | IIH | | | 5 | µA | |
| Output Low Voltage IOL = 4mA | VOL | - | - | 0.4 | Vdc | All Outputs (see buffer spec) |
| Output High Voltage IOH = 4mA | VOH | 2.4 | - | - | Vdc | All Outputs Using 3.3V Power (see buffer spec) |
| Tri-State leakage Current | Ioz | - | - | 10 | µA | |
| Dynamic Supply Current | Idd | - | - | 140 | mA | CPU = 66.6 MHz, PCI = 33.3 MHz |
| Static Supply Current | Isdd | - | - | 70 | µA | pwr_dwn# (PIN17) = 0 |
| Short Circuit Current | ISC | 25 | - | - | mA | 1 output at a time - 30 seconds |
| **VDD = VDDP=VDDR =3.3V ±5%, VDDC = 2.5V ±5%,  TA = 0ºC to +70ºC** | | | | | | |

## Switching Characteristics

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Output Duty Cycle | - | 45 | 50 | 55 | % | Measured at 1.5V |
| CPU to PCI Offset | tOFF | 1 | 3 | 4 | ns | 15 pf Load Measured at 1.5V |
| Buffer out Skew All CPU and PCI Buffer Outputs | tSKEW | - | - | 250 | ps | 15 pf Load Measured at 1.5V |
| ΔPeriod Adjacent Cycles | ΔP | - | - | ±250 | ps | - |
| Jitter Spectrum   20 dB Bandwidth from Center | BW$_J$ | | | 500 | KHz | |
| **VDD = VDDP =VDDR =3.3V ±5%, VDDC = 2.5V ±5%,  TA = 0ºC to +70ºC** | | | | | | |

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## Buffer Characteristics

### Buffer Characteristics for CPUCLK(0:1)

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $IOH_{min}$ | -40 | - | - | mA | Vout = VDD – 0.5V |
| Pull-Up Current Max | $IOH_{max}$ | -74 | - | - | mA | Vout = 1.25V |
| Pull-Down Current Min | $IOL_{min}$ | 55 | - | - | mA | Vout = 0.4V |
| Pull-Down Current Max | $IOL_{max}$ | 75 | - | - | mA | Vout = 0.6V |
| Dynamic Output Impedance | $Z_o$ | 10 | - | 15 | Ohms | 66 and 100 MHz |
| Rise Time Between 0.4 V and 2.0 V | TR | 0.4 | - | 1.6 | nS | 20 pF Load |
| Fall Time Between 0.4 V and 2.0 V | TF | 0.5 | - | 1.6 | nS | 20 pF Load |
| **VDD = VDDP= VDDR =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC** | | | | | | |

### Buffer Characteristics for REF, 48M

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $IOH_{min}$ | -13 | - | - | mA | Vout = VDD – 0.5V |
| Pull-Up Current Max | $IOH_{max}$ | -30 | - | - | mA | Vout = 1.5V |
| Pull-Down Current Min | $IOL_{min}$ | 13 | - | - | mA | Vout = 0.4V |
| Pull-Down Current Max | $IOL_{max}$ | 30 | - | - | mA | Vout = 1.5V |
| Dynamic Output Impedance | $Z_o$ | 18 | - | 25 | Ohms | 66 and 100 MHz |
| Rise Time Between 0.4 V and 2.4 V | TR | 0.5 | - | 2.0 | nS | 20 pF Load |
| Fall Time Between 0.4 V and 2.4 V | TF | 0.5 | - | 2.0 | nS | 20 pF Load |
| *VDD = VDDP= VDDR =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC* | | | | | | |

### Buffer Characteristics for PCI_F, PCI(1:5)

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Pull-Up Current Min | $IOH_{min}$ | -18 | - | - | mA | Vout = VDD – 0.5V |
| Pull-Up Current Max | $IOH_{max}$ | -44 | - | - | mA | Vout = 1.5V |
| Pull-Down Current Min | $IOL_{min}$ | 18 | - | - | mA | Vout = 0.4V |
| Pull-Down Current Max | $IOL_{max}$ | 50 | - | - | mA | Vout = 1.5V |
| Dynamic Output Impedance | $Z_o$ | 14 | - | 20 | Ohms | 66 and 100 MHz |
| Rise Time Between 0.4 V and 2.4 V | TR | 0.5 | - | 2.0 | nS | 30 pF Load |
| Fall Time Between 0.4 V and 2.4 V | TF | 0.5 | - | 2.0 | nS | 30 pF Load |
| **VDDP= VDDR =3.3V ±5%, VDDC = 2.5V ±5%,, TA = 0ºC to +70ºC** | | | | | | |

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## Crystal and Reference Oscillator Parameters

| Characteristic | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Frequency | $F_o$ | 12.00 | 14.31818 | 16.00 | MHz | |
| Tolerance | TC | - | - | +/-100 | PPM | Calibration Note 1 |
| | TS | - | - | +/- 100 | PPM | Stability (Ta -10 to +60C) Note 1 |
| | TA | - | - | 5 | PPM | Aging (first year @ 25C) Note 1 |
| Mode | OM | - | - | - | | Parallel Resonant |
| Pin Capacitance | CP | | 5 | | pF | Capacitance of XIN and Xout pins |
| DC Bias Voltage | $V_{BIAS}$ | 0.3Vdd | Vdd/2 | 0.7Vdd | V | |
| Startup time | Ts | - | - | 30 | $\mu$S | |
| Load Capacitance | CL | - | 20 | - | pF | Note 1 |
| Effective Series resonant resistance | R1 | - | - | 40 | Ohms | |
| Power Dissipation | DL | - | - | 0.10 | mW | Note 1 |
| Shunt Capacitance | CO | - | -- | 7 | pF | |
| X1 and X2 Load | CL | | 17 | | pF | Internal crystal loading capacitors on each pin (to ground) |
| For maximum accuracy, the total circuit loading capacitance should be equal to CL. This loading capacitance is the effective capacitance across the crystal pins and includes the device pin capacitance (CP) in parallel with any circuit traces, the clock generator and any onboard discrete load capacitors. <br> Budgeting Calculations <br> Typical trace capacitance, (< half inch) is 4 pF, Load to the crystal is therefore     2.0 pF <br> Clock generator internal pin capacitance of 36 pF, Load to the crystal is therefore    18.0 pF <br> the total parasitic capacitance would therefore be      = 20.0 pF(matching CL) ||||||||

Note 1: It is recommended but not mandatory that a crystal meets these specifications.

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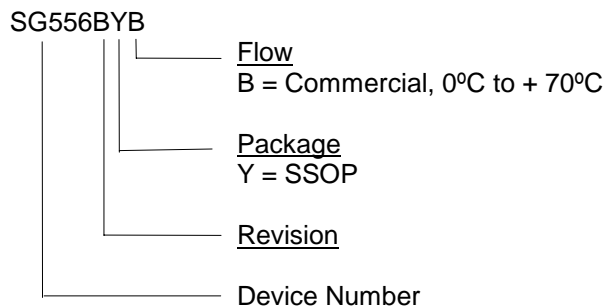## Package Drawing and Dimensions
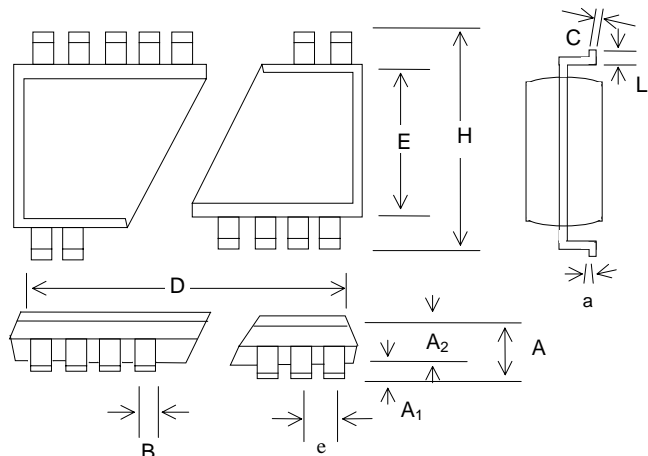


### 28 Pin SSOP Outline Dimensions

| SYMBOL | INCHES | | | MILLIMETERS | | |
|--------|--------|--------|--------|--------|--------|--------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.068 | 0.073 | 0.078 | 1.73 | 1.86 | 1.99 |
| $A_1$ | 0.002 | 0.005 | 0.008 | 0.05 | 0.13 | 0.21 |
| A2 | 0.066 | 0.068 | 0.070 | 1.68 | 1.73 | 1.78 |
| B | 0.010 | 0.012 | 0.015 | 0.25 | 0.30 | 0.38 |
| C | 0.005 | 0.006 | 0.009 | 0.13 | 0.15 | 0.22 |
| D | 0.397 | 0.402 | 0.407 | 10.07 | 10.20 | 10.33 |
| E | 0.205 | 0.209 | 0.212 | 5.20 | 5.30 | 5.38 |
| e | 0.0256 BSC | | | 0.65 BSC | | |
| H | 0.301` | 0.307 | 0.311 | 7.65 | 7.80 | 7.90 |
| a | 0° | 4° | 8° | 0° | 4° | 8° |
| L | 0.022 | 0.030 | 0.037 | 0.55 | 0.75 | 0.95 |

## Ordering Information

| Part Number | Package Type | Production Flow |
|-------------|--------------|-----------------|
| SG556BYB | 28 PIN SSOP | Commercial, 0ºC to +70ºC |

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: Cypress
SG556BYB
Date Code, Lot #

SG556BYB

Flow
B = Commercial, 0ºC to + 70ºC

Package
Y = SSOP

Revision

Device Number

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