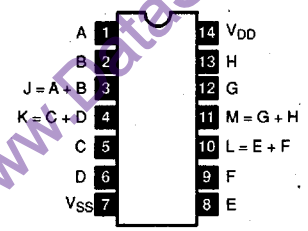
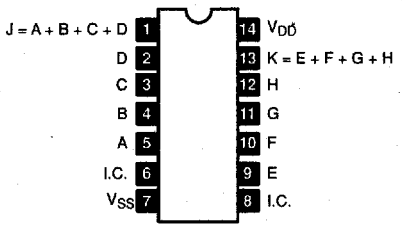
NTE4081B 14–Lead DIP, See Diag. 247
Quad 2–Input AND Gate

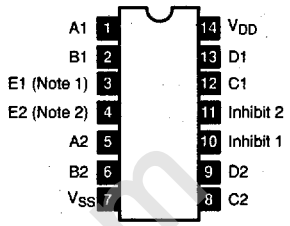


NTE4082B 14–Lead DIP, See Diag. 247
Dual 4–Input AND Gate



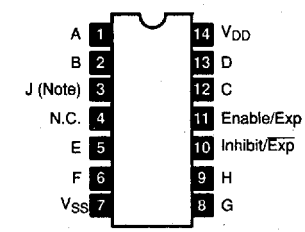
Note: I.C. = Internal Connection. **DO NOT USE.**

NTE4085B 14–Lead DIP, See Diag. 247
Dual 2–Wide, 2–Input AND/OR Invert Gate



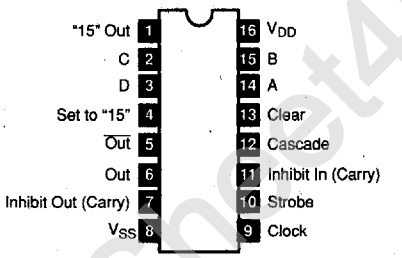
Note 1. E1= $\overline{INH1 + A1B1 + C1D1}$
Note 2. E2 = $\overline{INH2 + A2B2 + C2D2}$

NTE4086B 14–Lead DIP, See Diag. 247
Expandable 4–Wide, 2–Input AND/OR Invert Gate

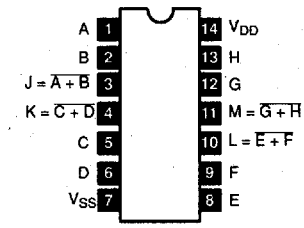


Note: I = INH + $\overline{Enable}$ + AB + CD + EF + GH

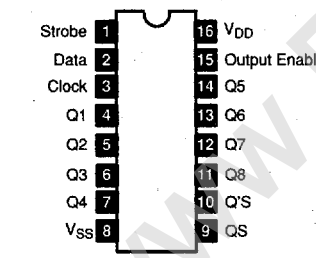
NTE4089B 16–Lead DIP, See Diag. 249
Binary Rate Multiplier



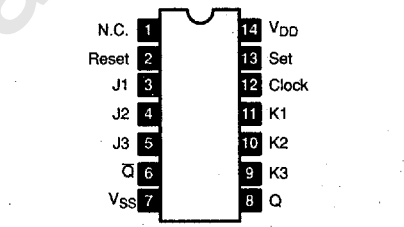
NTE4093B 14–Lead DIP, See Diag. 247
Quad 2–Input NAND Schmitt Trigger



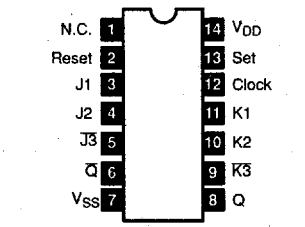
NTE4094B 16–Lead DIP, See Diag. 249
8–Stage Shift & Storage Bus Register



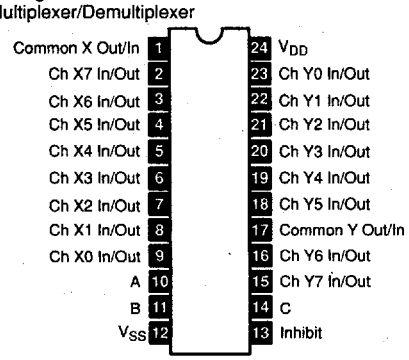
NTE4095B 14–Lead DIP, See Diag. 247
Gated J–K Master/Slave Flip–Flop w/Set–Reset Capability, Non–Inverting J & K Inputs



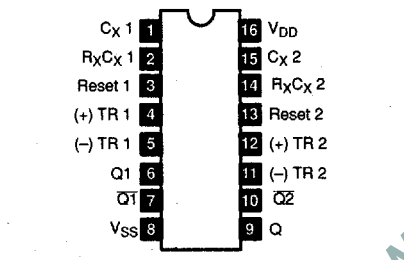
NTE4096B 14–Lead DIP, See Diag. 247
Gated J–K Master/Slave Flip–Flop w/Set–Reset Capability, Inverting & Non–Inverting J & K Inputs



NTE4097B 24–Lead DIP, See Diag. 343
Analog Differential 8–Channel Multiplexer/Demultiplexer

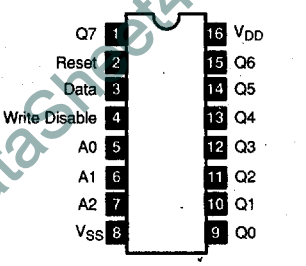


NTE4098B 16–Lead DIP, See Diag. 249
Dual Monostable Multivibrator



Note: Pins 1, 8, and 15 are electrically connected internally

NTE4099B 16–Lead DIP, See Diag. 249
8–Bit Addressable Latch



See Diagrams, beginning on Page 1–293