

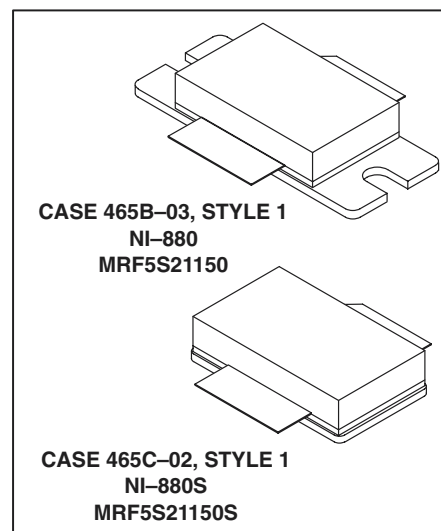
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 1300$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz, Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
 - Output Power — 33 Watts Avg.
 - Power Gain — 12.5 dB
 - Efficiency — 25%
 - IM3 — -37 dBc
 - ACPR — -39 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2140 MHz, 125 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Qualified Up to a Maximum of 32 V_{DD} Operation
- Available in Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

MRF5S21150
MRF5S21150R3
MRF5S21150S
MRF5S21150SR3

2170 MHz, 33 W AVG.,
2 x W-CDMA, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	367 2.1	Watts $\text{W}/^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$
CW Operation	CW	125	Watts

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C , 125 W CW Case Temperature 80°C , 33 W CW	$R_{\theta JC}$	0.47 0.53	$^\circ\text{C}/\text{W}$

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C7 (Minimum)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc)	I _{DSS}	—	—	1	μAdc
Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	—	—	1	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 360 μAdc)	V _{GS(th)}	2.5	—	3.5	Vdc
Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 1300 mAdc)	V _{GS(Q)}	—	3.7	—	Vdc
Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 3.6 Adc)	V _{DS(on)}	—	0.26	0.3	Vdc
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3.6 Adc)	g _{fs}	—	9	—	S

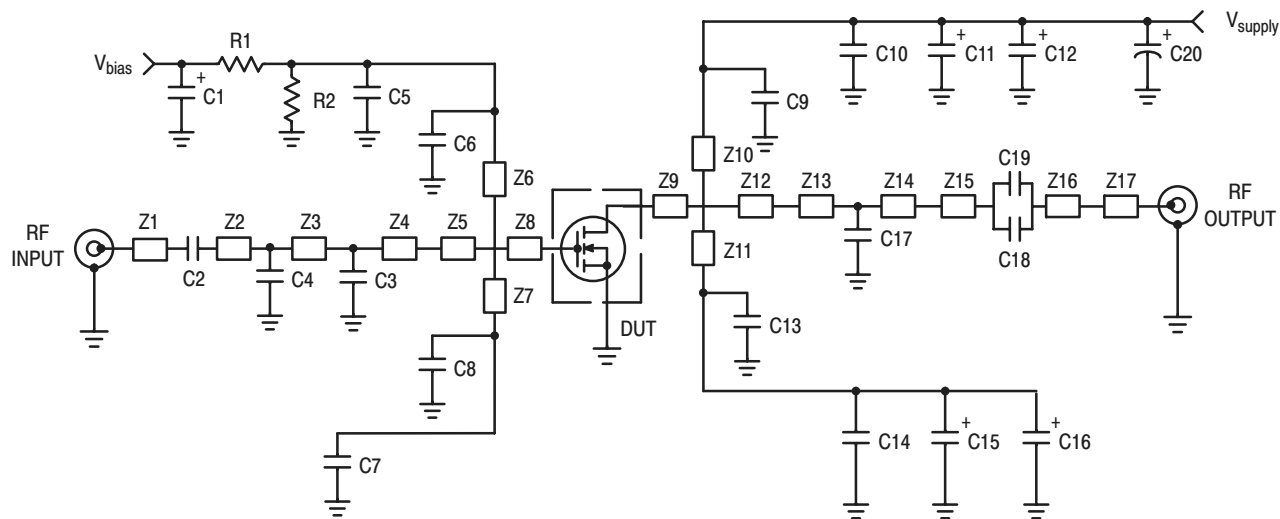
DYNAMIC CHARACTERISTICS (1)

Reverse Transfer Capacitance (V _{DS} = 28 Vdc ± 30 mV(rms)ac @ 1 MHz, V _{GS} = 0 Vdc)	C _{rss}	—	3.2	—	pF
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FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) 2–carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers, ACPR and IM3 measured in 3.84 MHz Bandwidth. Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.

Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	G _{ps}	11	12.5	—	dB
Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	η	23	25	—	%
Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW at f ₁ –10 MHz and f ₂ +10 MHz referenced to carrier channel power.)	IM3	—	–37	–35	dBc
Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz at f ₁ –5 MHz and f ₂ +5 MHz.)	ACPR	—	–39	–37	dBc
Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 33 W Avg., I _{DQ} = 1300 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz)	IRL	—	–12	–9	dB

(1) Part is internally matched both on input and output.



Z1	0.500" x 0.083" Microstrip	Z10, Z11	0.709" x 0.083" Microstrip
Z2	0.505" x 0.083" Microstrip	Z12	0.415" x 1.100" Microstrip
Z3	0.536" x 0.083" Microstrip	Z13	0.874" x 0.083" Microstrip
Z4	0.776" x 0.083" Microstrip	Z14	1.182" x 0.083" Microstrip
Z5	0.119" x 1.024" Microstrip	Z15, Z16	0.070" x 0.220" Microstrip
Z6, Z7	0.749" x 0.083" Microstrip	Z17	0.430" x 0.083" Microstrip
Z8	0.117" x 1.024" Microstrip	PCB	Taconic TLX8, 0.030", $\epsilon_r = 2.55$
Z9	0.117" x 1.100" Microstrip		

Figure 1. MRF5S21150 Test Circuit Schematic

Table 1. MRF5S21150 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1	22 μ F, 35 V Tantalum Capacitor	TAJE226M035R	AVX
C2, C6, C8, C9, C13, C18, C19	6.8 pF 100B Chip Capacitors	100B6R8CW	ATC
C3, C4	1.8 pF 100B Chip Capacitors	100B1R8BW	ATC
C5, C7, C10, C14	220 nF Chip Capacitors (1812)	1812Y224KXA	Vishay–Vitramon
C11, C12, C15, C16	10 μ F, 35 V Tantalum Capacitors	293D1106X9035D	Vishay–Sprague
C17	0.3 pF Chip Capacitor	100B0R3BW	ATC
C20	470 μ F, 63 V Electrolytic Capacitor, Radial	13661471	Philips
R1, R2	10 k Ω , 1/4 W Chip Resistors		

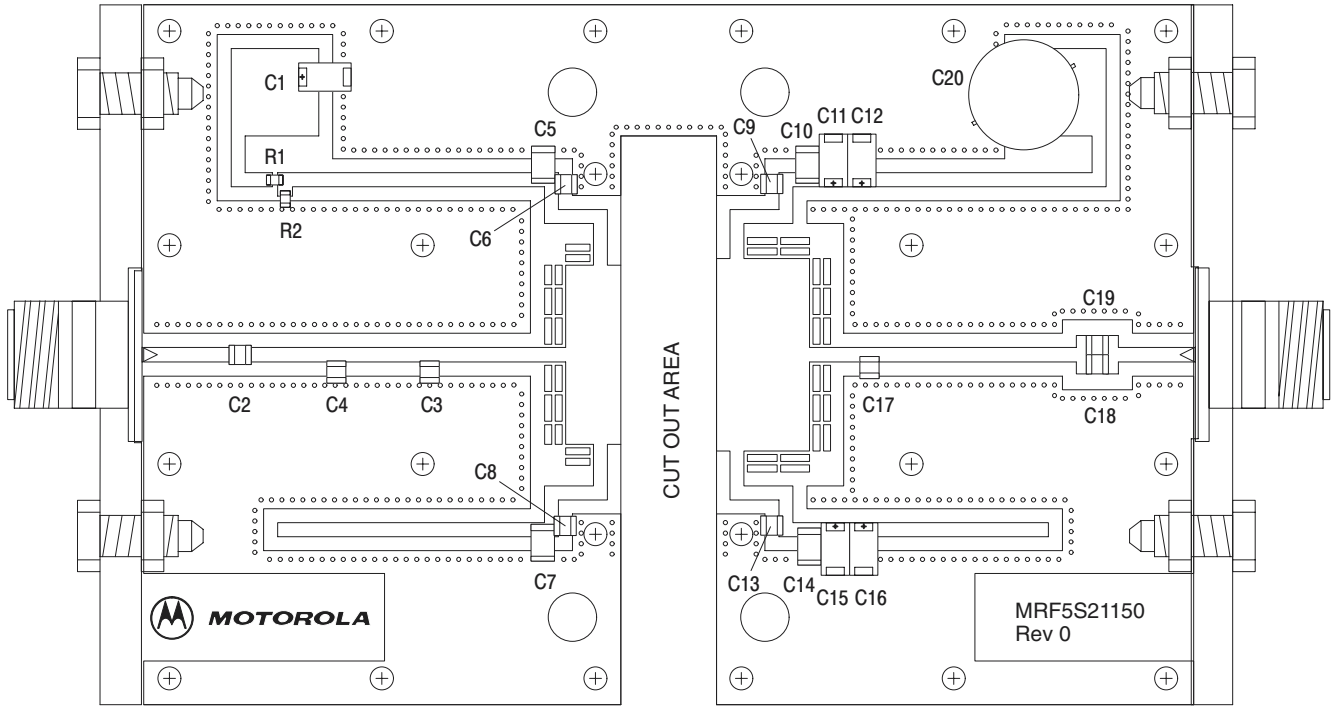


Figure 2. MRF5S21150 Test Circuit Component Layout

TYPICAL CHARACTERISTICS

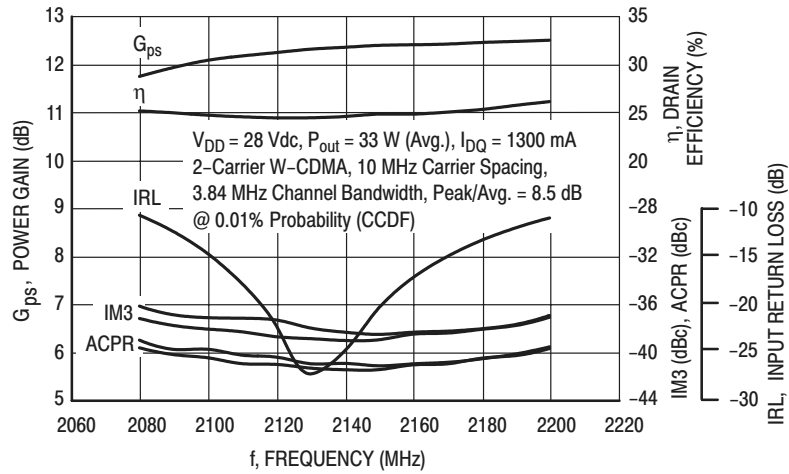


Figure 3. 2-Carrier W-CDMA Broadband Performance

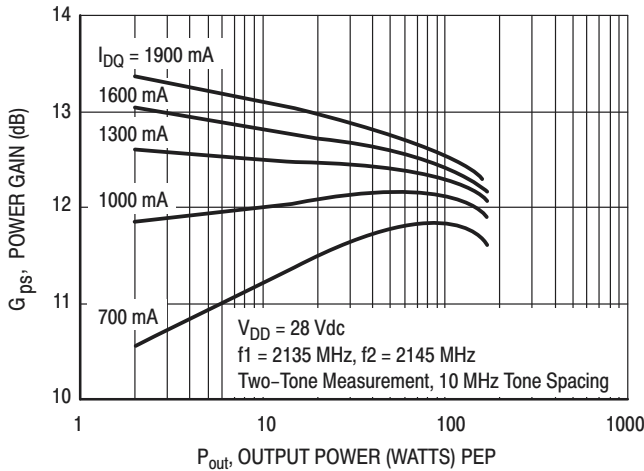


Figure 4. Two-Tone Power Gain versus Output Power

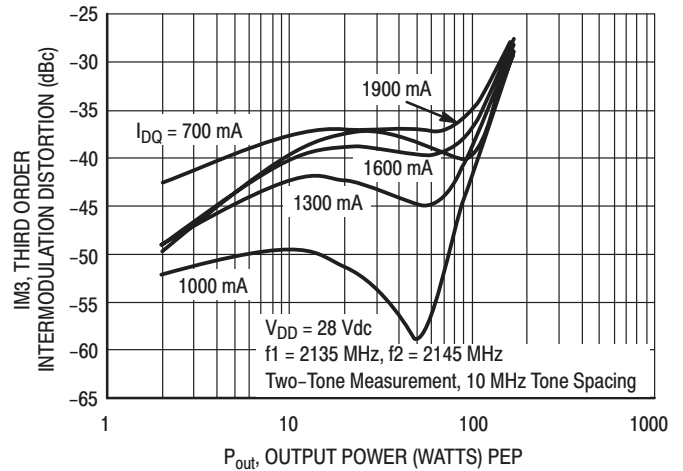


Figure 5. Third Order Intermodulation Distortion versus Output Power

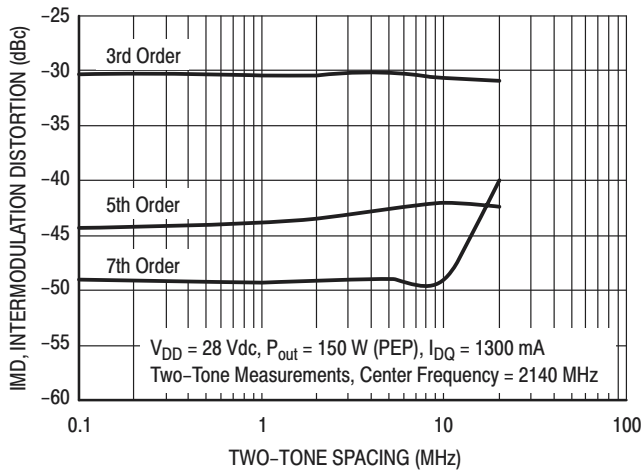


Figure 6. Intermodulation Distortion Products versus Tone Spacing

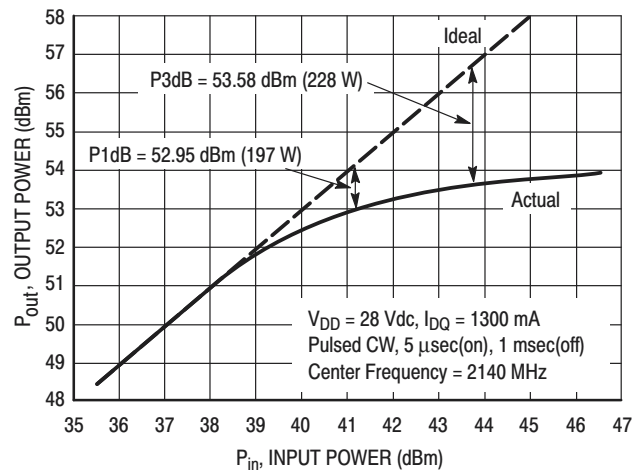


Figure 7. Pulse CW Output Power versus Input Power

TYPICAL CHARACTERISTICS

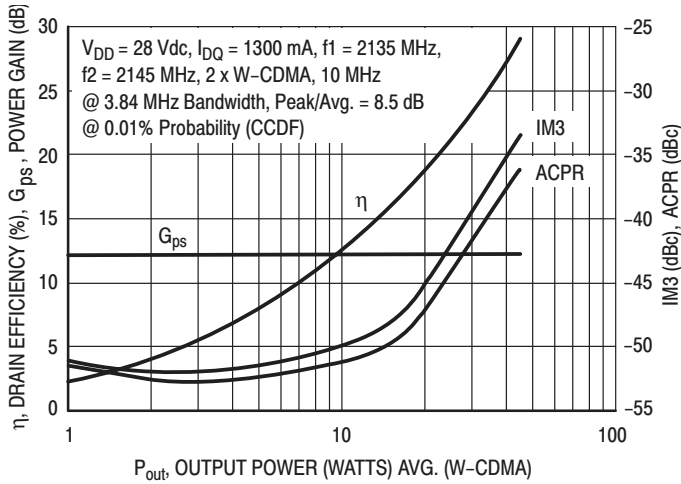


Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

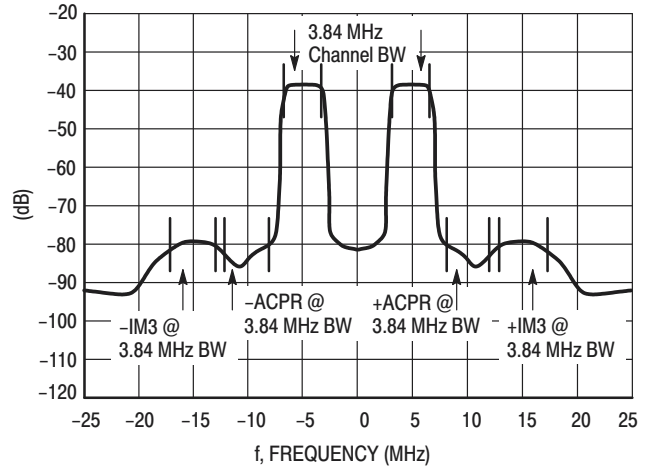


Figure 9. 2-Carrier W-CDMA Spectrum

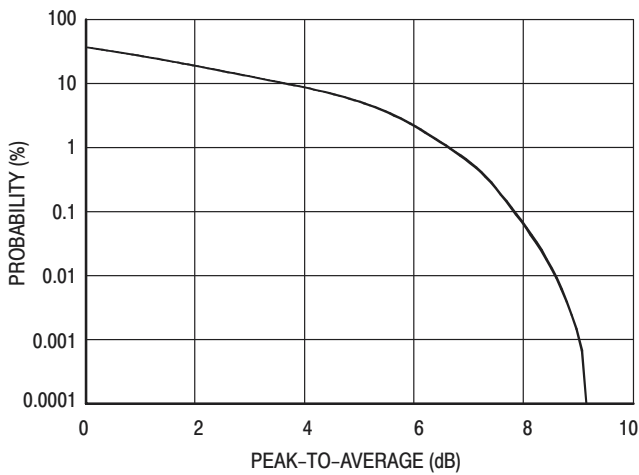
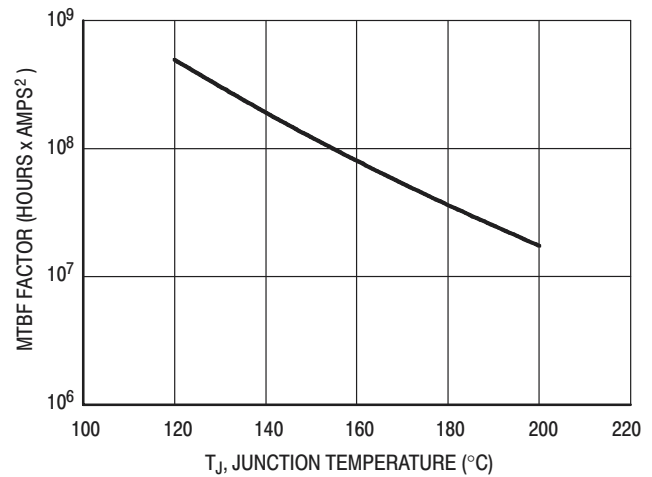
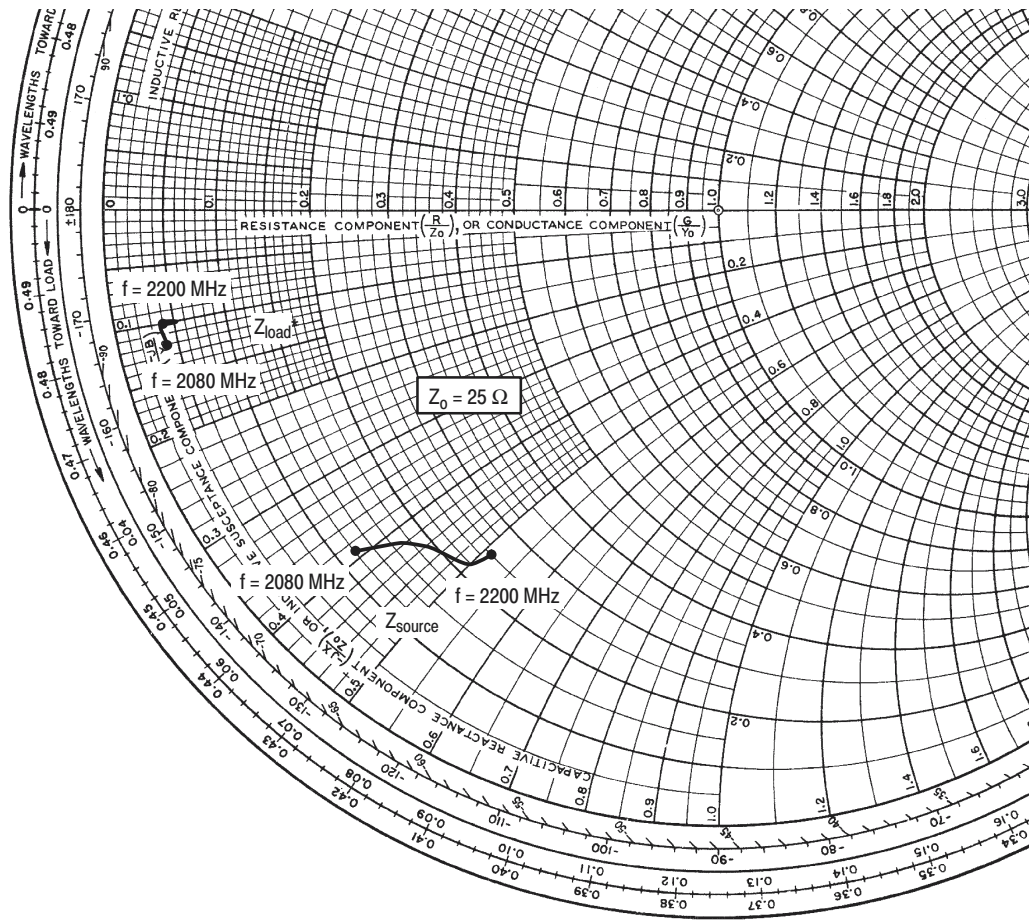


Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal



This above graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 11. MTBF Factor versus Junction Temperature



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1300 \text{ mA}$, $P_{out} = 33 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
2080	$3.05 - j9.66$	$1.02 - j2.94$
2110	$3.97 - j10.31$	$1.09 - j2.51$
2140	$4.70 - j11.03$	$1.16 - j2.46$
2170	$5.45 - j12.41$	$1.16 - j2.58$
2200	$6.18 - j13.04$	$1.02 - j2.55$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

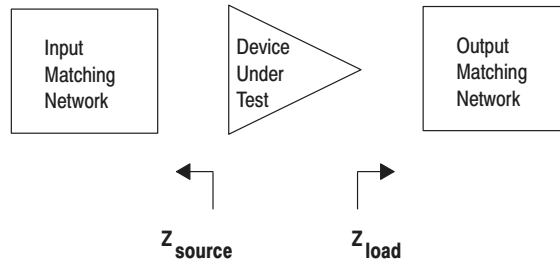


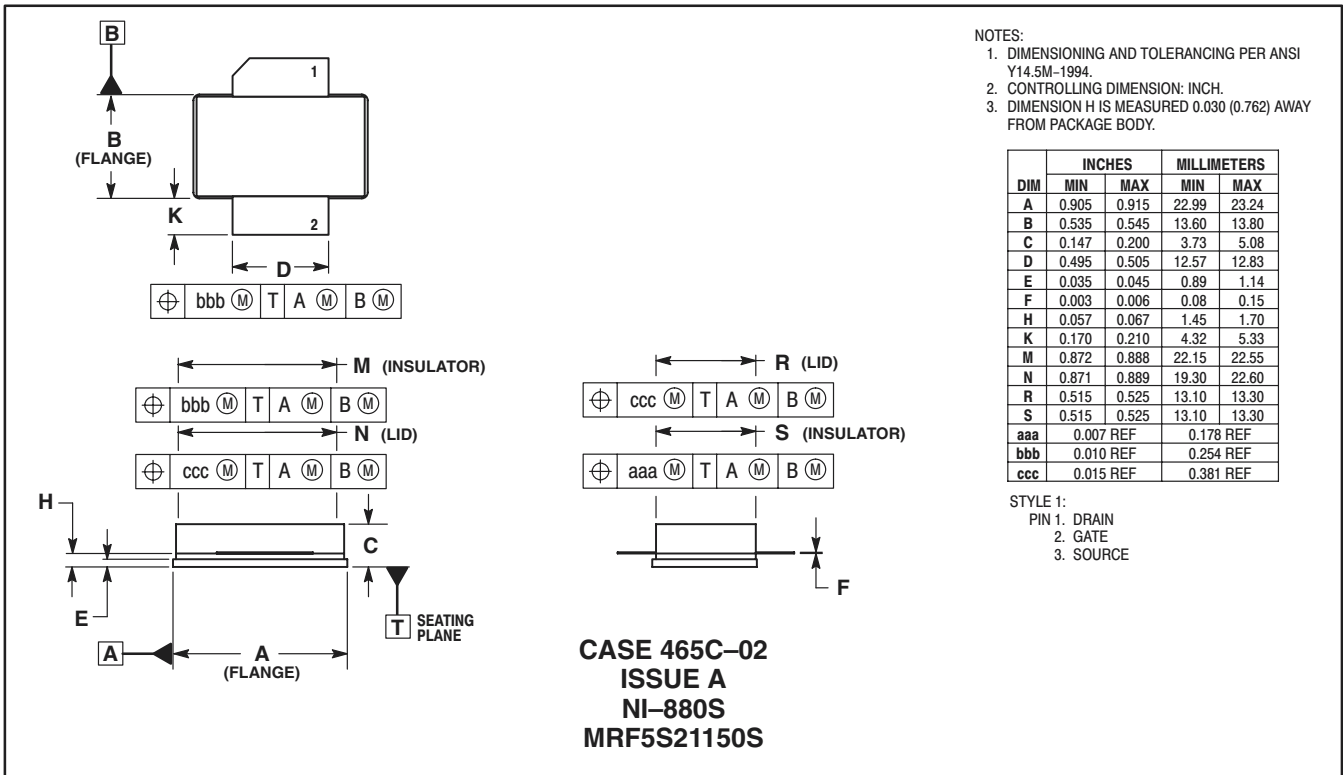
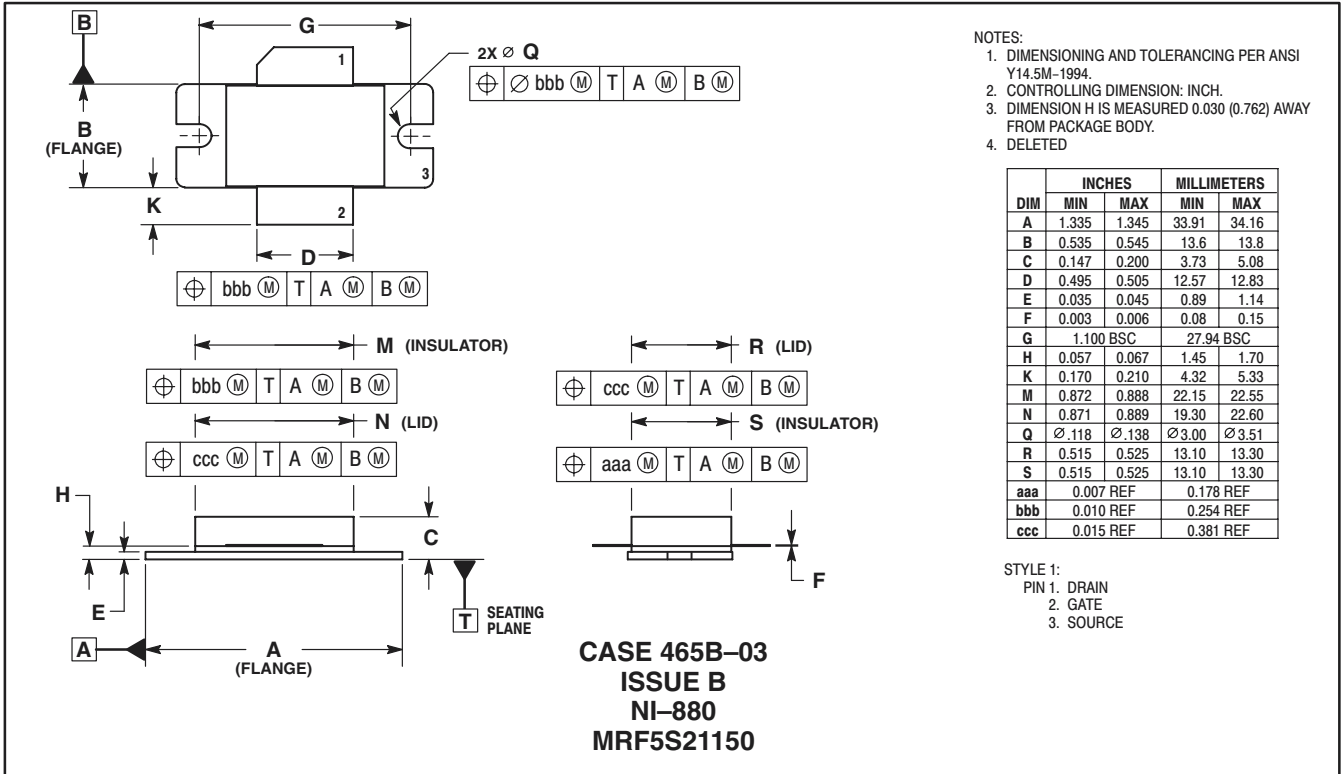
Figure 12. Series Equivalent Input and Output Impedance

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