

# Low-Voltage Quiet CMOS 1-of-8 Decoder/Demultiplexer

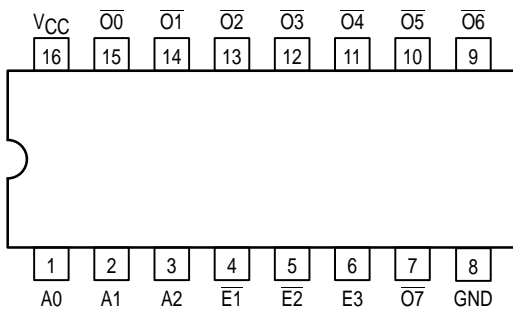
The MC74LVQ138 is a high performance, 1-of-8 decoder/demultiplexer operating from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. The MC74LVQ138 is suitable for memory address decoding and other TTL level bus oriented applications.

The MC74LVQ138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A0, A1, A2) and, when enabled, provides eight mutually exclusive active-LOW outputs ( $\overline{O0}$ – $\overline{O7}$ ). The LVQ138 features three Enable inputs, two active-LOW ( $\overline{E1}$ ,  $\overline{E2}$ ) and one active-HIGH (E3). All outputs will be HIGH unless  $\overline{E1}$  and  $\overline{E2}$  are LOW, and E3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LVQ138 devices and one inverter (See Figure 1). The LVQ138 can be used as an 8-output demultiplexer by using one of the active-LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Current drive capability is 12mA at the outputs.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation – Ideal for Low Power/Low Noise Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Guaranteed Skew Specifications
- Guaranteed Incident Wave Switching into 75Ω
- Low Static Supply Current (10μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V

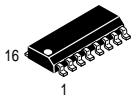
**Pinout: 16-Lead Plastic Package (Top View)**



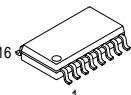
## MC74LVQ138

# LVQ

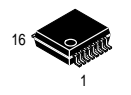
### LOW-VOLTAGE CMOS DECODER/DEMULPLEXER



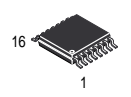
**D SUFFIX**  
PLASTIC SOIC  
CASE 751B-05



**M SUFFIX**  
PLASTIC SOIC EIAJ  
CASE 966-01



**SD SUFFIX**  
PLASTIC SSOP  
CASE 940B-03

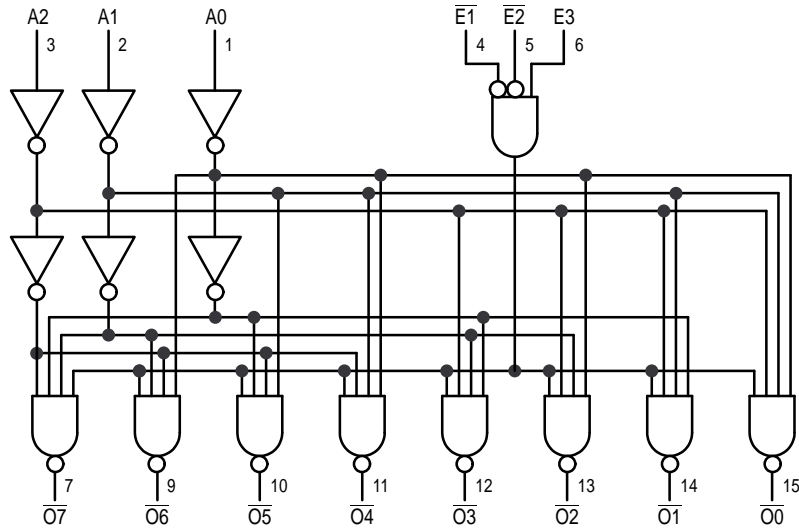


**DT SUFFIX**  
PLASTIC TSSOP  
CASE 948F-01

**PIN NAMES**

Pins	Function
A0–A2	Address Inputs
$\overline{E1}$ – $\overline{E2}$	Enable Inputs
E3	Enable Input
$\overline{O0}$ – $\overline{O7}$	Outputs

LOGIC DIAGRAM



INPUTS						OUTPUTS							
E1	E2	E3	A0	A1	A2	O0	O1	O2	O3	O4	O5	O6	O7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	L	H	L

H = High Voltage Level; L = Low Voltage Level; X = High or Low Voltage Level and Transitions Are Acceptable; For I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

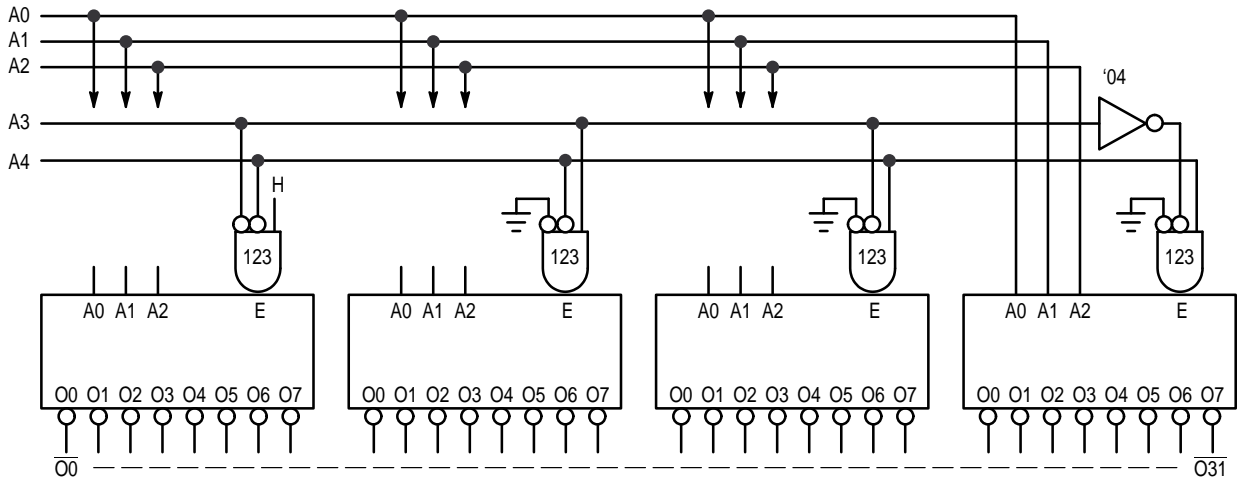


Figure 1. Expansion to 1-of-32 Decoding

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ V <sub>CC</sub> + 0.5V		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Output in HIGH or LOW State	V
I <sub>IK</sub>	DC Input Diode Current	-20	V <sub>I</sub> = -0.5V	mA
		+20	V <sub>I</sub> = V <sub>CC</sub> + 0.5V	mA
I <sub>OK</sub>	DC Output Diode Current	-20	V <sub>O</sub> = -0.5V	mA
		+20	V <sub>I</sub> = V <sub>CC</sub> + 0.5V	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current	±200		mA
I <sub>GND</sub>	DC Ground Current	±200		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	2.0	3.3	3.6	V
V <sub>I</sub>	Input Voltage	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output Voltage	0		V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C
ΔV/Δt	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		125	mV/ns

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 1)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V, V <sub>O</sub> = 0.1V or V <sub>CC</sub> - 0.1V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 1)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V, V <sub>O</sub> = 0.1V or V <sub>CC</sub> - 0.1V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -50μA	V <sub>CC</sub> - 0.1		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -12mA	2.48		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 50μA		0.1	V
		2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 12mA		0.4	
I <sub>I</sub>	Input Leakage Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = V <sub>CC</sub> , GND		±1.0	μA
I <sub>OLD</sub>	Minimum Dynamic Output Current (Note 2)	V <sub>CC</sub> = 3.6V; V <sub>OLD</sub> = 0.8V Max		36	mA
I <sub>OHD</sub>		V <sub>CC</sub> = 3.6V; V <sub>OHD</sub> = 2.0V Min		-25	mA
I <sub>CC</sub>	Quiescent Supply Current	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; V <sub>I</sub> = V <sub>CC</sub> , GND		10	μA

1. These values of V<sub>I</sub> are used to test DC electrical characteristics only. Functional test should use V<sub>IH</sub> ≥ 2.4V, V<sub>IL</sub> ≤ 0.5V.
2. Incident wave switching on transmission lines with impedances as low as 75Ω for commercial temperature range is guaranteed. Maximum test duration is 2ms, one output loaded at a time.

**DYNAMIC SWITCHING CHARACTERISTICS** ( $V_{CC} = 3.3V$ )

Symbol	Characteristic	Condition	$T_A = +25^\circ C$			Unit
			Min	Typ	Max	
VOLP	Dynamic LOW Peak Voltage (Note 1)	$C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V$		0.6	1.0	V
VOLV	Dynamic LOW Valley Voltage (Note 1)	$C_L = 50pF, V_{IH} = 3.3V, V_{IL} = 0V$		-0.5	-1.0	V
V <sub>IHD</sub>	High Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 0V to Threshold, $f=1MHz$		1.5	2.0	V
V <sub>ILD</sub>	Low Level Dynamic Input Voltage (Note 2)	Input–Under–Test Switching 3.3V to Threshold, $f=1MHz$		1.5	0.8	V

- Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW. The remaining output is measured in the LOW state.
- Number of data inputs is defined as “n” switching, “n–1” inputs switching 0V to 3.3V.

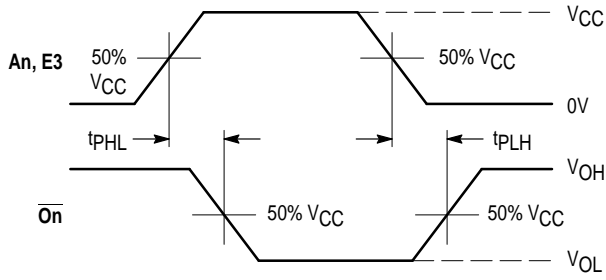
**AC CHARACTERISTICS** ( $t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500\Omega$ )

Symbol	Parameter	Limits									Unit
		$T_A = +25^\circ C$						$T_A = -40^\circ C \text{ to } +85^\circ C$			
		$V_{CC} = 3.0V \text{ to } 3.6V$			$V_{CC} = 2.7V$			$V_{CC} = 3.0V \text{ to } 3.6V$		$V_{CC} = 2.7V$	
		Min	Typ	Max	Min	Typ	Max	Min	Max	Max	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay An to $\overline{O_n}$	1.5 1.5	9.0 9.0	13.0 13.0	1.5 1.5	10.0 14.0	14.5 17.0	1.5 1.5	15.0 15.0	17.0 20.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{E1}, \overline{E2}$ to $\overline{O_n}$	1.5 1.5	12.0 10.0	15.0 13.0	1.5 1.5	13.0 12.0	17.0 15.0	1.5 1.5	16.0 15.0	20.0 17.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E3 to $\overline{O_n}$	1.5 1.5	11.5 10.0	14.5 12.5	1.5 1.5	13.0 11.0	16.5 14.0	1.5 1.5	16.5 14.5	19.0 16.5	ns
t <sub>OSSL</sub> t <sub>OSLH</sub>	Output–to–Output Skew (Note 1)		1.0 1.0	1.5 1.5		1.0 1.0	1.5 1.5		1.5 1.5	1.5 1.5	ns

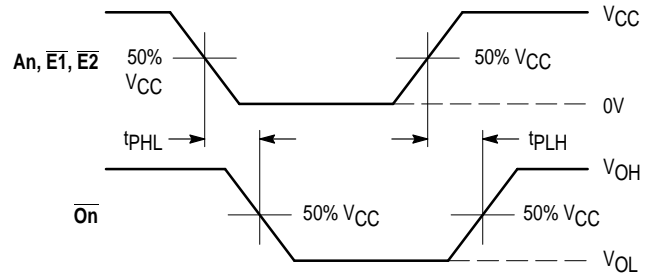
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t<sub>OSSL</sub>) or LOW–to–HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

**CAPACITIVE CHARACTERISTICS**

Symbol	Parameter	Condition	Typical	Unit
C <sub>PD</sub>	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3V, V_I = 0V$ or $V_{CC}$	26	pF
C <sub>IN</sub>	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V$ or $V_{CC}$	4.5	pF

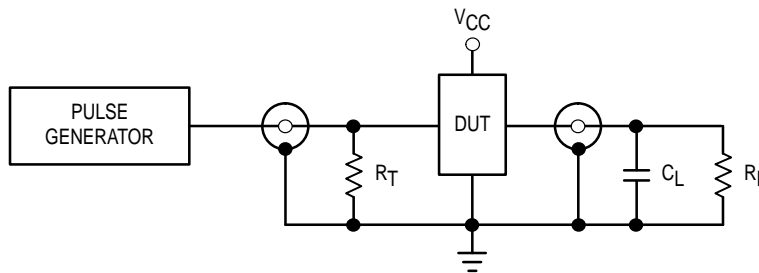


WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS



WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS

Figure 1. AC Waveforms

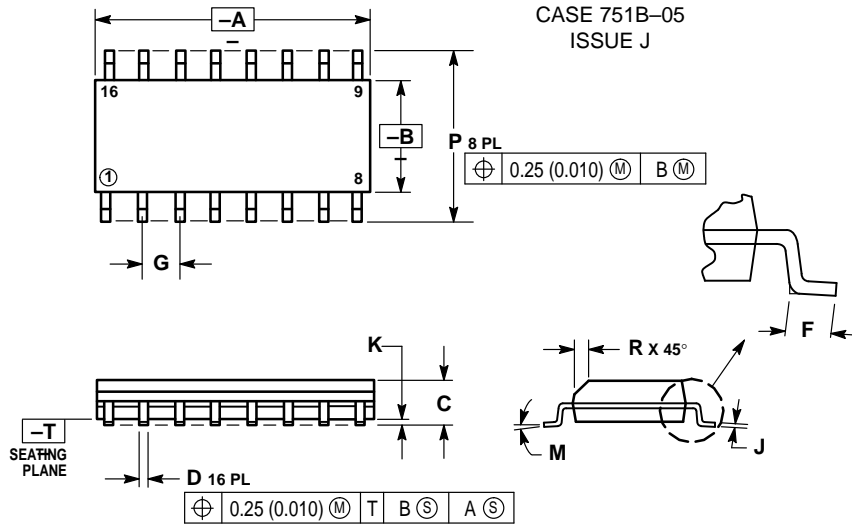


$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

Figure 2. Test Circuit

OUTLINE DIMENSIONS

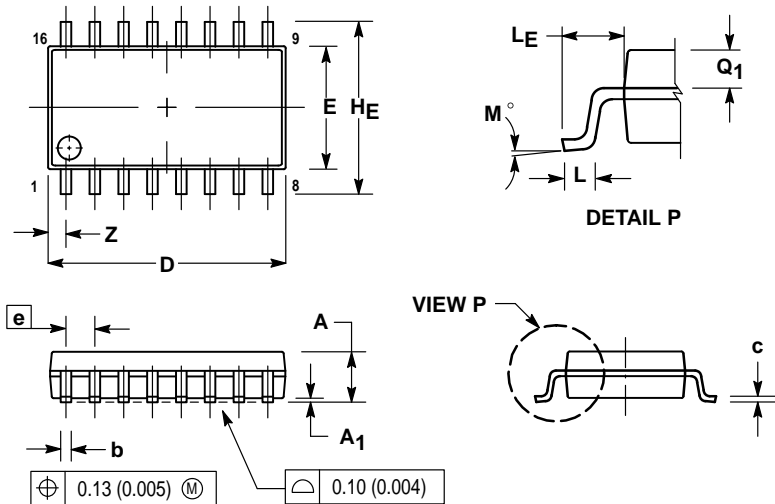
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

M SUFFIX  
PLASTIC SOIC EIAJ PACKAGE  
CASE 966-01  
ISSUE O

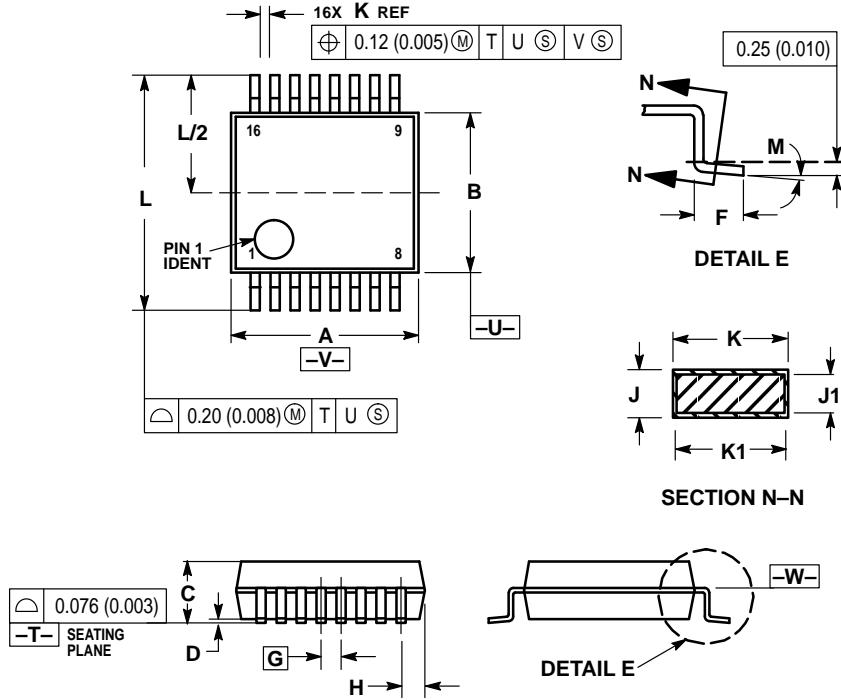


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

OUTLINE DIMENSIONS

SD SUFFIX  
 PLASTIC SSOP PACKAGE  
 CASE 940B-03  
 ISSUE B

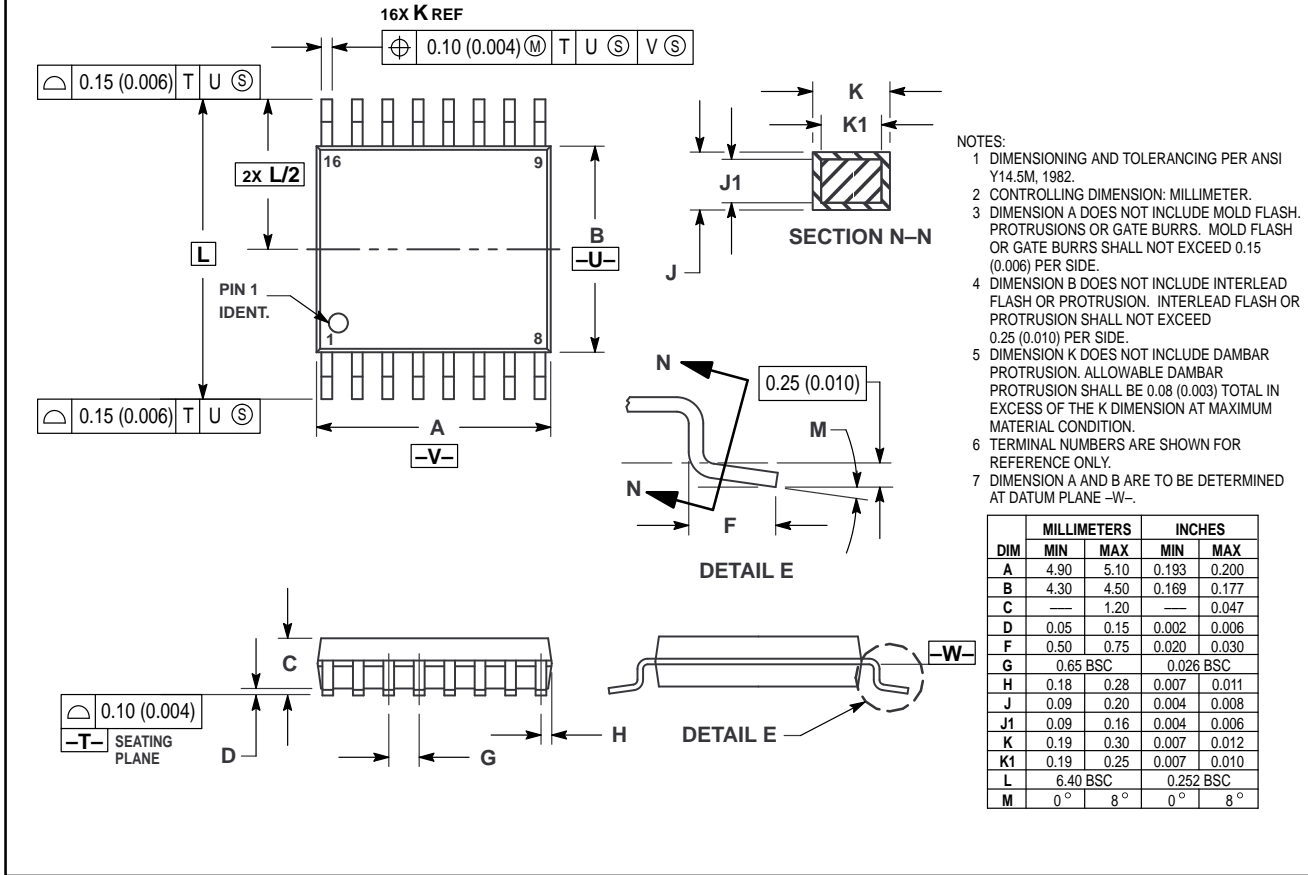


- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: MILLIMETER.
  - DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
  - TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.07	6.33	0.238	0.249
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.63	0.95	0.024	0.037
G	0.65 BSC		0.026 BSC	
H	0.73	0.90	0.028	0.035
J	0.09	0.20	0.003	0.008
J1	0.09	0.16	0.003	0.006
K	0.25	0.38	0.010	0.015
K1	0.25	0.33	0.010	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

OUTLINE DIMENSIONS

DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 948F-01  
 ISSUE O



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