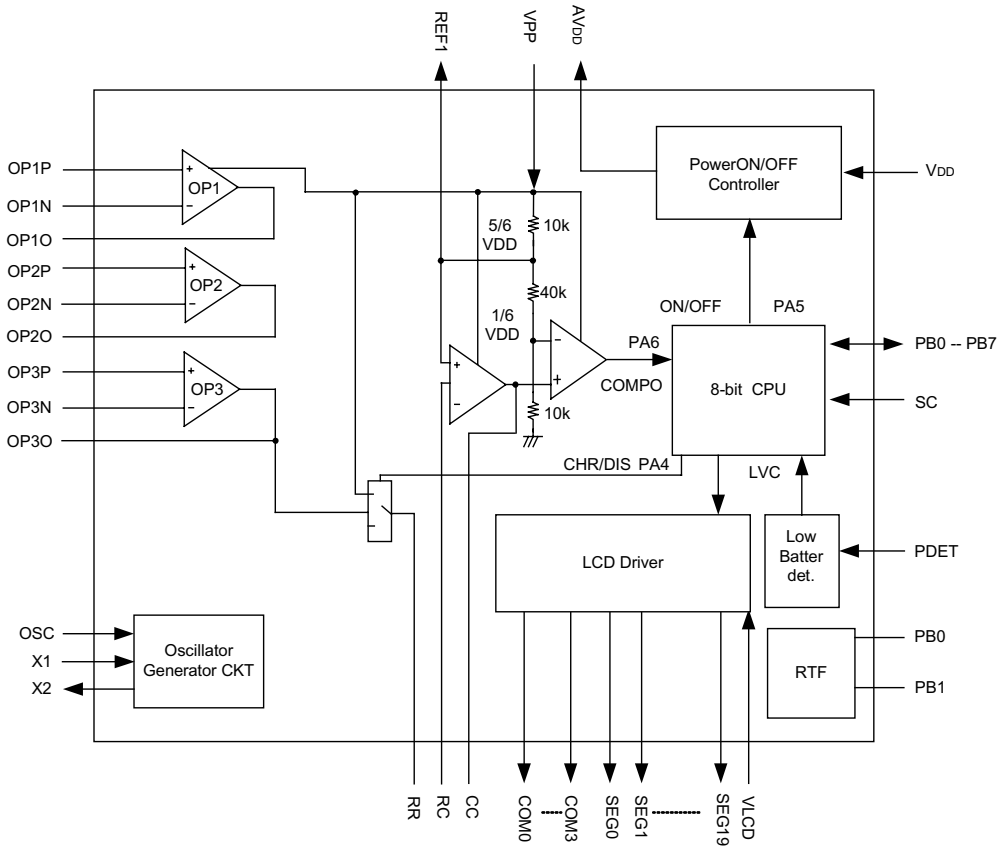
Features

- Operating Voltage: 2.4 V ~ 5.2V
- Stand-by Current=2uA @VDD=3V
- Operating Current = 2mA @ Fsys=2M VDD=3V, ADC off
- Built-in LCD driver: 4 COM * 20 SEG
- LCD duty option: 1/3 duty or 1/4 duty
- LCD bias option: 1/2 bias or 1/3 bias
- R-Bias or C-Bias for LCD by mask option
- RC oscillation for system clock (R external)
- External 32.768 KHz crystal for RTC
- Internal RC 32k for WDT or timer
- Internal with dual slope ADC and 3 OP amplifiers
- Internal with an 8-bit I/O port dedicated for ADC interface (Port A)
- Normal 8-bit I/O port for general I/O (Port B) with interrupt function
- Internal with two16-bit timers (TMR0, TMR1)
- Internal 8-bit WDT (watchdog timer)
- R/F circuit available (PB0, PB1)
- 7K bytes of Program ROM
- 128 bytes of data RAM
- STOP and HALT mode for power saving
- Low battery detect
- AVdd source current 20 mA
- AVdd and Vdd separated

General Description

The JA32050 incorporates an 8-bit MCU, ADC, LCD controller, timers, WDT, 8 programmable general I/Os and R/F circuits inside. It is designed for measuring application, especially suitable for pressure related product such as manometer.

Block Diagram



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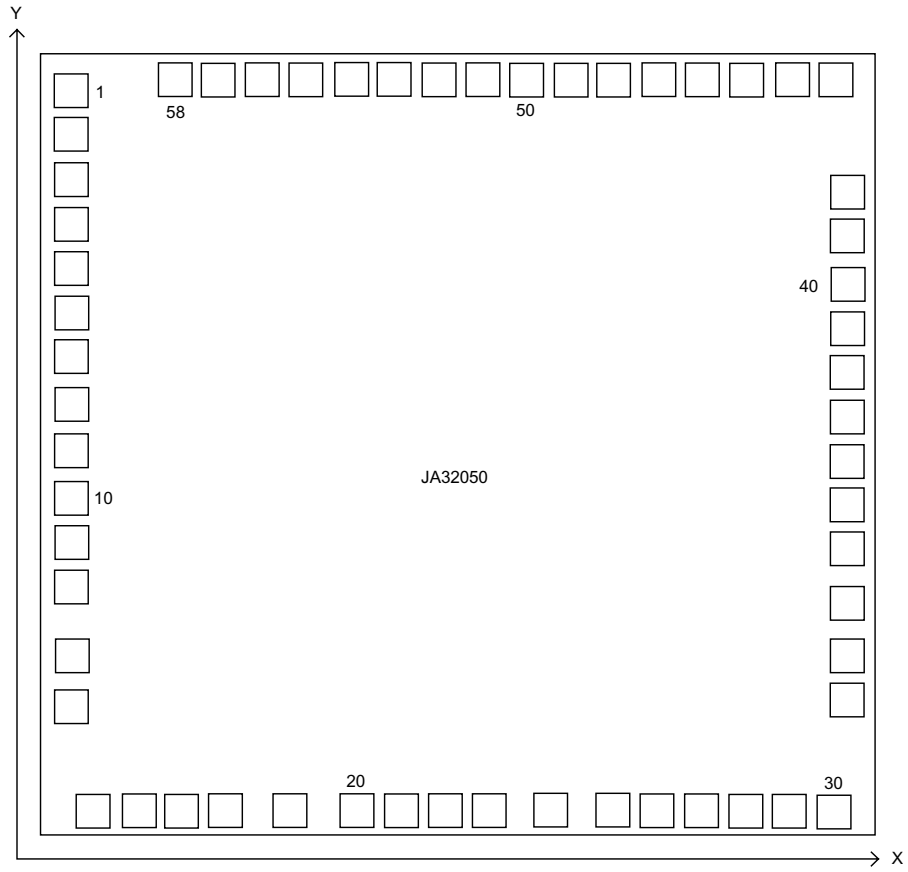
Pad Assignment



Pad Coordinates

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG6	70.00	1866.18	13	OP1O	70.00	455.30
2	SEG5	70.00	1755.98	14	OP2O	70.00	327.40
3	SEG4	70.00	1645.78	15	OP2N	124.30	70.00
4	SEG3	70.00	1535.58	16	OP2P	234.50	70.00
5	SEG2	70.00	1425.38	17	OP3P	344.70	70.00
6	SEG1	70.00	1315.18	18	OP3N	454.90	70.00
7	SEG0	70.00	1204.98	19	OP3O	613.46	70.00
8	VDD	70.00	1085.47	20	REF1	779.94	70.00
9	VCC	70.00	969.06	21	VSS	890.14	70.00
10	VPP	70.00	849.00	22	RR	1000.34	70.00
11	OP1P	70.00	738.80	23	RC	1110.54	70.00
12	OP1N	70.00	628.60	24	CC	1262.95	70.00

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Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
25	PB7	1419.58	70.00	42	COM2	2003.58	1619.08
26	PB6	1529.78	70.00	43	COM1	1974.44	1893.38
27	PB5	1639.98	70.00	44	COM0	1864.24	1893.38
28	PB4	1750.18	70.00	45	VLCD	1754.04	1893.38
29	PB3	1860.38	70.00	46	SEG19	1643.84	1893.38
30	PB2	1970.58	70.00	47	SEG18	1533.64	1893.38
31	PB1	2003.58	344.96	48	SEG17	1423.44	1893.38
32	PB0	2003.58	455.16	49	SEG16	1313.24	1893.38
33	SC	2003.58	588.93	50	SEG15	1203.04	1893.38
34	PDET	2003.58	724.48	51	SEG14	1092.84	1893.38
35	VDD	2003.58	834.68	52	SEG13	982.64	1893.38
36	OSCI	2003.58	944.88	53	SEG12	872.44	1893.38
37	VSS	2003.58	1055.08	54	SEG11	762.24	1893.38
38	RESB	2003.58	1165.28	55	SEG10	652.04	1893.38
39	XT1	2003.58	1275.48	56	SEG9	541.84	1893.38
40	XT2	2003.58	1385.68	57	SEG8	431.64	1893.38
41	COM3	2003.58	1508.88	58	SEG7	321.44	1893.38
Chip Size : 2073.58 x 1963.38(μm)^2							

Pin Descriptions

Pad No	Pad Name	I/O	Description
1	SEG6	O	Segment 6
2	SEG5	O	Segment 5
3	SEG4	O	Segment 4
4	SEG3	O	Segment 3
5	SEG2	O	Segment 2
6	SEG1	O	Segment 1
7	SEG0	O	Segment 0
8	VDD	O	Positive power supply
9	AVDD	O	Analog power supply (ON/Off by PA5)
10	VPP	I	Sensor power supply (SPWR)
11	OP1P	I	OP1 “+” input
12	OP1N	I	OP1 “-” input
13	OP1O	O	OP1 output
14	OP2O	O	OP2 output
15	OP2N	I	OP2 “-” input
16	OP2P	I	OP2 “+” input
17	OP3P	I	OP3 “+” input
18	OP3N	I	OP3 “-” input
19	OP3O	O	OP3 output
20	REF1	O	For reference voltage input
21	VSS	—	Negative power supply or GND
22	RR	I	2nd stage of internal amplifier
23	RC	I	2nd stage of OPA negative input end
24	CC	O	2nd stage of OPA output end
25	PB7	I/O	PB I/O pin 7

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26	PB6	I/O	PB I/O pin 6
27	PB5	I/O	PB I/O pin 5
28	PB4	I/O	PB I/O pin 4
29	PB3	I/O	PB I/O pin 3
30	PB2	I/O	PB I/O pin 2
31	PB1	I/O	PB1: normal I/O pin 1 or RS, RF control pin
32	PB0	I/O	PB0: normal I/O pin 0 or RS, RF control pin
33	SC	I/O	R/F output pin, connected to MCU TMR pin
34	PDET	I	Low battery detect input
35	VDD	O	Positive power supply
36	OSC	—	Oscillator generator I/O pins
37	VSS	—	Negative power supply or GND
38	RESB	I	System reset input, low active
39	X1	I	32.768k Hz crystal input
40	X2	I	32.768k Hz crystal input
41	COM3	O	Common 3 of LCD
42	COM2	O	Common 2 of LCD
43	COM1	O	Common 1 of LCD
44	COM0	O	Common 0 of LCD
45	VLCD	I	LCD panel bias voltage
46	SEG19	O	Segment 19, in C bias mode, this pin will be CAP2
47	SEG18	O	Segment 18, in C bias mode, this pin will be CAP1
48	SEG17	O	Segment 17, in C bias mode, this pin will be V30
49	SEG16	O	Segment 16, in C bias mode, this pin will be V15
50	SEG15	O	Segment 15
51	SEG14	O	Segment 14
52	SEG13	O	Segment 13
53	SEG12	O	Segment 12
54	SEG11	O	Segment 11
55	SEG10	O	Segment 10
56	SEG9	O	Segment 9
57	SEG8	O	Segment 8
58	SEG7	O	Segment 7

Electrical Characteristics

Symbol	Parameter	Test Condition		Min..	Typ.	Max.	Unit
		VDD	Condition				
VDD	Operating Voltage	—	—	2.2	3.0	5.2	V
IDD	Operating Current	3V	No Load, Fsys=2MHz	—	2	3	mA
ISTB1	Standby Current	3V	Fsys OFF, 32K ON	—	3	5	μA
ISTB2	Standby Current	3V	Fsys OFF, 32K OFF	—	1	3	μA
RPH	Pull high resistor	3V	PB0 – PB7	—	100	—	kΩ
IOH1	PB0, PB1 Source Current	3V	VOH1=2.7V	–20	–30	—	mA
IOL1	PB0, PB1 Sink Current	3V	VOL1=0.3V	20	30	—	mA
IOH2	PB2 – PB7 Source Current	3V	VOH1=2.7V	–1	–3	—	mA
IOL2	PB2 – PB7 Sink current	3V	VOL2=0.3V	1	3	—	mA
IOL3	SC sink current	3V	VOL3=0.3V	20	30	—	mA

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IOL4	LCD COM, SEG Sink Current	3V	VOL4=0.3V	80	150	—	μA
IOH3	LCD COM, SEG Source Current	3V	VOH2=2.7V	50	80	—	μA

MCU Function Description

JA32050 contains a 6502 based 8-bit Micro-Controller Unit (MCU) with Program ROM, Special register, user data RAM and two 16-bit Timers inside. This chip also provides multi external interrupt pins (I/O Port B) and Low Voltage Detector (LVD) function.

Memory

- Memory Mapping

Address	Definition
00h	POWERC (R/W)
01h	INTC (R/W)
02h	INTF (R/W)
03h	WDTCLR (W)
04h	WDTC (R/W)
05h	TMR0H (R/W)
06h	TMR0L (R/W)
07h	TMR0C (R/W)
08h	TMR1H (R/W)
09h	TMR1L (R/W)
0Ah	TMR1C (R/W)
0Bh	PA (R/W)
0Ch	PAC (R/W)
0Dh	PAR (R/W)
0Eh	PB (R/W)
0Fh	PBC (R/W)
10h	PBR (R/W)
11h-1Fh	Reserved
21h	CON0
22h	Reserved
23h	LCD0
24h	LCD1
80h ~ FFh	General purpose Data Memory & Stack
200h ~ 213h	LCD data RAM
E400h ~ FFFFh	User Program

- Data RAM
  Total 128 bytes of Data RAM (including the stack) are available from $80h to $FFh.
- Program ROM
  Total 7K bytes of user ROM located from $E400h to $FFFFh are available.
- Reset & Interrupt Vector
  The reset vector is located at $FFFCh, and interrupt vector followed.
- Stack Pointer
  The stack pointer is set from $FFh after power on.

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Power Configuration

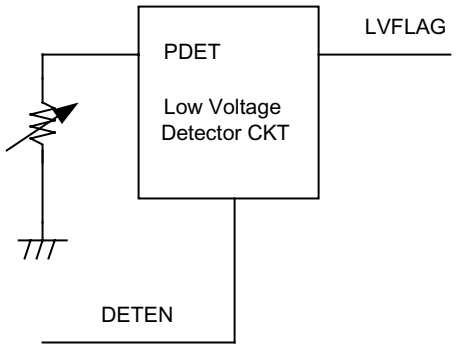
POWERC

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POWERC	00h	LVFLAG	DETEN	—	STOP	—	—	—	HALT

The system provides the HALT mode and the STOP mode for power saving:

- HALT mode
  Writing "1" to the HALT bit cause system enter HALT mode. In HALT mode, the system clock stop running but the internal RC clock (32K) continuously keeps free running. The timer overflow, WDT overflow, external interrupt (INTB) or PA,PB change state can wakeup the system to leave the HALT mode. The HALT bit will be cleared to "0" automatically when system is awakened (STOP bit unchanged).
- STOP mode
  Writing " 1" to the STOP bit causes system enter STOP mode. In STOP mode, both the system clock and internal RC clock stop running. External interrupt (INTB) or PA,PB change state can wakeup the system. The HALT bit and the STOP bit will be cleared to "0" automatically when system is awakened.
- Low voltage
  Writing " 1" to DETEN bit enable the low battery detector circuit of the system. If the low battery situation is detected, the LVFLAG bit will be set to "1" by detector circuit. After writing the DETEN bit, the user must insert 2 NOP instructions in the program before program reading the LVFLAG data.

External resistor shown below adjusts the low voltage level:



The table below is a reference for low voltage setting. If user set low voltage level at 2.15V then 40K ohm resistor shall be used. When Vdd drops to 2.15V the LVFLAG will become "1" indicating the low battery event.

Resistor	40 K	50 K	54 K	60 K	70 K
Vdd	2.15V	2.45V	2.55V	2.65V	2.85V
PDET	0.699V	0.899V	0.97V	1.09V	1.27V
LVFLAG	1	1	1	1	1

Reset and Wakeup

The system will be reset by the following conditions:

- Power on
- Reset pin activated (Low)
- Illegal address generation
- WDT overflow
- VDD voltage lower than 1.8V

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The system will be awakened from STOP mode or HALT mode by the following conditions:

- Timer/WDT overflow
- Level changes on PB input pins

The above situations will make system start running. The starting address depends on the INTF register setting. If the global interrupt bit (INTE) is cleared and the corresponding interrupt bit is set, no wakeup interrupt will be generated and program start running from next instruction in STOP mode or HALT mode. If the global interrupt bit (INTE) is set, the system will execute the corresponding interrupt service routine first then back to execute the next instruction in STOP mode or HALT mode.

Interrupt

In JA32050, the INTC register and the INTF register handle the interrupt operation. Setting or clearing the INTC (interrupt control register) bits will enable or disable the interrupt function. The INTF (interrupt flag) shows the current interrupt status.

The system will be interrupted by the following conditions:

- Timer/WDT overflow
- Level changes on PB input pins

Interrupt control register (INTC) definition is shown below:

INTC (R/W): 01h

Register	Bit No.	Label	Function
INTC	0	INTE	Global interrupt enable bit (1= Enabled; 0 = Disabled)
	1	Reserved	Must be set to “0”
	2	TMR0	TMR0 interrupt Enable bit (1= Enabled; 0 = Disabled)
	3	TMR1	TMR1 interrupt Enable bit (1= Enabled; 0 = Disabled)
	4	PAI	Port A change state interrupt Enable bit (1= Enabled; 0 = Disabled)
	5	PBI	Port B change state interrupt Enable bit (1= Enabled; 0 = Disabled)
	6		Reserved
	7		Reserved

Interrupt Flag (INTF) definition is shown below:

INTF (R/W): 02h

Register	Bit No.	Label	Function
INTF	0	INTF	External INT interrupt flag bit (1= Active; 0 = Inactive)
	1	TMR0F	TMR0 timer interrupt flag bit (1= Active; 0 = Inactive)
	2	TMR1F	TMR1 timer interrupt flag bit (1= Active; 0 = Inactive)
	3		Reserved
	4	PAF	Port A change state interrupt flag bit (1= Active; 0 = Inactive)
	5	PBF	Port B change state interrupt flag bit (1= Active; 0 = Inactive)
	6		Reserved
	7		Reserved

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Timers and WDT

The JA32050 contains two16-bit timers (TMR0, TMR1) and one watchdog timer (WDT). The registers related to timers are TMR (timer content) and TMRC (timer control).

- TMR0 (05h,06h) & TMR0C (07h)
  The TMR0 is a 16-bit count-up counter. The clock source may come from system clock (Fsys/4), internal RC clock, external pulse input (SC) or external 32k crystal. The default value of the control register TMR0C is 00. The definition of TMR0C is listed as following:

Labels	Bits	Function
TON0 (TMR0)	0	Timer0 enable/disable definition bit 0 = Disable; 1 = Enable
TS2, TS1, TS0	3 - 1	Timer clock rate selection bits (prescale)
	4	Reserved
TMR/WDT	5	To assign pre-scale counter to Timer0 or WDT 0: Timer 1: WDT
TM1, TM0	7, 6	To define the operation mode 00= Timer mode (system clock/4) 01= Timer mode (internal RC clock) 10= Event count mode from external SC pin 11= Timer mode (32.768k Hz crystal)

Both TMR0 and WDT share with an 8-bit prescaler. If the prescaler is assigned to TMR0, the WDT clock will be 1:1 to the clock source (no prescale function), vice versa. The ratio table is shown below:

TS2	TS1	TS0	TMR Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

- TMR1 (08h, 09h) & TMR1C (0Ah)
  The TMR01is a 16-bit count-up counter. The clock source may come from system clock, internal RC clock, external pulse input or external 32k crystal. The default value of the control register TMR1C is 00. The definition of TMR0C is listed as following:

Labels	Bits	Function
TON1	0	Timer1 enable/disable definition bit 0 = Disable; 1 = Enable
TS2, TS1, TS0	3 - 1	Timer clock source selection bits
—	4	Reserved
TMROUT	5	This bit has to be set to “0”; SC is configured as input pin.
TM1, TM0	7, 6	To define the operation mode 00= Timer mode (system clock/4) 01= Timer mode (internal RC clock) 10= Event count mode from External SC pin 11= Timer mode (32.768k crystal)

There is an 8-bit prescaler dedicated to TMR1. The ratio table is shown below:

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TS2	TS1	TS0	TMR1 Clock Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

- Watchdog Timer
  The clock source for watchdog timer (WDT) can be either internal RC (32kHz) or system clock/4; decided by Bit 4 of WDTC register. When WDT is enabled, user shall reset (writing "1") Bit 0 of WDTCLR register within a specific time to prevent WDT overflow.

WDTCLR (W): 03h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	—	—	—	—	—	CLRWDT

WDTC (R/W): 04h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
—	—	—	WDTCLK	—	—	—	WDTEN

Bit 4 (WDTCLK): Select the WDT clock source
0=system clock/4 (Default) , 1= Internal RC clock
Bit0 (WDTEN): To enable/disable the WDT, 0= Disable (Default), 1= Enable

I/O Configuration

The I/O port A (PA) is dedicated to ADC circuit so that user cannot use PA for other use. Port B (PB) can be used as normal input and output operations. For input operation, PB is non-latched , for output operation, all the data are latched and remain unchanged till the output latch is re-written.
Each I/O port has its own control register (PAC, PBC) to control the input/output configuration.

- PA Configuration
  PA control register specifies the characteristic of PA. Please refer to the table below:

Label	Address	Function	R/W	Default
PA	0Bh	PA data input/output	R/W	FF
PAC	0Ch	PA direction control, 1=input 0=output	R/W	FF
PAR	0Dh	PA pull-high resistor option, 1=With, 0=Without	R/W	FF

In JA32050, PA is dedicated to ADC circuit, PA5 for ON/OFF control, PA6 for COMPO, PA4 for CHAR/DIS (charge/discharge) control, others PA pins cannot be used. Please see the block diagram on first page for reference.

- PB Configuration
  For port B, they can be configured as follows:

Label	Address	Function	R/W	Default
PB	0Eh	PB data input/output	R/W	FF
PBC	0Fh	PB direction control, 1=input 0=output	R/W	FF
PBR	10h	PB pull-high resistor option, 1=With, 0=Without	R/W	FF

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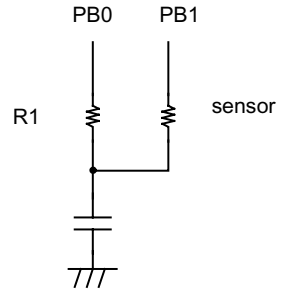
R/F Function Descriptions

PB0, PB1 of port B can be configured (mask option) to perform either R/F function or normal I/O function. In R/F application, user put reference resistor (R1) to PB0, sensor to PB1 (interchangeable). One capacitor also used to from the RC oscillation loop. Please see the following figure for reference:



To active R1, MCU output high signal to PB0 and output low signal to PB1at the same time. Signal can be generated on the SC pin. Inside the JA32050, the signal on SC pin can be routed to the clock source of timer by programming. The R/F circuit will be activated only when timer in event count mode (“10” for TM1, TM0).

LCD Function Descriptions

- LCD Clock
  The clock source for LCD can be internal RC (32kHz), external 32k crystal or system clock; decided by Bit 5, Bit 4 of CON0. The Bit 3 of CON0 controls the LCD on/off, “1” for LCD on, “0” for LCD off.

CON0 (R/W): 21h

B7	B6	B5	B4	B3	B2	B1	B0
—	—	OSC1	OSC0	LCD	—	—	—

OSC1, OSC2: 00 internal RC 32k
01 internal RC 32k
10 external 32k
11 system clock

Note: The STOP mode and the HALT mode will affect the LCD display. In STOP mode, the LCD cannot show any message because all clock are disabled. In HALT mode, message can be seen on the LCD if the clock source is internal RC or external RC.

- LCD Common & Segment
  If user chooses R bias for the LCD, the segment will be SEG 0 to SEG 19. If user chooses C bias for the LCD, the segment will be SEG 0 to SEG 15.
  The user can configure LCD controller to 3 COM or 4 COM; decided by Bit 6, Bit 5, and Bit 4 of LCD0. The Bit 7 of LCD0 controls frame frequency of LCD, “1” for 170 Hz on, “0” for 85 Hz. Please see the table below:

  LCD0 (R/W): 23h

B7	B6	B5	B4	B3	B2	B1	B0
Frame	C2	C1	C0	—	—	—	—

  Frame: 0 - 85 Hz
  1 - 170 Hz
  C2, C1, C0: (1, 0, 0): 3 COM, (0, 1, 1): 4 COM

- LCD Bias
  The user can configure LCD controller to 1/2 bias or 1/3 bias; decided by Bit 2, Bit 1, and Bit 0 of LCD1.

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LCD1 (R/W): 24h

B7	B6	B5	B4	B3	B2	B1	B0
—	—	—	—	—	B2	B1	B0

B2, B1, B0: (1, 0, 0): 1/2 bias, (0, 1, 1): 1/3 bias.

- LCD Data RAM

The RAM is located from 200h to 213h. Please refer to the table below, "*" means "don't care".

RAM Address	Segment number	Content
200h	Seg0	*,*,*,*,COM3,COM2,COM1,COM0
201h	Seg1	*,*,*,*,COM3,COM2,COM1,COM0
202h	Seg2	*,*,*,*,COM3,COM2,COM1,COM0
203h	Seg3	*,*,*,*,COM3,COM2,COM1,COM0
204h	Seg4	*,*,*,*,COM3,COM2,COM1,COM0
205h	Seg5	*,*,*,*,COM3,COM2,COM1,COM0
206h	Seg6	*,*,*,*,COM3,COM2,COM1,COM0
207h	Seg7	*,*,*,*,COM3,COM2,COM1,COM0
208h	Seg8	*,*,*,*,COM3,COM2,COM1,COM0
209h	Seg9	*,*,*,*,COM3,COM2,COM1,COM0
20Ah	Seg10	*,*,*,*,COM3,COM2,COM1,COM0
20Bh	Seg11	*,*,*,*,COM3,COM2,COM1,COM0
20Ch	Seg12	*,*,*,*,COM3,COM2,COM1,COM0
20Dh	Seg13	*,*,*,*,COM3,COM2,COM1,COM0
20Eh	Seg14	*,*,*,*,COM3,COM2,COM1,COM0
20Fh	Seg15	*,*,*,*,COM3,COM2,COM1,COM0
210h	Seg16	*,*,*,*,COM3,COM2,COM1,COM0
211h	Seg17	*,*,*,*,COM3,COM2,COM1,COM0
212h	Seg18	*,*,*,*,COM3,COM2,COM1,COM0
213h	Seg19	*,*,*,*,COM3,COM2,COM1,COM0

LCD R bias / C bias

LCD can be configured as R bias or C bias. In R bias, Seg0-Seg19 all can be used. In C bias, only Seg0-Seg15 can be used.

The circuit for LCD interface will be little different in different Vdd and LCD bias when using capacitor for LCD biasing (C bias). Please see the table below:

Vdd = 3 V

	Vlcd	V30	V15	CAP1, CAP2
1/2 bias	Connected to Vdd	Connected to Vdd or open	Connected to Vss through a 104 cap	CAP1 connected to CAP2 through a 104 cap
1/3 bias	Connected to Vss through a 104 cap	Connected to Vdd	Connected to Vss through a 104 cap	CAP1 connected to CAP2 through a 104 cap

Vdd = 4.5 V

	Vlcd	V30	V15	CAP1, CAP2
1/2 bias	Connected to Vdd	Connected to Vdd or open	Connected to Vss through a 104 cap	CAP1 connected to CAP2 through a 104

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				cap
1/3 bias	Connected to Vdd	Connected to Vdd through a 104 cap	Connected to Vss through a 104 cap	CAP1 connected to CAP2 through a 104 cap

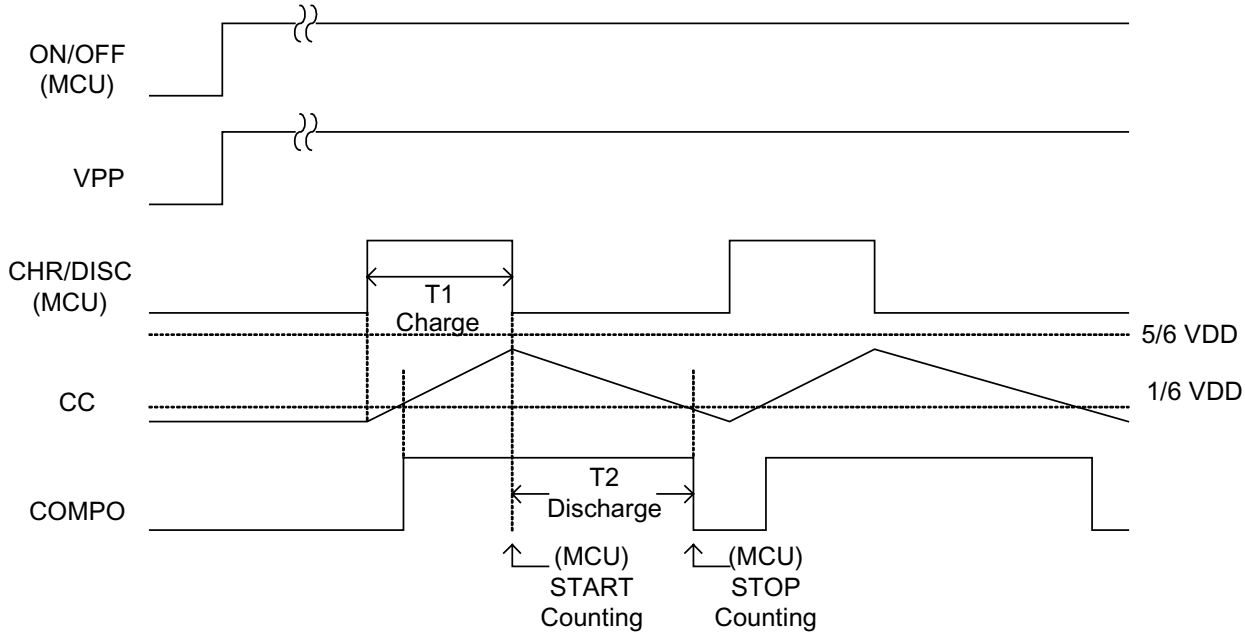
In R bias application, V30, V15, CAP1, CAP2 are normal segment signals.

ADC Function Description

- ADC General

The JA32050 offers very high accuracy A/D conversion by using Dual Slope integration. It incorporates operational amplifiers, comparators, power on/off control circuit and charge/discharge control circuit inside to achieve high performance for application. A voltage follower was used as buffer for sensor signal input. Because of the buffer's great isolating characteristic, the signal from sensor will be precisely duplicated and sent out at output pin without any distortion.
An operational amplifier was designed for user to properly amplify the sensor signal from buffer. Inside the chip, a current accurately proportional to the amplified signal level will be generated to charge an external RC network for a fixed time interval. After being charged for this interval, the capacitor is discharged by a constant current until the voltage reaches 1/6 VDD. This discharging time is proportional to the input signal level and is used by external controller to enable a counter; the final count is proportional to the input level and can be converted to digital output. Because the charge cycle and discharge cycle go through the same RC network, using a high quality capacitor is recommended.

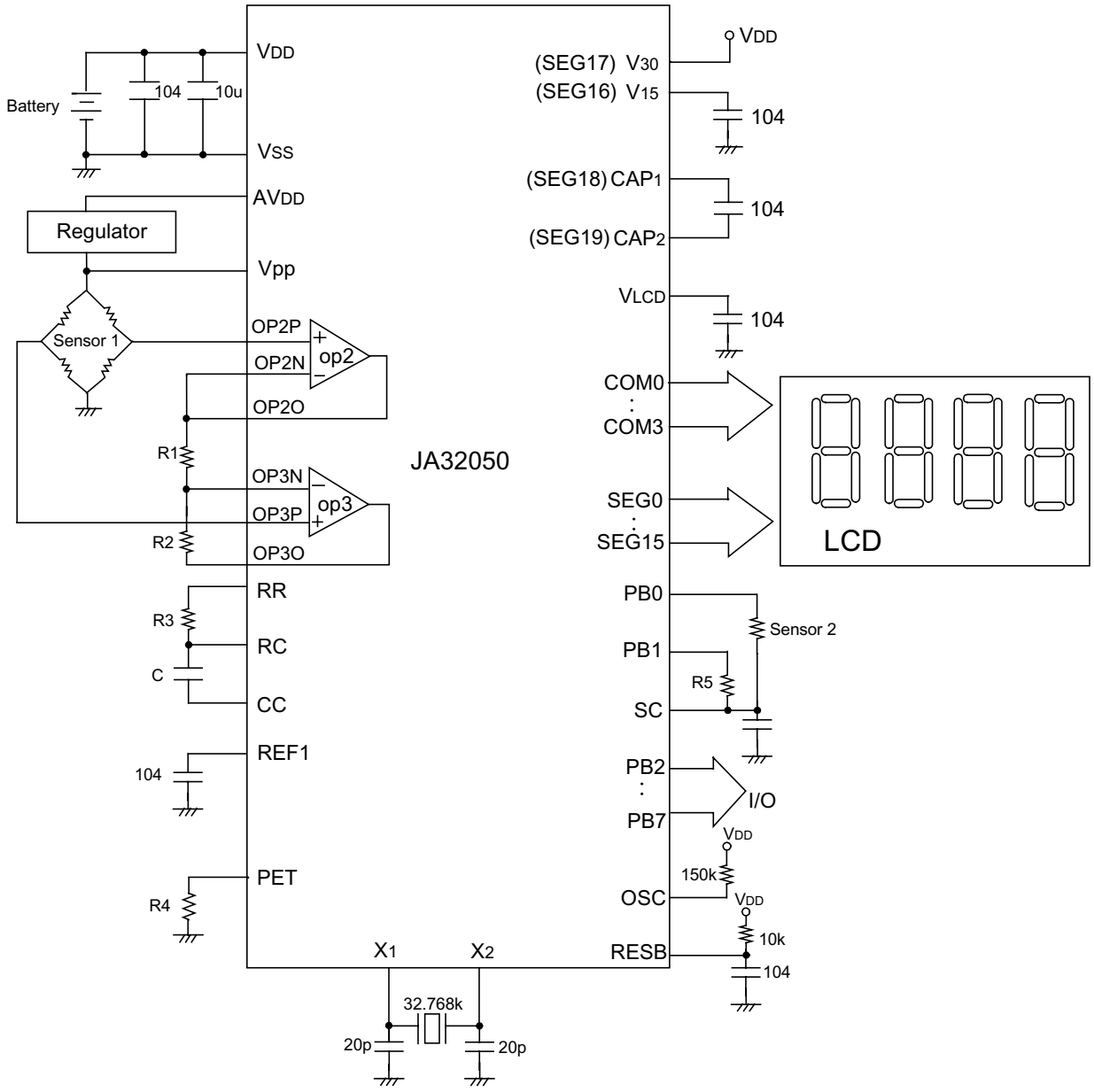
- ADC Timing Diagram



T1(Charge): The fixed charge time control by controller(MCU).
T2 (Discharge): The discharge time provide to controller(MCU).
CC: The voltage charge/discharge on pin CC

Application Diagram

The application diagram shown below is a simple illustration for using the JA32050 chip. It shall be noted that inside the JA32050, PA is dedicated to ADC circuit (PA5 for ON/OFF control(PA6 for COMPO, PA4 for CHAR/DIS control). Vdd:3 V and C type 1/3 bias were used in this application.



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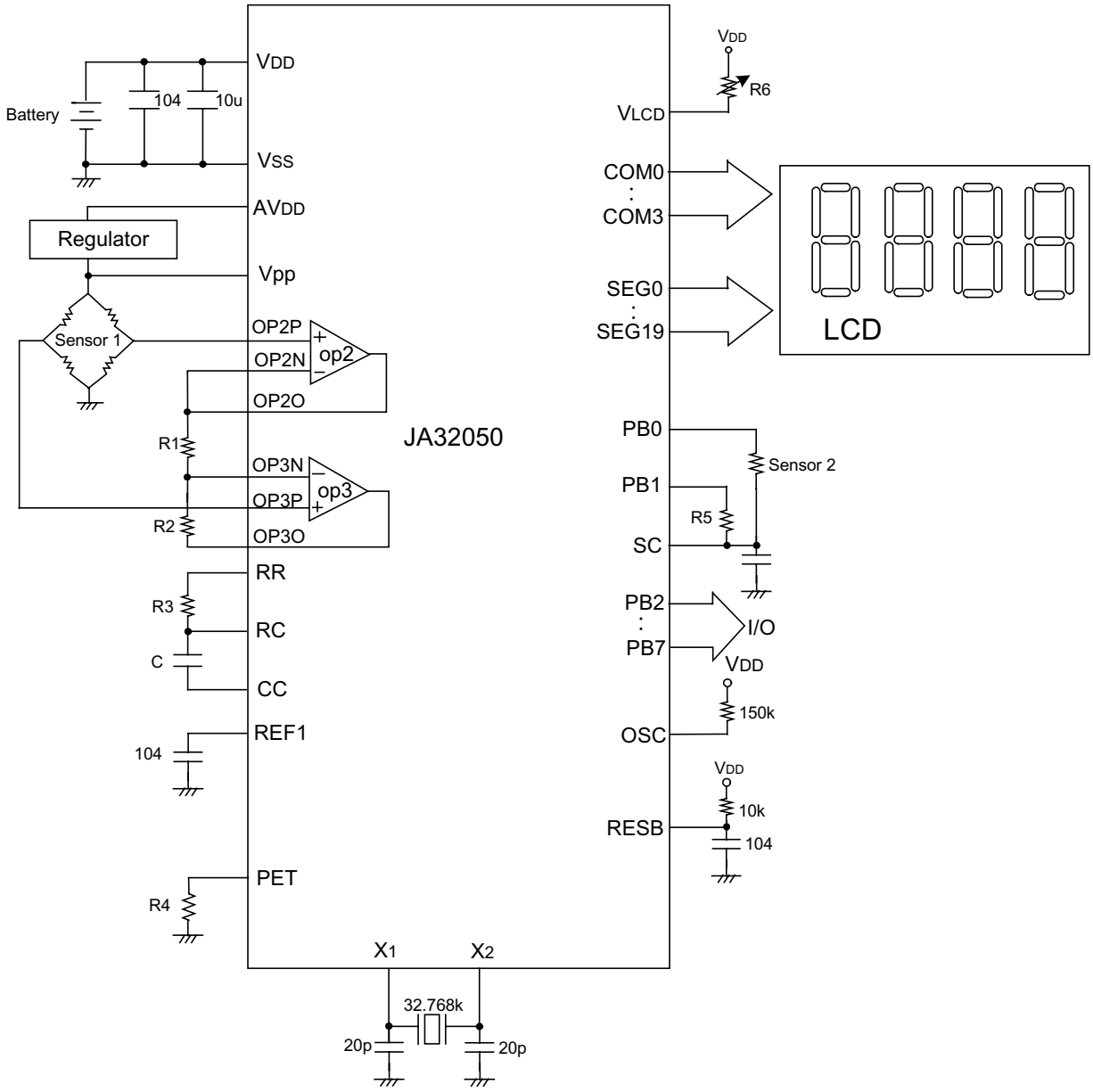
The application shown below uses R type bias for LCD biasing. All segments (SEG0 – SEG19) can be used.



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Note:

a. Pin 8 VDD shall be connected to power supply input.
b. Pin 9 AVDD is the voltage output controlled by PA5.
c. Pin 10 VPP is a voltage input pin used for sensor power supply and OP operation.
d. If no voltage regulation for VPP is needed, connect AVDD to VPP.
e. If VPP needs a regulated voltage level, use AVDD as the input voltage to an external regulator then connects the output of the regulator to the VPP.

Application Introduction

The circuit above was designed for multi function application. It handles two sensors of different functions. Sensor 1 can be pressure related type sensor such as sensors for manometer or sphygmomanometer application. Sensor 2 is the kind of sensor that output different resistance when the outside environment changes such as temperature sensor. Please see the following introduction for reference:

a. System Clock: External RC oscillation was used to generate the system clock. The OSC was connected to Vdd through a 150 k ohm resistor; the system clock will be around 4 MHz.
b. 32.768 k Crystal: This crystal used to generate real time clock.
c. Sensor 1: The ADC circuit was used by sensor 1. Sensor 1 can be pressure related type sensor such as sensors for manometer, sphygmomanometer application.
d. OP gain: R2, R3 decides the OP gain.
e. Charge/Discharge circuit: R3, C forms the charge/discharge path.
f. REF1, REF2: capacitors were connected to filter the noise.
g. R4: used for low voltage detect.
h. Sensor 2: R/F circuit was used by sensor 2. The reference resistor R5 was connected to PB1.
i. General I/O: PB2 – PB7 reserved for general I/O
j. LCD: COM0-COM3, SEG0-SEG15 were used for LCD interface.
k. LCD C bias type: In this application, C bias was used so the V15, CAP1, CAP2 shall need capacitor for C type bias.
l. Vlcd & V30: In this application Vdd = 3 V, and 1/3 bias was used for LCD, the V30 shall be connected to Vdd and Vlcd needs a capacitor to Vss.

Programming Example

The following program is an example for JA32050 programming. It demonstrates how MCU controls the ADC circuit. This program also shows users the way to configure the JA32050. User can learn some programming skills listed below:

a. Program format
b. Assign program memory location
c. PA, PB configuration
d. Timers enable/disable
e. ADC control
f. Interrupt routine handle

```
;
;
;
;-----------------------------------------------------------------
; This is an example program for JA32050 programming
;-----------------------------------------------------------------
;I/O port description:
;PA0-PA7 for ADC control(COMPO,ON/OFF,CHR)
;PB0-PB3 for press key
;
;Main program brief description
;a. MCU set up internal registers
```


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```
;b. MCU enable timer0 and asserts CHR(charge) signal to inform ADC starts charging
;c. MCU disable timer0 and asserts DISC signal to inform ADC starts discharging
;d. MCU enables timer1 to count discharge time simultaneously
;d. ADC asserts COMPO low when CC reaches 1/6 Vdd
;e. MCU stop timer1 counting when COMPO low detected
;f. Timer1 content was ready to read out
;-----------------------------------------------------------------

; MCU internal register address definition

POWERC     =      $00
INTC       =      $01
INTF       =      $02
WDTCLR     =      $03
WDTC       =      $05
TMR0L      =      $06
TMR0C      =      $07
TMR1L      =      $09
TMR1C      =      $0a
PA         =      $0b    ; ADC control
PAC        =      $0c
PAR        =      $0d
PB         =      $0e
PBC        =      $0f
PBR        =      $10
CON0       =      $21
LCD0       =      $23
LCD1       =      $24
SEG0       =      $200
SEG1       =      $201
SEG2       =      $202
SEG3       =      $203
SEG4       =      $204
SEG5       =      $205
SEG6       =      $206
SEG7       =      $207
SEG8       =      $208
SEG9       =      $209
SEG10      =      $20a
SEG11      =      $20b
SEG12      =      $20c


;================================================
; General purpose data memory & stack
;================================================
   Temp         = $e0h
   DELAY        = Temp+1
   COUNT        = DELAY+1
   Timer1_h     = COUNT+1
 ;=============================================
 ;
 ;Program located from $e400
 ;


       org $e400
```

```
START:

    cld                 ;clear decimal flag
    clc                 ;clear carry flag
    clv                 ;clear overflow flag
    cli                 ;clear interrupt disable flag, allow MCU accept INT

    lda   #$00
    sta   TMR0H          ;clear timer0 high byte
    sta   TMR0L          ;clear timer0 low byte
    sta   TMR1L          ;clear timer1 low byte

    lda   #$0e           ;"0000,1110" TMR clk rate= 1:256 ,timer disable
    sta   TMR0C          ;initial for TMR0
    lda   #$04           ;"0000,0100" TMR clk rate= 1:8 ,timer disable
    sta   TMR1C          ; initial for TMR1

    ldx   #$ff          ;initial stack pointer address from $FF
    txs                 ;copy x register value to stack pointer


    lda   #$40           ;"0100,0000"configure PA6 as input port
    sta   PAC
    lda   #$f0           ;"1111,0000" PA4-PA7 pull-high resistor
    sta   PAR
    lda   #$00          ;"0000,0000"
    sta   PA            ;PA0-PA7 , output low

    lda   #$0f           ;configure PB0-PB3    as input port, PB4-PB7 as output
    sta   PBR
    sta   PBC
    lda   #$ff
    sta   PB            ;PB4-PB7 output high

LCD_INIT:               ;LCD initial and clear
    lda   #$88           ; LCD clock source: internal 32k clock, LCD "on"
    sta   CON0           ; CON0 bit 7 was not used for real chip
    lda   #$46           ; LCD: 3 common, LCD0 bit0-bit2 was not used for real chip
    sta   LCD0
    lda   #$04           ; LCD: 1/2 bias
    sta   LCD1
    jsr   LCD_CLEAR

ON_OFF:
    lda   #$20           ;"0010,0000",enable ADC
    ora    PA
    sta   PA

CHARGE_HI:
     lda   #$10          ;"0001,0000",output CHARGE high
     ora    PA
     sta   PA

  TMR1_ON:
     lda   #$01          ; enable timer0 for charge time
     ora    TMR1C
```

```
        sta   TMR1C

   CHARGE_TIME:
        lda      TMR0L          ;charge time loop; leave the loop when time up
        cmp     #$b0
        bne     CHARGE_TIME

   TMR1_OFF:
        lda     #$fe                ; charge done, disable the timer0 "1111,1110"
        and    TMR1C
        sta     TMR1C

        lda     #$00                ; clear timer1 content for next charging
        sta     TMR1L


DISCHARGE_ON:
        lda      #$ef               ;"1110,1111", assert low signal to start discharging
        and     PA
        sta      PA

TMR0_ON:
        lda    #$00                ; clear timer0 content
        sta    TMR0L
        sta    TMR0H
        lda    #$01             ; enable timer0 for discharge time counting
        ora    TMR0C
        sta    TMR0C

COMPO:
        lda    #$40                ;"0100,0000"

   WAIT:
        bit     PA                 ;checking if PA6 is zero or not
        bne    WAIT

TMR0_OFF:
        lda     #$fe               ; charge done, disable the timer1 "1111,1110"
        and    TMR0C
        sta     TMR0C
        jsr     DLY1
        jmp    CHARGE_HI ;run again
;----------------------------------------
    LCD_CLEAR:
        lda    #$00
        ldx    #$00
        ldy    #$0e             ;14 times
    NEXT_BYTE:
        sta    SEG0,x
        inx
        dey
        bne    NEXT_BYTE
        rts
;--------- subroutine DLY1 ------------
DLY1:
         lda    #$ff
         sta    DELAY          ; DELAY = 256
```

```
        sta   COUNT          ; COUNT = 256
Loop1:
        nop
        nop
        dec   COUNT
        bne   Loop1
        nop                  ; now count = 0
        nop
        dec   DELAY
        bne   Loop1
        rts
;-------------------------------------
;Interrupt service routine
;-------------------------------------

INTHANDLE:
        sei                  ;disable INT
        pha                  ;push A register
        php                  ;push status register

        lda    #$02
        bit    INTF          ; timer0 INT?
        bne    TIMER0_INT ; timer0
        lda    #$04
        bit    INTF          ; timer1 INT?
        bne    TIMER1_INT ; timer1

    TIMER0_INT:
        lda    #$fd           ;"1111,1101", clear timer0 flag
        and    INTF
        sta    INTF
        jmp    INT_RTN
   TIMER1_INT:
        lda    #$fb           ;"1111,1011", clear timer1 flag
        and    INTF
        sta    INTF
        inc    timer1_h       ; add carry
        jmp    INT_RTN

   INT_RTN:
        plp                  ;pop status register
        pla                  ;pop A register
        cli                  ;enable INT
        rti
;--------------------------------------
       org    $fffc
       dw     START          ;FFFC - FFFD : store program start address
       dw     INTHANDLE      ;FFFE - FFFF : store interrupt subroutine address
       ends
       end
```


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