Features

- Fast Read Access Time - 150 ns
- Low Power
  - 40 mA Maximum (Active)
  - 1 mA Maximum (Standby)
- 2-V Data Retention
- Fully Static: No Clock Required
- Three Control Inputs ($\overline{CE_1}$, CE_2, and $\overline{OE}$)
- TTL Compatible Inputs and Outputs
- 5 V ± 10% Supply
- 28-Lead Dual In-line
- JEDEC Pinout
- Full Military Temperature Range

64K (8K x 8) CMOS SRAM

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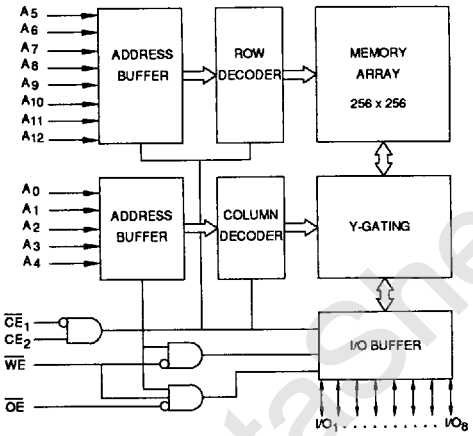
Block Diagram



Description

The AT3864L-15DMB is a high performance CMOS static Random Access Memory. Its 64K of memory is organized as 8192 words by 8 bits. Manufactured with an advanced CMOS technology, the AT3864L-15DMB offers access times down to 150 ns with power dissipation of 220 mW maximum. When the AT3864L-15DMB is deselected, the standby current is just 1 mA. In addition, the AT3864L-15DMB offers a data retention capability of only 800 µW power dissipation when operated on a 2 V power supply.

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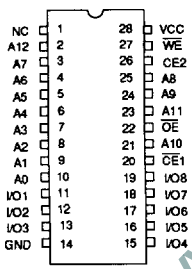
Pin Configurations

Pin Name	Function
A_0-A_{12}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE_1}$, CE_2	Chip Enables
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground
NC	No Connect



Description (Continued)

The AT3864L-15DMB powers down to the standby mode when deselected ($\overline{CE_1}$ is HIGH or CE_2 is LOW). The I/O pins remain in the high impedance state unless the chip is selected ($\overline{CE_1}$ is LOW and CE_2 is HIGH), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT3864L-15DMB is completely TTL compatible and requires a single 5-V power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 150° C
Storage Temperature	-65° C to 150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3 V to V_{CC}+0.3 V
All Output Voltages with Respect to Ground	-0.3 V to V_{CC}+0.3 V
Maximum Supply Voltage	+7.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the eight bits of data stored at the memory location determined by the address input (pins A_0 through A_{12}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE_1}$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW, the eight bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{12}).

DATA RETENTION: When the chip is in standby mode, V_{CC} can be reduced to as low as two volts without impacting data integrity. Power dissipation will be reduced to 800 µW maximum.

Operating Modes

MODE\PIN	$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	H	L	H	D_{OUT}
Write	L	H	X(1)	L	D_{IN}
$Standby_1$	H	X	X	X	High Z
$Standby_2$	X	L	X	X	High Z
Output Disable	X	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT3864L-15
Operating Temperature (Case)	Military	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%

D.C. and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$\overline{CE_1}$ = 2.2 V to V_{CC} + 0.3 V or CE_2 = -0.3 V to 0.8 V or $\overline{OE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{WE}$ = -0.3 V to 0.8 V $V_{I/O}$ = 0 to V_{CC}	-1.0		1.0	µA
I_{SB1}	Standby Current (CMOS)	$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CC}$ - 0.2 V, $CE_2 \ge V_{CC}$ - 0.2 V or $CE_2 \le 0.2$ V V_{IN} = 0 to V_{CC}			1	mA
I_{SB2}	Standby Current (TTL)	CE_2 = -0.3 V to 0.8 V or $\overline{CE_1}$ = 2.2 V to V_{CC} +0.3 V, V_{IN} = 0 to V_{CC}			3	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE_1}$ = -0.3 V to 0. 8V, CE_2 = 2.2 V to V_{CC} + 0.3 V, I_{OUT} = 0 mA, min cycle		20	40	mA
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		2.2 V		V_{CC}+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4			V

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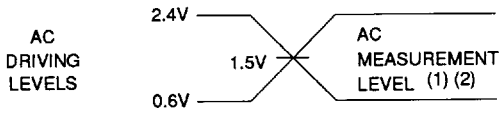
Pin Capacitance (f = 1 MHz, T = 25°C) [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0 V		6	10	pF
C_{IN}	Input Capacitance	V_{IN} = 0 V		6	10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Input Test Waveforms and Measurement Levels



Notes: 1. Input rise and fall time 5 ns.
2. Output load: 1TTL gate + 100 pF.

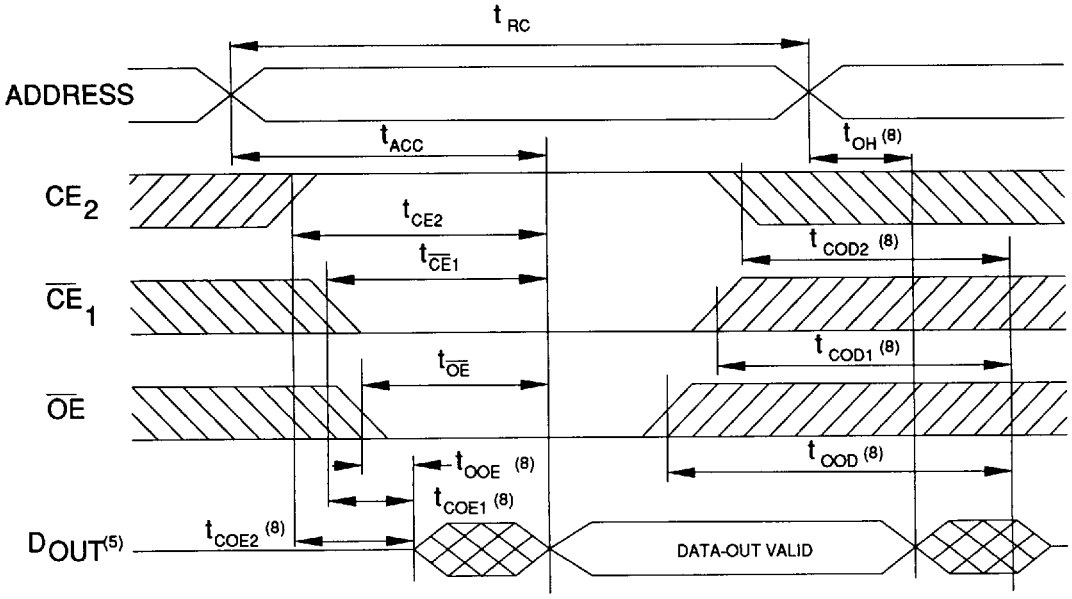
A.C. Characteristics for Read

Symbol	Parameter	AT3864L-15		Units
		Min	Max	
t_{RC}	Read Cycle Time	150		ns
t_{ACC}	Address Access Time		150	ns
$t_{\overline{CE}1}$,t_{CE2}	$\overline{CE}_1$,CE_2 Access Time		150	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		70	ns
t_{OH}	Output Hold Time	15		ns
$t_{COE1,2}$	$\overline{CE}_1$, CE_2 Output Enable Time	10		ns
t_{OOE}	$\overline{OE}$ Output Enable Time	5		ns
$t_{COD1,2}$	$\overline{CE}_1$, CE_2 Output Disable Time		60	ns
t_{OOD}	$\overline{OE}$ Output Disable Time		50	ns

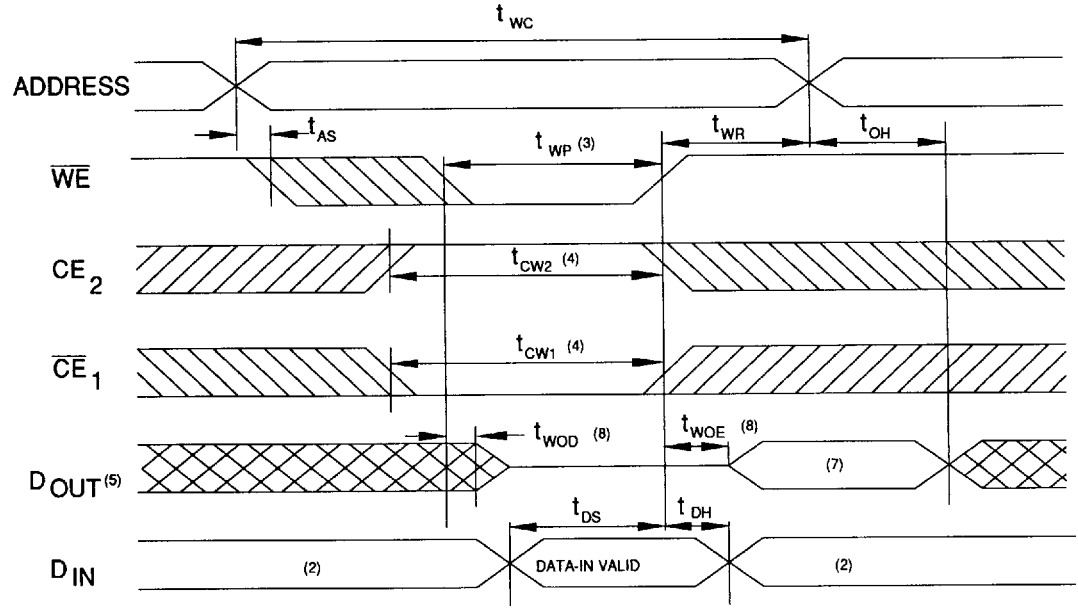
A.C. Characteristics for Write

Symbol	Parameter	AT3864L-15		Units
		Min	Max	
t_{WC}	Write Cycle Time	150		ns
t_{AS}	Address Setup Time	0		ns
t_{WP}	Write Pulse Width	90		ns
$t_{CW1,2}$	$\overline{CE}_1$, CE_2 Setup Time	90		ns
t_{WR}	Write Recovery Time	0		ns
$t_{WR1,2}$	$\overline{CE}_1$, CE_2 Write Recovery Time	0		ns
t_{DS}	Data Setup Time	60		ns
t_{DH}	Data Hold Time	0		ns
$t_{DH1,2}$	$\overline{CE}_1$, CE_2 Data Hold Time	0		ns
t_{WOE}	$\overline{WE}$ Output Enable Time	5		ns
t_{WOD}	$\overline{WE}$ Output Disable Time		50	ns

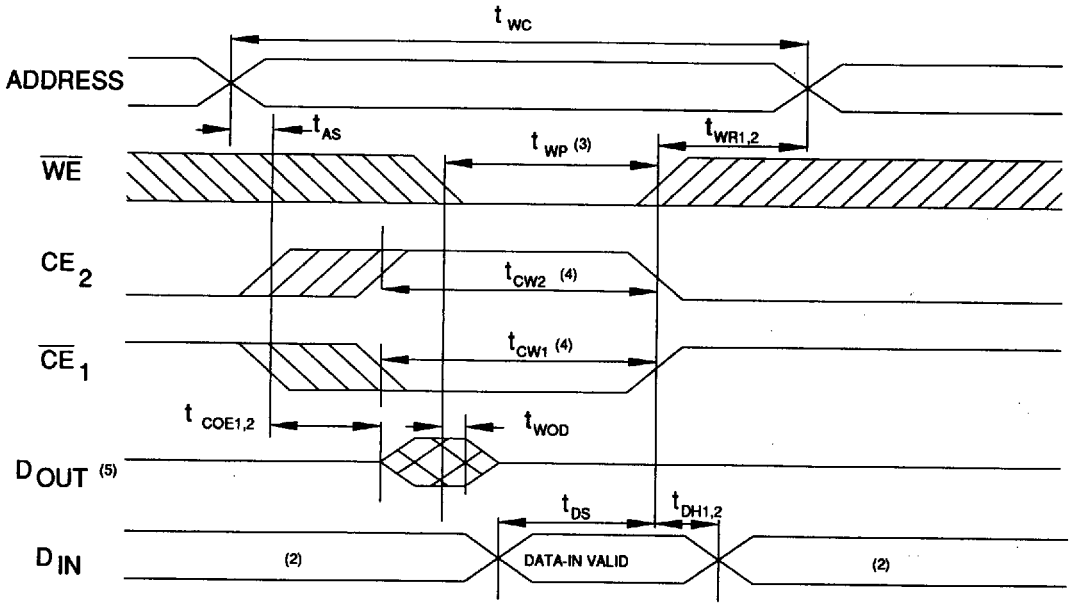
A.C. Waveforms for Read Cycle [1]



A.C. Waveforms for Write Cycle 1 (WE Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) (6)



Notes:
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE}_1$ is LOW, CE_2 is HIGH, and $\overline{WE}$ is LOW.
   A Write begins at the latest transition among $\overline{CE}_1$ going LOW, CE_2 going HIGH and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE}_1$ going HIGH, CE_2 going LOW and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE}_1$ going LOW or CE_2 going HIGH to the end of Write.
5. If $\overline{OE}$ or $\overline{CE}_1$ is HIGH, or CE_2 or $\overline{WE}$ is LOW, D_{OUT} goes to a HIGH impedance state.
6. During a write cycle, $\overline{OE}$ = V_{IH} or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.
8. Parameter is sampled and not 100% tested.

Data Retention Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Power Supply Voltage	VDR1	$\overline{CE_1} \geq V_{CC}$ - 0.2 V $CE_2 \geq V_{CC}$ - 0.2 V or $CE_2 \leq 0.2$ V	2.0		5.5	V
	V_{DR2}	$CE_2 \leq 0.2$ V	2.0		5.5	
Data Retention Current	I_{CCDR1}	V_{CC} = 3.0 V $\overline{CE_1} \geq V_{CC}$ - 0.2 V $CE_2 \geq V_{CC}$-0.2 V or $CE_2 \leq 0.2$ V		1	400	µA
	I_{CCDR2}	V_{CC} = 3.0 V, $CE_2 \leq 0.2$ V		1	400	µA
Chip Enable Setup Time	t_{CDR}		0			ns
Chip Enable Hold Time	t_R		t_{RC}(1)			ns

Note: 1. t_{RC} = Read Cycle Time

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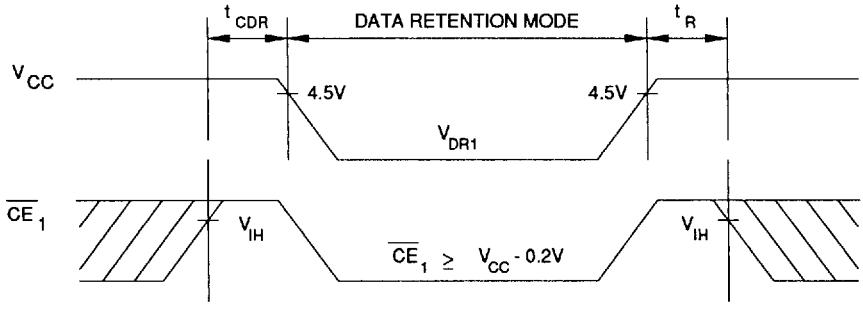
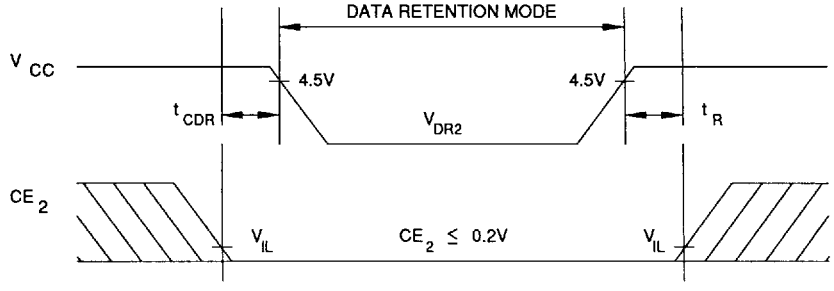
Data Retention Waveform 1 ($\overline{CE}_1$ Control)



Data Retention Waveform 2 (CE 2 Control)



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	40	1.0	AT3864L-15DMB	28D6	Military (-55° to 125°C)

Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)