

DRAM

64K x 4 DRAM

FAST PAGE MODE

AVAILABLE AS MILITARY SPECIFICATION

- SMD 5962-92132
- MIL-STD-883

FEATURES

- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 15mW standby; 150mW active, typical
- Optional PAGE MODE access cycle
- Refresh modes: RAS\-ONLY, CAS\-BEFORE-RAS, and HIDDEN
- 256-cycle refresh distributed across 4ms
- Specifications guaranteed over full military DRAM temperature range (-55°C to +125°C)

OPTIONS

- Timing
- | | |
|--------------|-----|
| 100ns access | -10 |
| 120ns access | -12 |
| 150ns access | -15 |

MARKING

- Packages
- | | | |
|-----------------------|----|---------|
| Ceramic DIP (300 mil) | C | No. 101 |
| Ceramic LCC | EC | No. 200 |
| Ceramic LCC | EA | No. 201 |

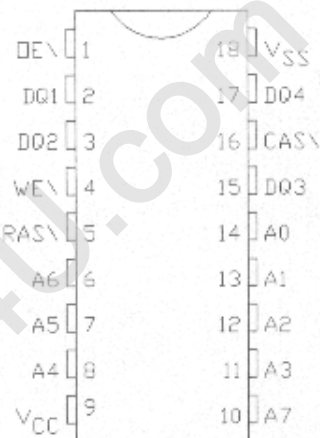
NOTE: Contact factory for other package options.

GENERAL DESCRIPTION

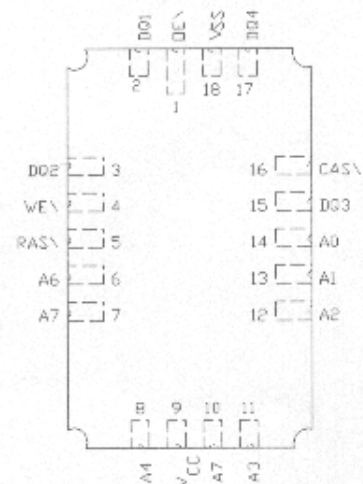
The AS4C4067 883C is a randomly accessed solid-state memory containing 262,144 bits organized in a 65,536 x 4 configuration. The 16 address bits are entered 8 bits at a time using RAS\ to latch the first 8 bits and CAS\ the latter 8 bits. If WE\ goes LOW after data reaches the output pins, the output pins are activated and retain the selected cell data as long as CAS\ and OE\ remain LOW (regardless of WE\ or RAS\). This late WE\ pulse results in a READ-MODIFY-WRITE cycle. Data in is latched when WE\ strobes LOW. CAS\ may be toggled-in by holding RAS\ LOW to execute several faster READ, WRITE or READ-MODIFY-WRITE cycles within the RAS\ address defined page boundary. Returning RAS\ HIGH terminates the memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS\ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing a RAS\ (READ, WRITE, RAS\-ONLY or HIDDEN REFRESH) cycle so that all 256 combinations of RAS\ addresses are executed at least every 4ms (regardless of sequence).

PIN ASSIGNMENT (Top View)

18-Pin DIP

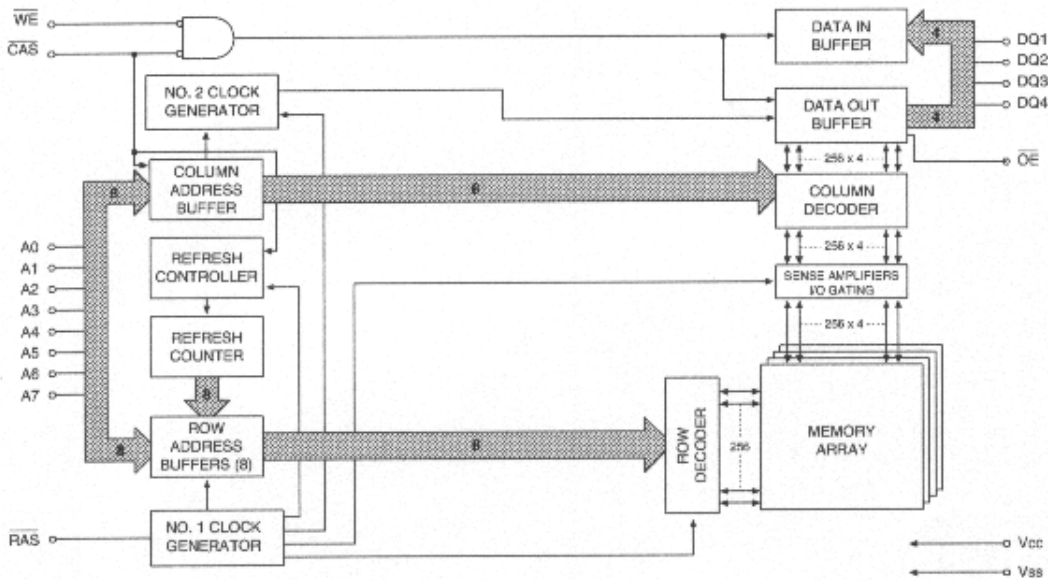


18-Pin LCC





EQUIVALENT FUNCTIONAL BLOCK DIAGRAM
PAGE MODE



TRUTH TABLE

FUNCTION	RAS	CAS	WE	OE	ADDRESSES		
					t _R	t _C	
Standby	H	H	H	H	X	X	High-Z
READ	L	L	H	L	ROW	COL	Data Out
WRITE (EARLY-WRITE)	L	L	L	X	ROW	COL	Data In
READ-WRITE	L	L	H→L→H	L→H	ROW	COL	Data Out, Data In
PAGE-MODE READ	L	H→L→H	H	L	ROW	COL	Data Out, Data Out
PAGE-MODE WRITE	L	H→L→H	L	X	ROW	COL	Data In, Data In
PAGE-MODE READ-WRITE	L	H→L→H	H→L→H	L→H	ROW	COL	Data Out, Data In
RAS-ONLY REFRESH	L	H	X	H	ROW	n/a	High-Z
HIDDEN REFRESH	L→H→L	L	H	L	ROW	COL	Data Out
CAS-BEFORE-RAS REFRESH	H→L	L	H	X	X	X	High-Z



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss -1.5V to +7.0V
 Storage Temperature Range -65°C to +150°C
 Power Dissipation 1 Watt
 Lead Temperature (soldering 5 sec.) 300°C
 Junction Temperature (Tj) +150°C
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 4, 6, 7) (-55°C ≤ T_C ≤ +125°C; V_{CC} = 5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Current from V _{CC} (Active); \overline{RAS} and \overline{CAS} Cycling; t _{RC} = t _{PC} (MIN)	I _{CC1}		70	mA	2
Supply Current from V _{CC} (Active, PAGE MODE); \overline{RAS} = V _{IL} , \overline{CAS} Cycling; t _{PC} = t _{PC} (MIN)	I _{CC2}		65	mA	2
Supply Current from V _{CC} (Standby); \overline{RAS} and \overline{CAS} = V _{IH}	I _{CC3}		8	mA	
Supply Current from V _{CC} (REFRESH, \overline{RAS} only); \overline{RAS} Cycling, \overline{CAS} = V _{IH}	I _{CC4}		70	mA	2
Supply Current from V _{CC} (REFRESH, \overline{CAS} -BEFORE- \overline{RAS}); \overline{RAS} and \overline{CAS} Cycling	I _{CC5}		70	mA	2
Output High Voltage (I _{OH} = -5mA)	V _{OH}	2.4		V	1
Output Low Voltage (I _{OL} = 5mA)	V _{OL}		0.4	V	1
Input Leakage	I _{IH}	-5	5	μA	
Any input (0V ≤ V _{IN} ≤ V _{CC}), all other pins = 0V	I _{IL}	-5	5	μA	
Output Leakage (0 ≤ V _{OUT} ≤ V _{CC})	I _{OZ}	-5	5	μA	

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
V _{CC} Supply Voltage	V _{CC}	4.5	5.5	V	
V _{SS} Power Supply and Signal Reference	V _{SS}	0.0	0.0	V	1
High Level Input Voltage, all inputs	V _{IH}	2.4	V _{CC} +0.5	V	1
Low Level Input Voltage, all inputs	V _{IL}	-0.5	0.8	V	1

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A8	C _{I1}		7	pF	2
Input Capacitance: \overline{RAS} , \overline{CAS} , WE, OE	C _{I2}		7	pF	2
Output Capacitance: DQ	C _O		8	pF	2

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 4, 5, 6, 7, 8) (-55°C ≤ T C ≤ 125°C, VCC = 5.0V ±10%)

AC CHARACTERISTICS		-10		-12		-15			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	[†] RC	180		210		250		ns	
READ-MODIFY-WRITE cycle time	[†] RWC	245		280		330		ns	20
PAGE-MODE cycle time	[†] PC	75		90		110		ns	20
Access time from RAS\	[†] RAC		100		120		150	ns	9
Access time from CAS\	[†] CAC		50		60		75	ns	10
RAS\ pulse width	[†] RAS	100	10,000	120	10,000	150	10,000	ns	
CAS\ pulse width	[†] CAS	50	10,000	60	10,000	75	10,000	ns	
RAS precharge time	[†] RP	70		80		90		ns	
RAS hold time	[†] RSH	50		60		75		ns	
RAS\ to CAS\ delay time	[†] RCD	25	50	30	60	35	75	ns	16
CAS\ precharge time	[†] CPN	15		20		25		ns	20
CAS\ precharge time (PAGE-MODE)	[†] CP	15		20		25		ns	11
CAS to RAS\ set-up time	[†] CRP	5		5		5		ns	
CAS\ hold time	[†] CSH	110		120		150		ns	
Row address set-up time	[†] ASR	0		0		0		ns	20
Row address hold time	[†] RAH	15		15		20		ns	
Column address set-up time	[†] ASC	0		0		0		ns	20
Column address hold time	[†] CAH	20		25		25		ns	
Column address hold time referenced to RAS\	[†] AR	70		80		100		ns	
READ command set-up time	[†] RCS	0		0		0		ns	20
READ command hold time referenced to CAS\	[†] RCH	0		0		0		ns	20
READ command hold time referenced to RAS\	[†] RRH	10		10		10		ns	
Output disable delay	[†] OFF	0	20	0	20	0	25	ns	12
Output disable	[†] OD		20		20		25	ns	12
Output Enable	[†] OE		25		25		30	ns	13
WRITE command set-up time	[†] WCS	0		0		0		ns	14
WRITE command hold time	[†] WCH	35		40		45		ns	
WRITE command hold time referenced to RAS\	[†] WCR	85		100		120		ns	
WRITE command pulse width	[†] WP	35		40		45		ns	
WRITE command to RAS\ lead time	[†] RWL	35		40		45		ns	
WRITE command to CAS\ lead time	[†] CWL	35		40		45		ns	
Data-in set-up time	[†] DS	0		0		0		ns	15,20
Data-in hold time	[†] DH	35		35		45		ns	15
Data-in hold time referenced to RAS\	[†] DHR	85		100		120		ns	
CAS\ to WRITE delay	[†] CWD	70		90		110		ns	14
RAS\ to WRITE delay	[†] RWD	125		145		180		ns	14
Transition time (rise or fall)	[†] T	3	50	3	50	3	50	ns	20
CAS\ set-up time (CAS-BEFORE-RAS REFRESH)	[†] CSR	10		10		10		ns	17
CAS\ hold time (CAS-BEFORE-RAS REFRESH)	[†] CHR	20		25		30		ns	17
Refresh period (256 cycles distributed)	[†] REFD		4		4		4	ms	18
Refresh period (256 cycles burst)	[†] REFB		4		4		4	ms	19
RAS\ to CAS\ precharge time	[†] RPC	0		0		0		ns	20
WE\ set-up time before RAS\ low	[†] WRP	10		10		10		ns	9,10,11
WE\ hold time after RAS\ low	[†] WRH	10		10		10		ns	9,10,11
CAS\ before RAS\ refresh									

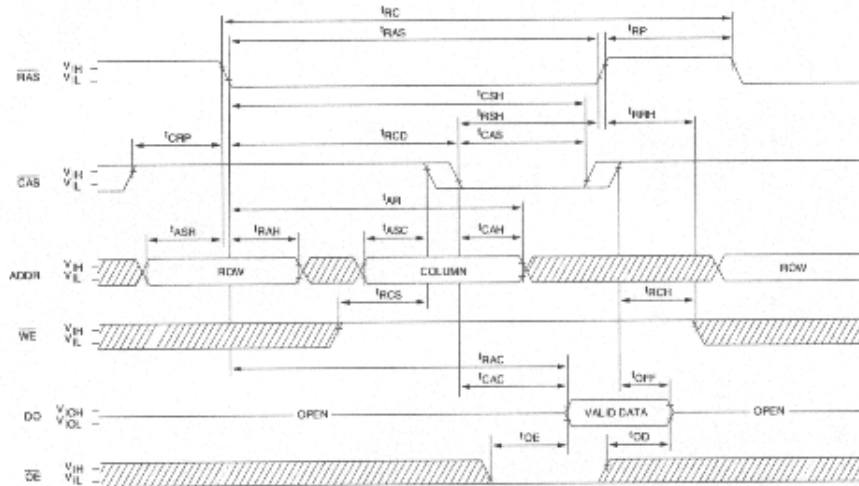


NOTES

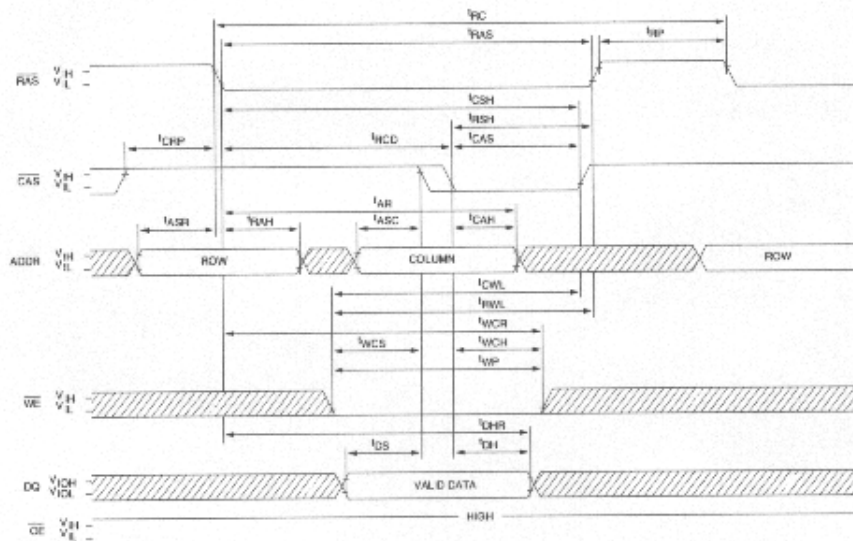
1. All voltages referenced to V_{SS} .
2. Specified values are obtained with the output load equal to 2TTL loads and 100pF to V_{SS} .
3. This parameter is sampled. $V_{CC} = 5V \pm 10\%$, $f = 1$ MHz.
4. An initial pause of 100 μ s is required after power-up followed by any 8 RAS only refresh cycles or CBR refresh cycle (\overline{WE} held high) before proper device operation is assured.
5. AC characteristics assume transition time (t_T) = 5ns. This parameter is not measured.
6. V_{IL} (MAX) and V_{IH} (MIN) are reference levels for measuring timing of input signals. Transition times are measured between V_{IL} and V_{IH} .
7. In addition to meeting the transition rate specification, all input signals must transit between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
8. If $\overline{CAS} = V_{IH}$ or $\overline{OE} = V_{IH}$, DQs are High-Z. If $\overline{CAS} = V_{IL}$ or $\overline{OE} = V_{IL}$, DQs may contain data from the last valid READ cycle.
9. Assumes that $t_{RCD} < t_{RCD} (MAX)$.
10. Assumes that $t_{RCD} \geq t_{RCD} (MAX)$.
11. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , DQs will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, \overline{CAS} must be pulsed HIGH for t_{CP} . Note 8 applies to determine valid data out.
12. This parameter refers to the time when the outputs are no longer driven.
13. If \overline{OE} is taken LOW then HIGH, DQs go open. If \overline{OE} is tied permanently LOW a READ-WRITE or READ-MODIFY-WRITE operation requires a separate READ and WRITE cycle.
14. t_{WCS} , t_{CWD} and t_{RWD} are restrictive operating parameters in READ-MODIFY-WRITE cycle only. If $t_{WCS} \geq t_{WCS} (MIN)$ the cycle is an EARLY-WRITE cycle and the DQs will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD} (MIN)$ and $t_{RWD} \geq t_{RWD} (MIN)$, the cycle is a READ-WRITE and the DQs will contain data read from the selected address. When performing LATE-WRITE cycle t_{WCS} , t_{CWD} and t_{RWD} do not apply.
15. These parameters are referenced to \overline{CAS} leading edge in EARLY-WRITE cycles and to the \overline{WE} leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
16. Operation within the $t_{RCD} (MAX)$ limit ensures that $t_{RAC} (MAX)$ can be met. $t_{RCD} (MAX)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (MAX)$ limit, then access time is controlled exclusively by t_{CAC} .
17. Enables on-chip refresh and address counters.
18. A 256-cycle distributed refresh consists of an address location refresh cycle being performed within 15.625 μ s so that all 256 RAS address combinations are executed within 4ms (regardless of sequence). Micron recommends distributed refresh.
19. A 256-cycle burst refresh consists of refreshing, as rapidly as minimum cycle time allows, all 256 combinations of RAS addresses (regardless of sequence). The refresh mode must be executed within 4ms.
20. This parameter is a "conditionally" guaranteed parameter that is specified to aid with device application. It is not directly verified by a specific test but is used, with several other parameters, in the performance verification of other attributes.
21. A HIDDEN REFRESH may also be performed after a Write cycle. In this case $\overline{WE} = LOW$ and $\overline{OE} = HIGH$.



READ CYCLE



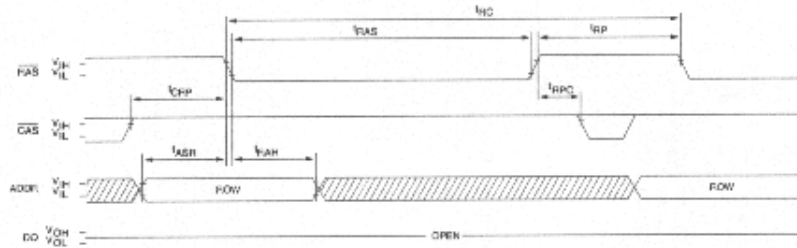
EARLY-WRITE CYCLE (OE = DONT CARE)



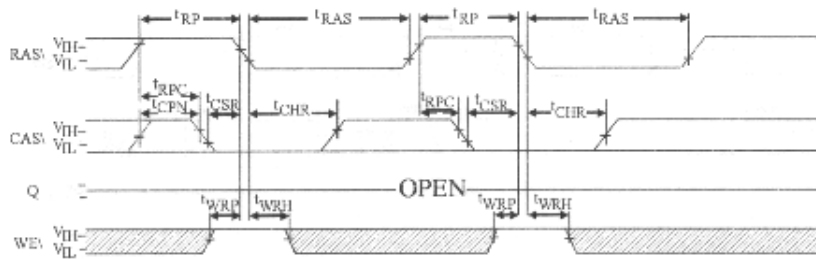
DONT CARE
 UNDEFINED



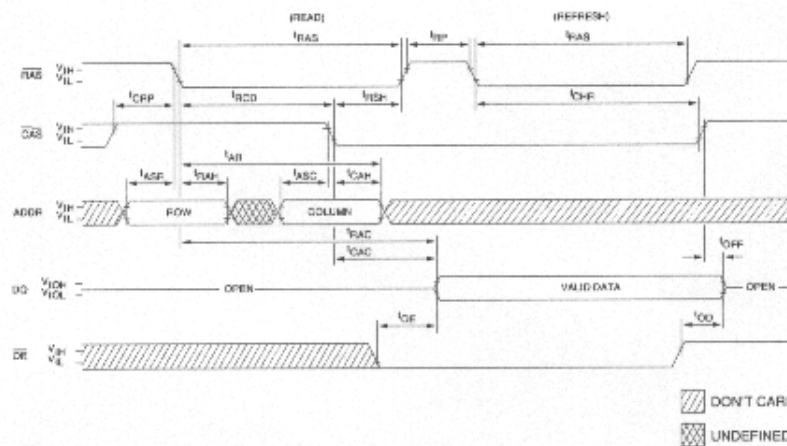
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A7; \overline{WE} = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A7; \overline{WE} , \overline{OE} = DON'T CARE)



HIDDEN REFRESH CYCLE²¹
(\overline{WE} = HIGH)





ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

