

**OKI** Semiconductor

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**MSM5716C50/MSM5718C50/  
MD5764802**

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**16M/18Mb (2M × 8/9) & 64Mb (8M × 8) Concurrent RDRAM**

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**DESCRIPTION**

The 16/18/64-Megabit Concurrent Rambus™ DRAMs (RDRAM®) are extremely high-speed CMOS DRAMs organized as 2M or 8M words by 8 or 9 bits. They are capable of bursting unlimited lengths of data at 1.67 ns per byte (13.3 ns per eight bytes). The use of Rambus Signaling Level (RSL) technology permits 600 MHz transfer rates while using conventional system and board design methodologies. Low effective latency is attained by operating the two or four 2KB sense amplifiers as high speed caches, and by using random access mode (page mode) to facilitate large block transfers. Concurrent (simultaneous) bank operations permit high effective bandwidth using interleaved transactions.

RDRAMs are general purpose high-performance memory devices suitable for use in a broad range of applications including PC and consumer main memory, graphics, video, and any other application where high-performance at low cost is required.

**FEATURES**

- Compatible with Base/LL RDRAMs
- 600 MB/s peak transfer rate per RDRAM
- Rambus Signaling Level (RSL) interface
- Synchronous, concurrent protocol for block-oriented, interleaved (overlapped) transfers
- 480 MB/s effective bandwidth for random 32 byte transfers from one RDRAM
- 13 active signals require just 32 total pins on the controller interface (including power)
- 3.3 V operation
- Additional/multiple Rambus Channels each provide an additional 600 MB/s bandwidth
- Two or four 2KByte sense amplifiers may be operated as caches for low latency access
- Random access mode enables any burst order at full bandwidth within a page
- Graphics features include write-per-bit and mask-per-bit operations
- Available in horizontal surface mount plastic package (SHP32-P-1125-0.65-K)

**PART NUMBERS**

The 16/18- and 64-Megabit RDRAMs are available in horizontal surface mount plastic package (SHP), with 533 and 600 MHz clock rate. The part numbers for the various options are shown in Table 1.

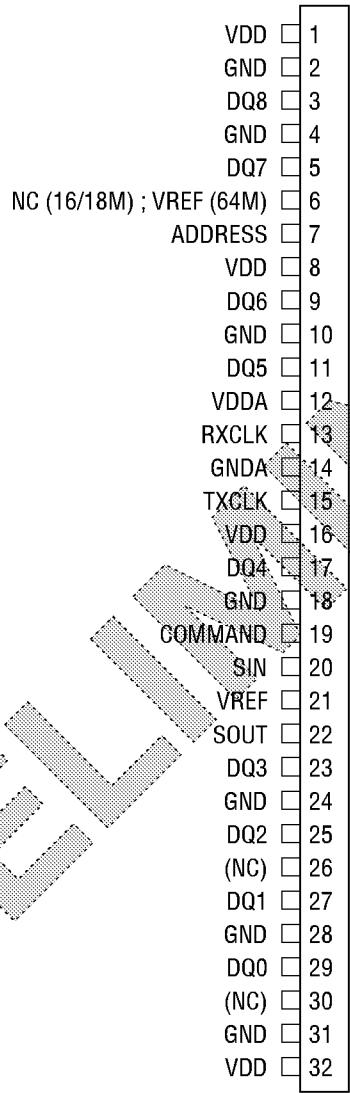
**Table 1 Part Numbers by Option**

Options	533 MHz	600 MHz
16-Megabit SHP	MSM5716C50-53GS-K	MSM5716C50-60GS-K
18-Megabit SHP	MSM5718C50-53GS-K	MSM5718C50-60GS-K
64-Megabit SHP	MD5764802-53GS-K	MD5764802-60GS-K

PRELIMINARY

**RDRAM PACKAGES AND PINOUTS**

RDRAMs are available in horizontal surface mount plastic package (SHP). The package has 32 signal pins and four mechanical pins that provide support for the device. The mechanical pins are located on the opposite side from the signal leads in the SHP.

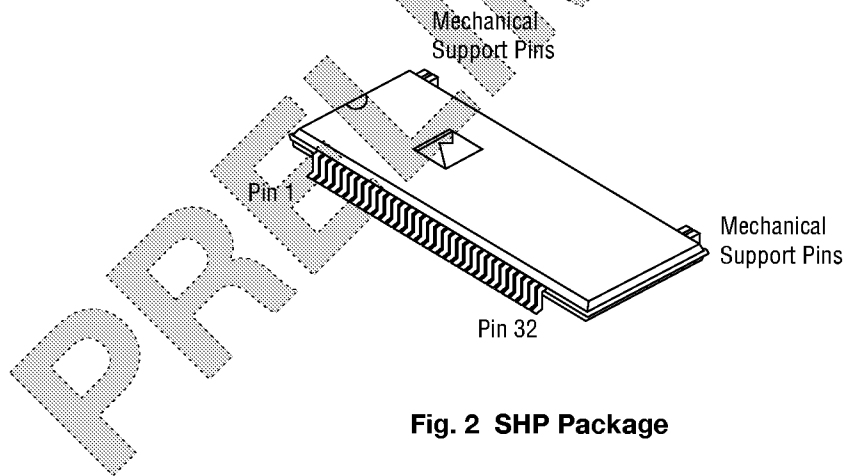


**Fig. 1 SHP Pin Numbering**

**Table 2 Pin Descriptions**

Signal	I/O	Description
DQ8..DQ0 (BUSDATA [8:0])	I/O	Signal lines for REQ, DIN, and DOUT packets. The REQ packet contains the address field, command field, and other control fields. These are RSL signals. <sup>a</sup>
CLK (RXCLK)	I	Receive clock. All input packets are aligned to this clock. This is an RSL signal. <sup>a</sup>
CLK (TXCLK)	I	Transmit clock. DOUT packets are aligned with this clock. This is an RSL signal. <sup>a</sup>
VREF	I	Logic threshold reference voltage for RSL signals.
COMMAND (BUSCTRL)	I	Signal line for REQ, RSTRB, RTERM, WSTRB, WTERM, RESET, and CKE packets. This is an RSL signal. <sup>a</sup>
ADDRESS (BUSENABLE)	I	Signal line for COL packets with column addresses. This is an RSL signal. <sup>a</sup>
VDD, VDDA	—	+3.3 V power supply. VDDA is a separate analog supply for clock generation in the RDRAM.
GND, GNDA	—	Circuit ground. GNDA is a separate analog ground for clock generation in the RDRAM.
SIN	I	Initialization daisy chain input. CMOS levels.
SOUT	O	Initialization daisy chain output. CMOS levels.

a. RSL stands for Rambus Signaling Levels, a low-voltage-swing, active-low signaling technology.

**Fig. 2 SHP Package**

## GENERAL DESCRIPTION

Figure 3 is a block diagram of an RDRAM. At the bottom is a standard DRAM core organized as two or four independent banks, with each bank organized as 512 or 1024 rows, and with each row consisting of 2KBytes of memory cells. One row of a bank may be "activated" at any time (ACTV command) and placed in the 2KByte "page" for the bank. Column accesses (READ and WRITE commands) may be made to this active page.

The smallest block of memory that may be accessed with READ and WRITE commands is an octbyte (eight bytes). Bitmask and bytemask options are available with the WRITE command to allow finer write granularity. There are six control registers that are accessed at initialization time to configure the RDRAM for a particular application.

PRELIMINARY

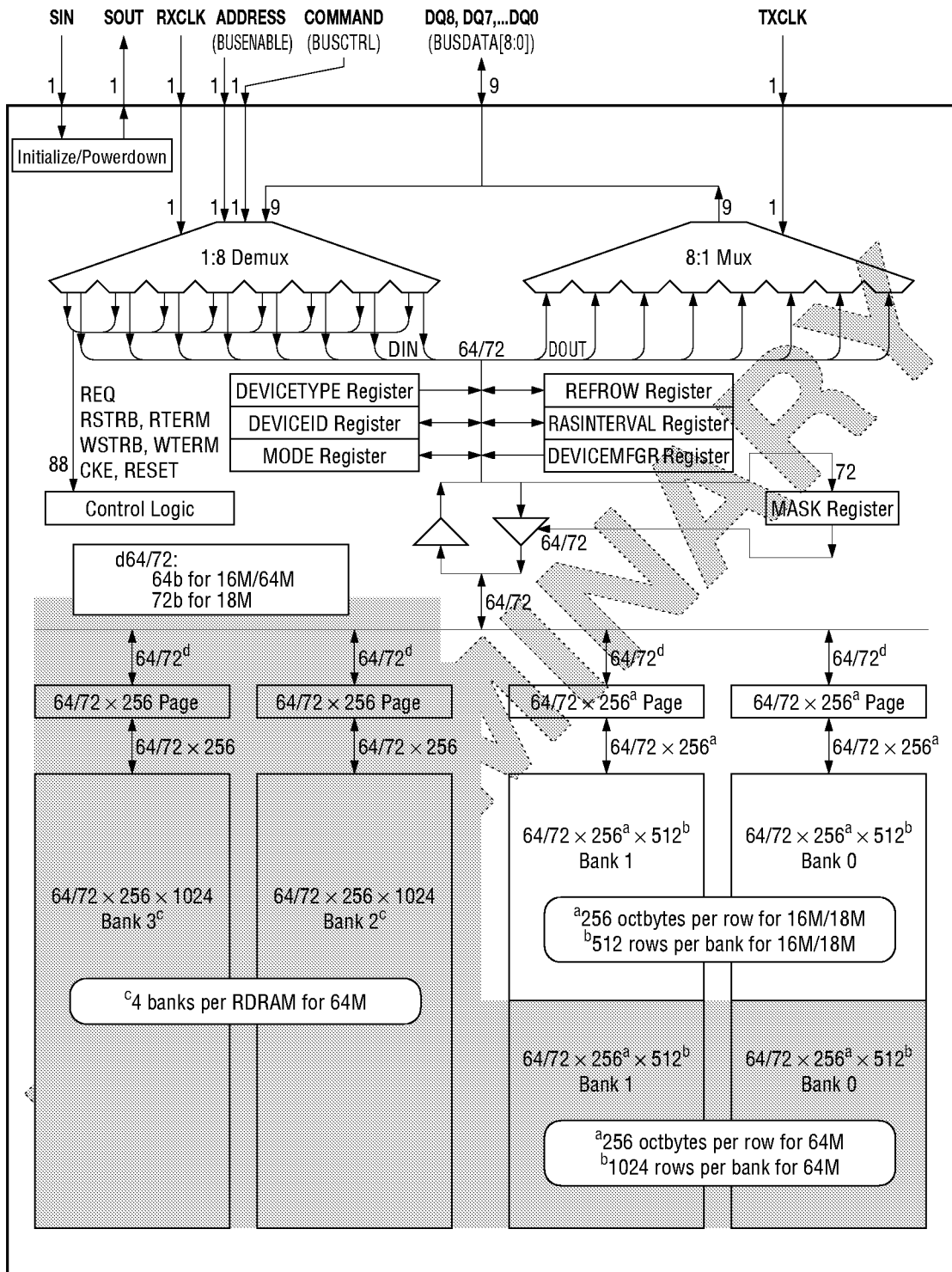
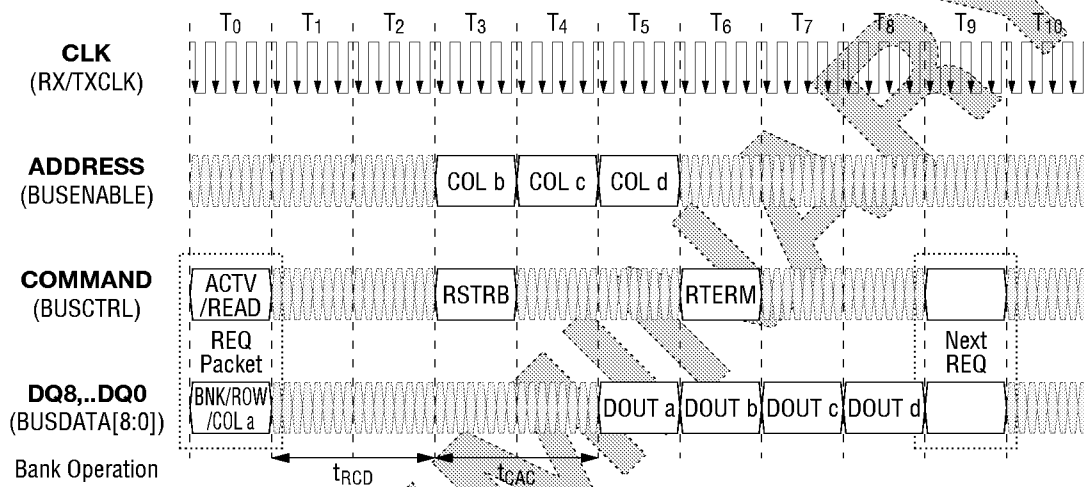


Fig. 3 16/18/64-Mbit Concurrent RDRAM Block Diagram

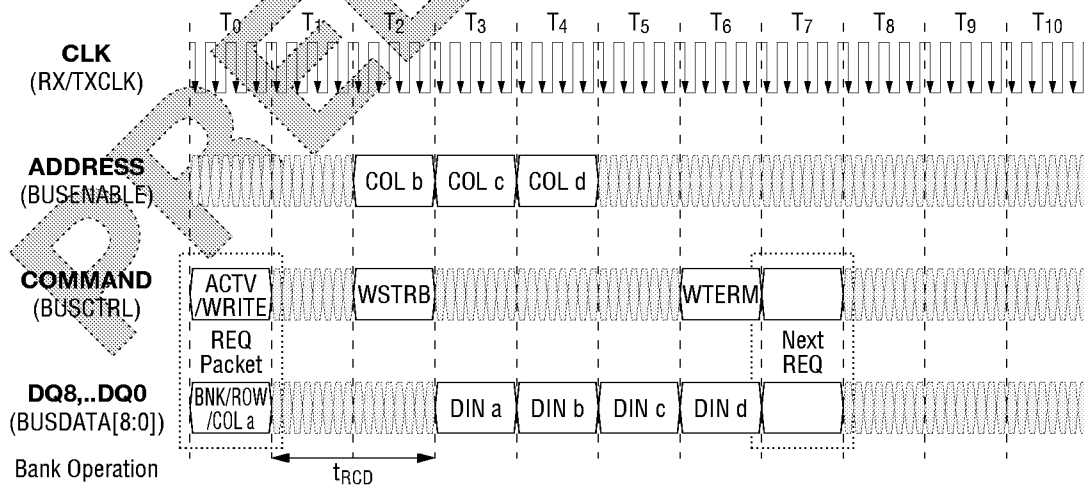
**BASIC OPERATION**

Figure 4 (a) shows an example of a read transaction. A transaction begins in interval  $T_0$  with the transfer of a REQ packet. The REQ packet contains the command (ACTV/READ), a device, bank, and row address (BNK/ROW) of the page to be activated, and the column address (COLa) of the first octbyte to be read from the page.

The selected bank performs the activation of the selected row during  $T_1$  and  $T_2$  (the  $t_{RCD}$  interval). Next, the selected bank reads the selected octbyte during  $T_3$  and  $T_4$  (the  $t_{CAC}$  interval). A second command RSTRB (read strobe) is transferred during  $T_3$  and causes the first octbyte (DOUTa) to be transferred during  $T_5$ .



**(a) BANK ACTIVATE AND RANDOM READ CYCLES WITHIN A PAGE**



**(b) BANK ACTIVATE AND RANDOM WRITE CYCLES WITHIN A PAGE**

**Fig. 4 Read and Write Transaction Examples**

In this example, three additional octbytes are read from the activated page. These column addresses (COLb, COLc, and COLd) are transferred in  $T_3$ ,  $T_4$ , and  $T_5$ , respectively. The data octbytes (DOUTb, DOUTC, and DOUTd) are transferred in  $T_5$ ,  $T_6$ , and  $T_7$ . The end of the data octbytes is signaled by a third command RTERM (read terminate) in  $T_6$ . The next REQ packet may be sent in  $T_9$ , or in any interval thereafter.

Figure 4 (b) shows an example of a write transaction. The transaction begins in interval  $T_0$  with the transfer of a REQ packet. The REQ packet contains, the command (ACTV/WRITE), a device, bank, and row address (BNK/ROW) of the page to be activated, and the column address (COLa) of the first octbyte to be written to the page.

The selected bank performs the activation of the selected row during  $T_1$  and  $T_2$  (the  $t_{RCD}$  interval). A second command WSTRB (write strobe) is transferred during  $T_2$  and causes the first octbyte (DINa) to be transferred during  $T_3$ .

In this example, three additional octbytes are written to the activated page. These column addresses (COLb, COLc, and COLd) are transferred in  $T_2$ ,  $T_3$ , and  $T_4$  respectively. The data octbytes (DINb, DINc, and DINd) are transferred in  $T_4$ ,  $T_5$ , and  $T_6$ . The end of the data octbytes is signaled by a third command WTERM (write termination) in  $T_6$ . The next REQ packet may be sent in  $T_7$ , or in any interval thereafter.

## INTERLEAVED TRANSACTIONS

The previous examples showed noninterleaved transactions - the next REQ packet was transferred *after* the last data octbyte of the current transaction. In an interleaved transaction, the next REQ packet is transferred *before* the first data octbyte of the current transaction. This permits the row and column access intervals of the next transaction to overlap the data transfer of the current transaction.

Figure 5 shows an example of interleaved read transactions. The first transaction proceeds exactly as the noninterleaved example of Figure 4(a) (all packets of the first transaction are labeled with "1"). However, in  $T_5$  the REQ packet for the second transaction is transferred (all packets of the second transaction are labeled with "2"). The  $t_{RCD2}$  and  $t_{CAC2}$  intervals overlap the transfer of DOUT1 data octbytes and thus increase the effective bandwidth of the RDRAM since there are no unused intervals.

A transaction consists of an address transfer phase and a data transfer phase. The REQ packet performs address transfer, and the remaining packets perform data transfer (DOUT, COL, RSTRB, and RTERM in the case of a read transaction). The time interval between the address and data transfer phases of the current transaction may be adjusted to match the data length of the previous transaction (as long as the row and column access times for the current transaction are observed). Thus, there are no limits on the types of memory transaction which may be interleaved; any mixing of transaction length and command type is permitted.



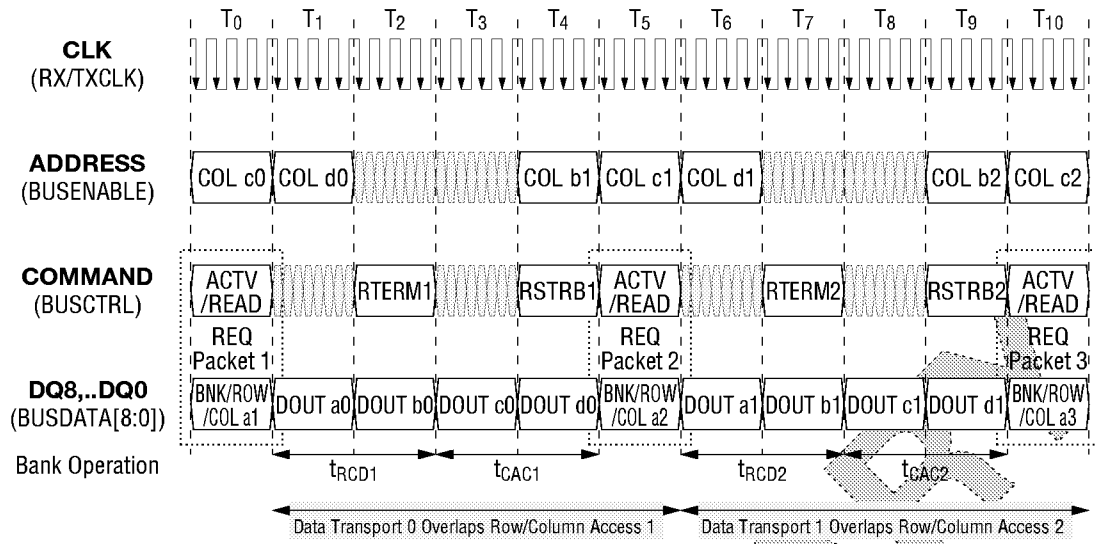


Fig. 5 Interleaved Read Transaction Example

PRELIMINARY

## REQ PACKET (ADDRESS TRANSFER)

An REQ packet initiates a transaction by transferring the address and command information to the RDRAM. Figure 6 shows the format of the REQ packet. Note that each RDRAM wire carries eight bits of information in each  $t_{\text{PACKET}}$ . This is the time required to transfer an octabyte of data and is the natural granularity with which to illustrate timing relationships. The clock that is actually used by the RDRAM has a period of  $t_{\text{CYCLE}}$ , with information transferred on each clock edge.  $t_{\text{PACKET}}$  is four times  $t_{\text{CYCLE}}$ .

In the REQ packet, the bits which are gray are reserved, and should be driven with a zero. In particular, the bits in  $t_{\text{CYCLE}} t_6$  and  $t_7$  are needed for bus-turn-around during read transactions.

**A35..A3:** The address field A35..A3 consumes the greatest number of bits. These are allocated to device, bank, row, and column addressing according to Table 3:

**Table 3 A35..A3 Address Fields**

Field	16M/18M (2KB Page)	64M (2KB Page)
COL	A10..A3	A10..A3
ROW	A19..A11	A20..A11
BNK	A20	A22, A21
DEV	A35..A21	A35..A23

**OP5..OP0:** The command field OP5..OP0 specifies the type of transaction that is to be performed, according to Table 4. The OP0 bit selects a read or write transaction, the OP1 bit selects a memory or register space access, and OP5..OP2 select command options. These command options include B in OP2 (see byte masking on page 22), D in OP3 for selecting broadcast operations (see refresh on page 35), and b1, b0 in OP5, OP4 (see bit masking on page 23).

**ACTV:** This bit specifies activation or precharge/activation of a bank at the beginning of a transaction, and is designated by prepending "ACTV/" or "PRE/ACTV/" to the command.

**AUTO:** This bit specifies auto-precharge of a bank at the end of the transaction, and is designated by appending "A" to the command.

**START:** This bit is always set to a one and indicates the beginning of a request to the RDRAM.

**REGSEL:** This bit is used for accessing registers.

**PEND2...PEND0:** This field is set to "000" for noninterleaved transactions, and to a nonzero value for interleaved transactions. This is the number of previous STRB and TERM packets the RDRAM is to skip. Refer to the *Concurrent RDRAM Design Guide* for further details.

**M7..M0:** This field is used to perform byte masking of the first data octabyte  $DINa$  for all memory write transactions (OP1, OP0 = 01). Refer to byte masking on page 22.

Table 4 Command Encoding

ACTV	AUTO	OP5	OP4	OP3	OP2	OP1	OP0	Command	Description
0	0	0	0	0	X	0	0	READ	Read
0	0	b1	b0	D	B	0	1	WRITE	Write (b1, b0, B masking and D broadcast options)
0	0	0	0	0	1	1	0	RREG	Register Read
0	0	0	0	D	1	1	1	WREG	Register Write (D)
0	1	0	0	0	X	0	0	READA	Read/AutoPrecharge
0	1	b1	b0	D	B	0	1	WRITEA	Write/AutoPrecharge (b1, b0, D, B)
1	0	0	0	0	X	0	0	ACTV/READ	Activate/Read
1	0	b1	b0	D	B	0	1	ACTV/WRITE	Activate/Write (b1, b0, D, B)
1	1	0	0	0	X	0	0	ACTV/READA	Activate/Read/AutoPrecharge
1	1	b1	b0	D	B	0	1	ACTV/WRITEA	Activate/Write/AutoPrecharge (b1, b0, D, B)
1	0	0	0	0	X	0	0	PRE/ACTV/READ	Precharge/Activate/Read
1	0	b1	b0	D	B	0	1	PRE/ACTV/WRITE	Precharge/Activate/Write (b1, b0, D, B)
1	1	0	0	0	X	0	0	PRE/ACTV/READA	Precharge/Activate/Read/AutoPrecharge
1	1	b1	b0	D	B	0	1	PRE/ACTV/WRITEA	Precharge/Activate/Write/AutoPrecharge (b1, b0, D, B)

PRELIMINARY

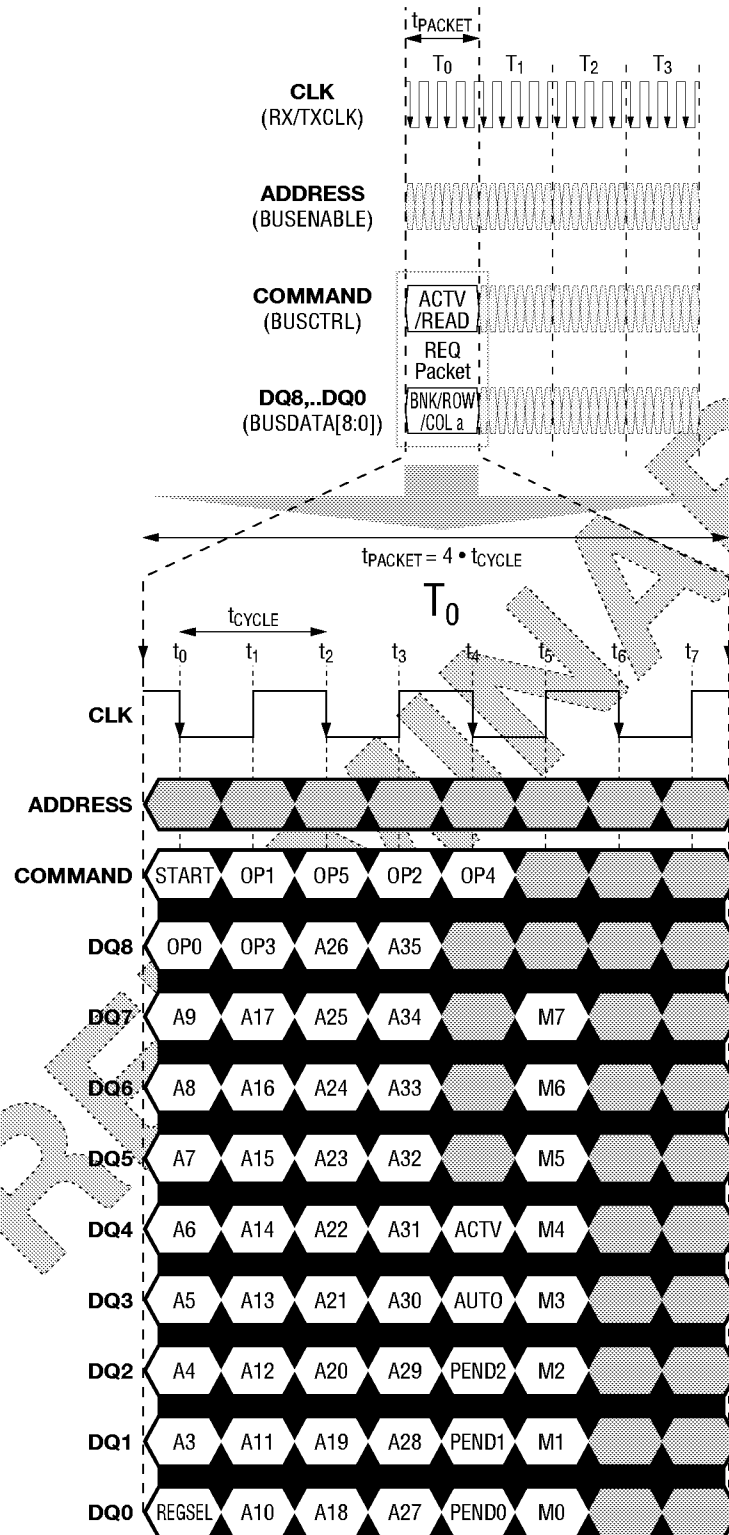


Fig. 6 REQ Packet Format

## DATA TRANSFER PACKETS

The next set of packet types are used for data transfer. Their formats are summarized in Figure 7.

As in the REQ packet, eight bits are transferred on each wire during each  $t_{\text{PACKET}}$  interval. The rising and falling edges of the RDRAM clock define the transfer windows for each of these bits. The data transfer packets will align to the  $t_{\text{PACKET}}$  intervals defined by the START bit of the REQ packet by simply observing the timing rules that are developed in the next few sections of this document.

### DIN and DOUT Packets

There are nine wires allocated for the data bytes. These wires are labeled DQ8..DQ0. The eight bytes transferred in a DIN or DOUT packet have 72 bits, which are labeled D0..D63 (on the DQ0..DQ7 wires) and E0..E7 (on the DQ8 wire). The 18Mbit RDRAM have storage cells for the E0..E7 bits. The E0..E7 bits are also used with byte masking operations. This is described in the section on byte masking on page 22.

### COL Packet

The column address A10..A3 of the first octbyte of data (DINA or DOUTa) is provided in the REQ packet. The COL packet contains an eight bit field A10..A3, which provides the column address for the second and subsequent data octbytes. The COL packets have a fixed timing relationship with respect to the DIN and DOUT packets to which they correspond. As the DIN and DOUT packets are moved (to accommodate interleaving), the COL packets move with them.

### RSTRB and RTERM Packets

The RSTRB and RTERM packets indicate the beginning and end of the DOUT packets that are transferred during a read transaction. The RSTRB and RTERM packets are each eight bits and consist of a single "1" in an odd  $t_{\text{CYCLE}}$  position, with the other seven positions "0". Note that when a transaction transfers a single data octbyte, the RSTRB and RTERM packets will overlay one another. This is permitted and is in fact the reason that each packet consists of a single asserted bit. An example of this case is shown in Figure 14 (a). There will be transaction situations in which the RTERM overlays a REQ packet (two octbyte interleaved transaction). Again, this is permitted. The general rule is that the RTERM may overlay any of the other packets on the Command (BUSCTRL) wire, and RSTRB may overlay any other except for a REQ packet.

### WSTRB and WTERM Packets

TheWSTRB and WTERM packets indicate the beginning and end of the series of DIN packets that are transferred during a write transaction. TheWSTRB and WTERM packets are each eight bits and consist of a single "1" in an odd  $t_{\text{CYCLE}}$  position, with the other seven positions "0". Note that when a transaction transfers a single data octbyte, theWSTRB and WTERM packets will not overlay one another (unlike the case of a one octbyte read). An example of this case is shown in Figure 14 (b). There will be transaction situations in which theWSTRB overlays a REQ packet (no bank activate). Again, this is permitted. An example of this is shown in Figure 9 (a). The general rule is that theWSTRB may overlay any of the other packets on the Command (BUSCTRL) wire, and WTERM may overlay any other except for a REQ packet.

## CKE PACKET

The average power of the RDRAM can be reduced by using Suspend power mode. This is done by setting the FR field of the MODE register to a zero (the MODE register is shown in Figure 17). A CKE packet must be sent a time  $t_{CKE}$  ahead of each REQ packet (this is shown in interval  $T_0$  in Figure 21 (b)). This causes the RDRAM to transition from Suspend to Enable mode. When the RDRAM has finished the transaction, it returns to Suspend mode. The CKE packet will overlay the RSTRB and RTERM packets when transactions are interleaved. If the FR field is set to a one, CKE packets are not used and the RDRAM remains in Enable mode.

## RESET PACKET

The RESET packet is used during initialization. When RESET packets are driven for a time  $t_{RESET}$  or greater, the RDRAM will assume a known state. Because the RESET packet is limited to this one use, it will not interact with the other packet types. This is illustrated in Figure 21 (a).

## PWRUP PACKET

The PWRUP packet is used to cause an RDRAM to transition from Powerdown to Enable mode. This is illustrated in Figure 21 (c).

PRELIMINARY

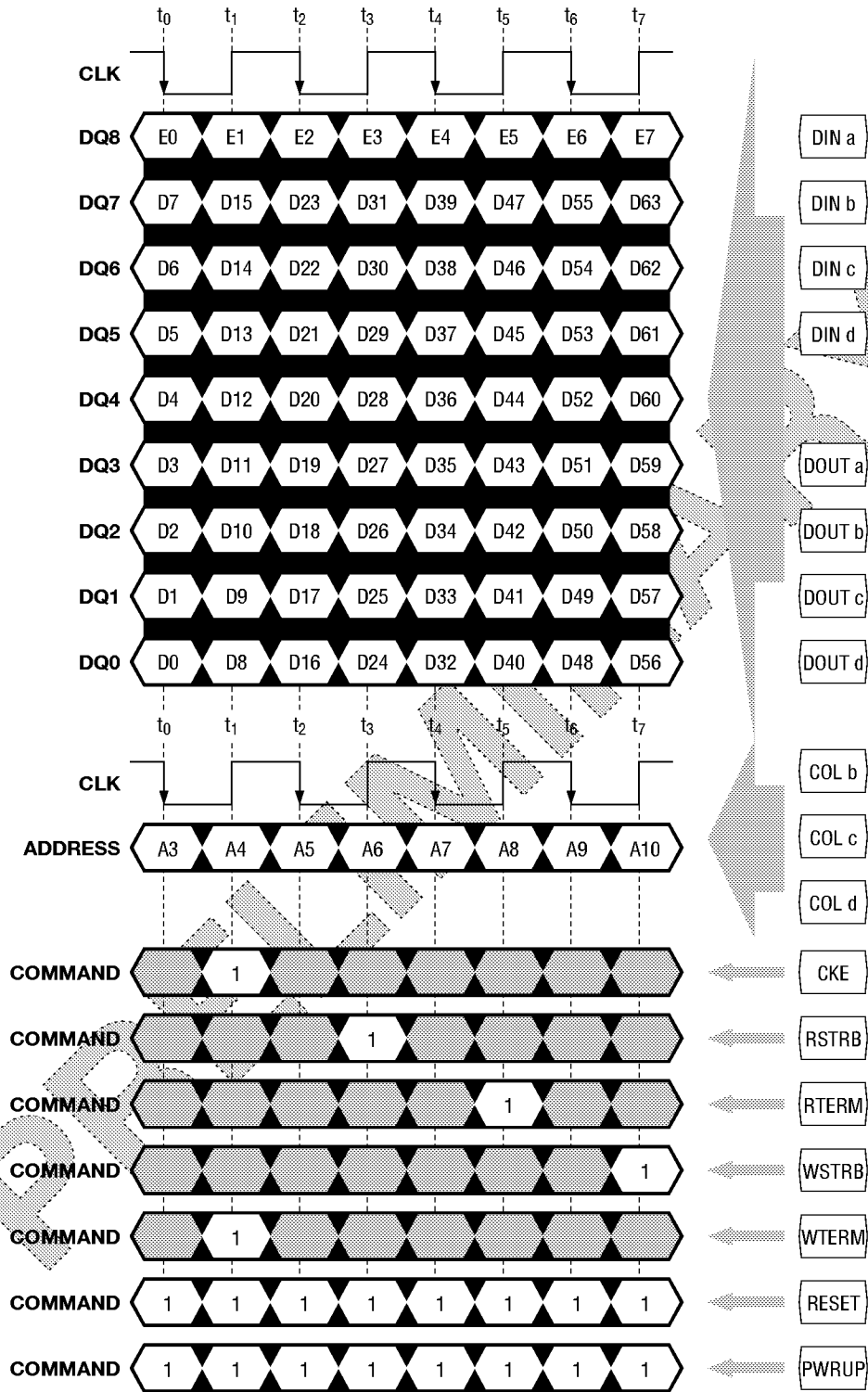


Fig. 7 DIN, DOUT, COL, CKE, RSTRB, RTERM, WSTRB, WTERM, and RESET Packet Formats

## READ TRANSACTIONS

When a controller issues a read request to an RDRAM, one of three transaction cases will occur. This is a function of the request address and the state of the RDRAM.

**READ:** The first case is shown in Figure 8 (a). This occurs when the requested bank has been left in an activated state and the requested row address matches the address of this activated row. This is also called a page hit read and is invoked by the READ or READA commands.

There are three timing parameters which specify the positioning of the packets which control the data transfer. These are as follows:

$t_{SDR}$	Start of RSTRB to start of DOUT
$t_{CDR}$	Start of COL to start of DOUT
$t_{TDR}$	Start of RTERM to end of DOUT

These parameters are all expressed in units of  $t_{CYCLE}$ , and the minimum and maximum values are the same; the RSTRB, RTERM, COL, and DOUT packets move together as a block.

A fourth parameter has a minimum value only, and positions the block of data transfer packets relative to the REQ (address transfer) packet:

$t_{RSR}$	Start of REQ to start of RSTRB for READ
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When a read transaction is formed, these packet constraints must be observed. In addition, there are constraints upon the timing of the bank operations which must also be observed. These are shown in Figure 8 (a) next to the label "Bank Operation". After the transfer of the REQ packet in  $T_0$ , the RDRAM performs a column access (requiring  $t_{CAC}$  for the column access time) of the first data octbyte DOUTa during  $T_1$  and  $T_2$ . The RDRAM performs three column cycles (requiring  $t_{CC}$  for the column cycle time) in order to access the next three data octbytes (DOUTb, DOUTc, DOUTd) during  $T_3$ ,  $T_4$  and  $T_5$ . Each data octbyte is transferred one  $t_{PACKET}$  interval after it is accessed.

**ACTV/READ:** The second case is shown in Figure 8 (b). This occurs when the requested bank has been left in a precharged state. This is invoked by the ACTV/READ and ACTV/READA commands.

The RSTRB, RTERM, COL, and DOUT packets remain in the same relative positions as in the READ case, but they move further from the REQ packet:

$t_{ASR}$	Start of REQ to start of RSTRB for ACTV/READ
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After the transfer of the REQ packet in  $T_0$ , the RDRAM performs an activation operation (requiring  $t_{RCD}$  for the row-column delay) during  $T_1$  and  $T_2$ . This leaves the requested row activated. From this point the sequence of bank operations are identical to the READ case, except that everything has shifted two  $t_{PACKET}$  intervals further from the REQ packet. The sum of  $t_{RCD}$  and  $t_{CAC}$  is also known as  $t_{RAC}$  (the row access time).



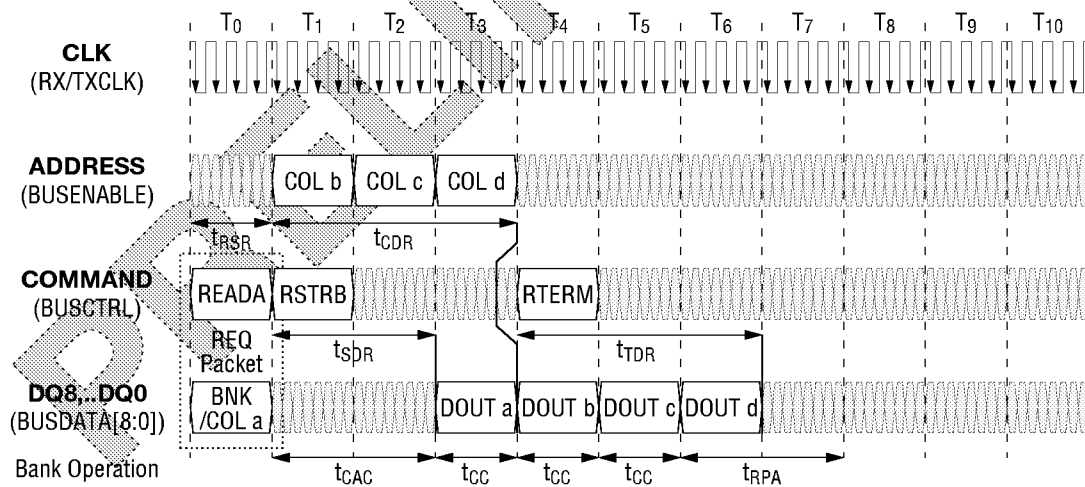
**PRE/ACTV/READ:** The third case is shown in Figure 8 (c). This occurs when the requested bank has been left in an activated state and the requested row address doesn't match the address of this activated row. This is also called a page miss read and is invoked by the PRE/ACTV/READ and PRE/ACTV/READA commands. The RDRAM knows the difference between a PRE/ACTV/READ and a ACTV/READ because each RDRAM bank has a flag indicating whether it is precharged or activated. The external controller tracks this flag, and also tracks the address of each activated bank in order to distinguish READ and PRE/ACTV/READ accesses.

The RSTRB, RTERM, COL, and DOUT packets remain in the same relative positions as in the READ case, but they move further from the REQ packet:

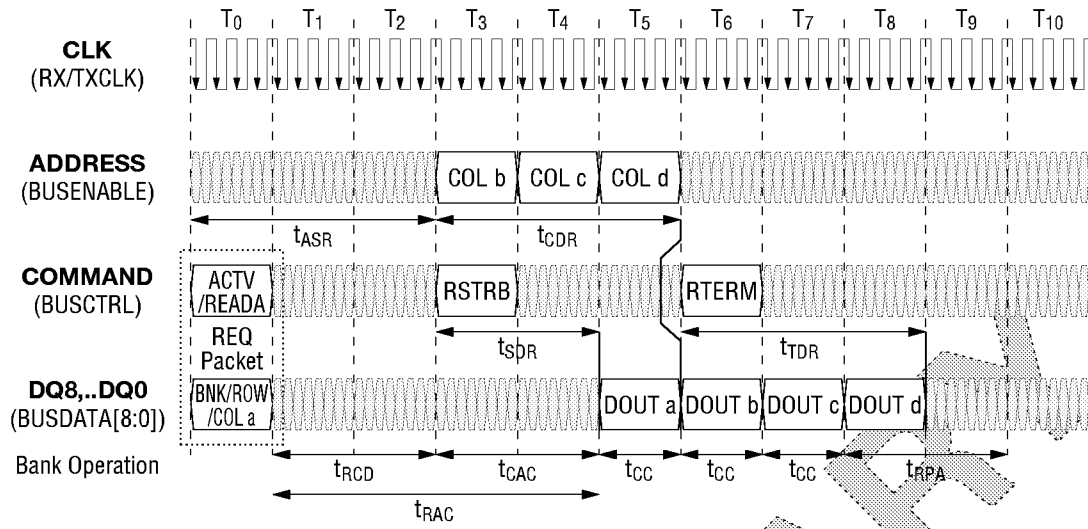
$t_{PSR}$  Start of REQ to start of RSTRB for PRE/ACTV/READ

After the transfer of the REQ packet in  $T_0$ , the RDRAM performs a precharge operation ( $t_{RP}$ ) during  $T_1$  and  $T_2$ , and an activation operation ( $t_{RCD}$ ) during  $T_3$  and  $T_4$ . This leaves the requested row activated. From this point the sequence of bank operations are identical to the READ case, except that everything has shifted four  $t_{PACKET}$  intervals further from the REQ packet. The sum of  $t_{RP}$ ,  $t_{RCD}$ , and  $t_{CAC}$  is also known as  $t_{RC}$  (the row cycle time).

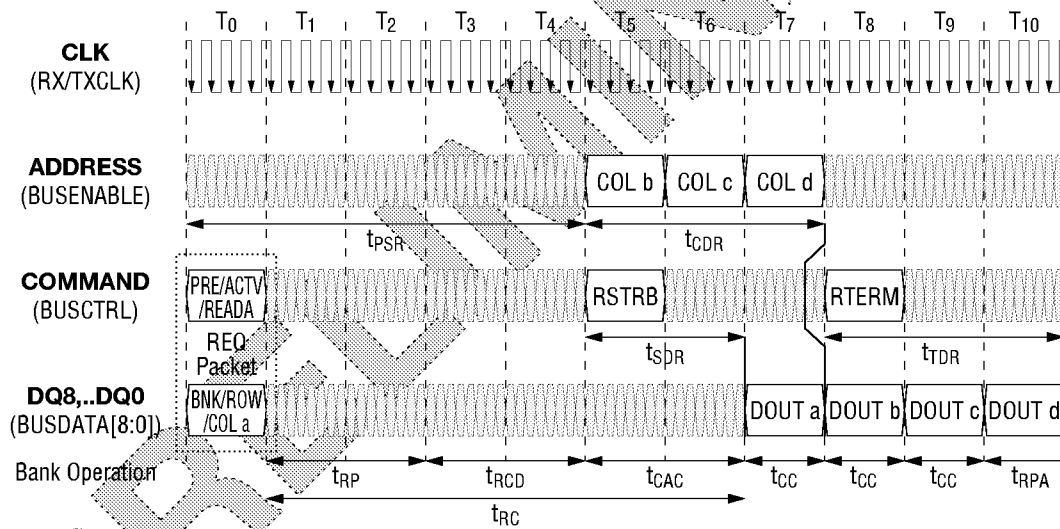
**Auto-Precharge Option:** For a READ, ACTV/READ, or a PRE/ACTV/READ command, the bank operations are complete once the last data octbyte has been accessed. The bank will be left with the requested row activated. For a READA, ACTV/READA, or a PRE/ACTV/READA command, there is an additional step. During the two  $t_{PACKET}$  intervals after the last data octbyte access, an auto-precharge operation (requiring  $t_{RPA}$  for the row precharge, auto) is performed. This leaves the bank in a precharged state.



(a) READA - RANDOM READ CYCLES WITHIN A PAGE



(b) ACTV/READA - BANK ACTIVATE AND RANDOM READ CYCLES WITHIN A PAGE



(c) PRE/ACTV/READA - BANK PRECHARGE/ACTIVATE AND RANDOM READ CYCLES IN A PAGE

Fig. 8 Read Transactions

## WRITE TRANSACTIONS

When a controller issues a write request to an RDRAM, one of three transaction cases will occur. This is a function of the request address and the state of the RDRAM.

**WRITE:** The first case is shown in Figure 9 (a). This occurs when the requested bank has been left in an activated state and the requested row address matches the address of this activated row. This is called a page hit write and is invoked by the WRITE or WRITEA commands.

There are three timing parameters which specify the positioning of the packets which control the data transfer. These are as follows:

$t_{SDW}$	Start of WSTRB to start of DIN
$t_{CDW}$	Start of COL to start of DIN
$t_{TDW}$	Start of WTERM to end of DIN

These parameters are all expressed in units of  $t_{CYCLE}$ , and the minimum and maximum values are the same; the WSTRB, WTERM, COL, and DIN packets move together as a block.

A fourth parameter has a minimum value only, and positions the block of data transfer packets relative to the REQ (address transfer) packet:

$t_{WSW}$	Start of REQ to start of WSTRB for WRITE
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When a write transaction is formed, these packet constraints must be observed. In addition, there are constraints upon the timing of the bank operations which must also be observed. These are shown in Figure 9 (a) next to the label "Bank Operation". After the transfer of the REQ packet in  $T_0$ , the RDRAM performs a column access (requiring  $t_{CAC}$  for the column access time) of the first data octbyte DINa during  $T_1$  and  $T_2$ . The RDRAM performs three column cycles (requiring  $t_{CC}$  for the column cycle time) in order to access the next three data octbytes (DINb, DINc, DINd) during  $T_3$ ,  $T_4$  and  $T_5$ . Each data octbyte is transferred one  $t_{PACKET}$  interval before it is accessed.

**ACTV/WRITE:** The second case is shown in Figure 9 (b). This occurs when the requested bank has been left in a precharged state. This is invoked by the ACTV/WRITE and ACTV/WRITEA commands.

The WSTRB, WTERM, COL, and DIN packets remain in the same relative positions as in the page hit case, but they move further from the REQ packet:

$t_{ASW}$	Start of REQ to start of WSTRB for ACTV/WRITE
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After the transfer of the REQ packet in  $T_0$ , the RDRAM performs an activation operation (called  $t_{RCD}$  or row-column delay) during  $T_1$  and  $T_2$ . This leaves the requested row activated. From this point the sequence of bank operations are identical to the WRITE case, except that everything has shifted two  $t_{PACKET}$  intervals further from the REQ packet. The sum of  $t_{RCD}$  and  $t_{CAC}$  is also known as  $t_{RAC}$  (the row access time).

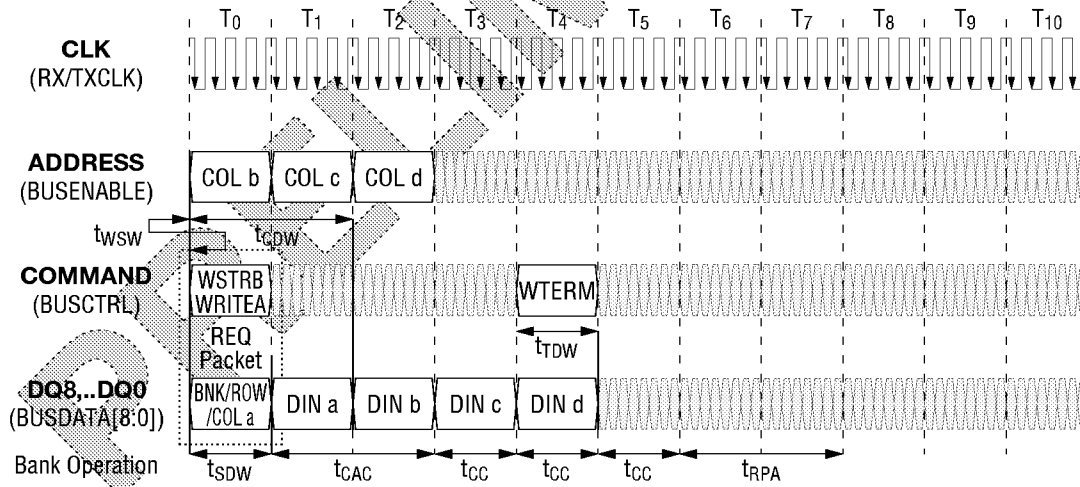
**PRE/ACTV/WRITE:** The third case is shown in Figure 9 (c). This occurs when the requested bank has been left in an activated state and the requested row address doesn't match the address of this activated row. This is also called a page miss write and is invoked by the PRE/ACTV/WRITE and PRE/ACTV/WRITEA commands. The RDRAM knows the difference between a PRE/ACTV/WRITE and a ACTV/WRITE because each RDRAM bank has a flag indicating whether it is precharged or activated. The external controller tracks this flag, and also tracks the address of each activated bank in order to distinguish PRE/ACTV/WRITE and WRITE accesses.

The WSTRB, WTERM, COL, and DIN packets remain in the same relative positions as in the WRITE case, but they move further from the REQ packet:

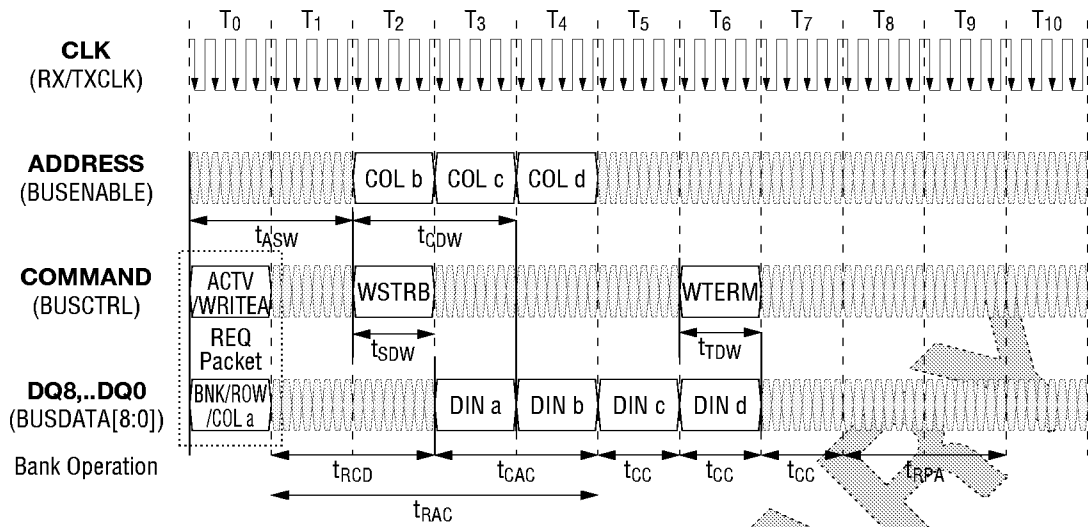
$t_{PSW}$  Start of REQ to start of WSTRB for PRE/ACTV/WRITE

After the transfer of the REQ packet in  $T_0$ , the RDRAM performs a precharge operation ( $t_{RP}$ ) during  $T_1$  and  $T_2$ , and an activation operation ( $t_{RCD}$ ) of during  $T_3$  and  $T_4$ . This leaves the requested row activated. From this point the sequence of bank operations are identical to the WRITE case, except that everything has shifted four  $t_{PACKET}$  intervals further from the REQ packet. The sum of  $t_{RP}$ ,  $t_{RCD}$ , and  $t_{CAC}$  is also known as  $t_{RC}$  (the row cycle time).

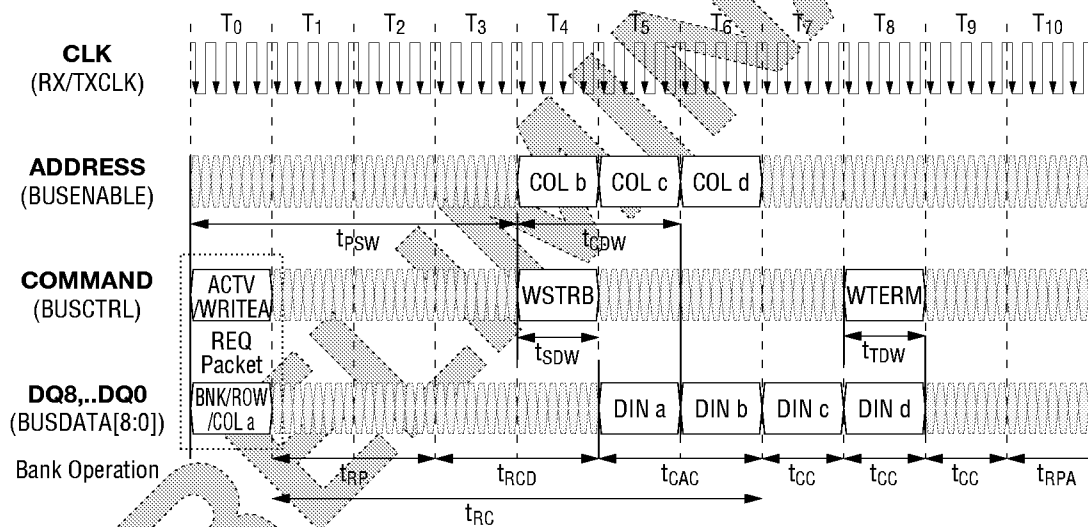
**Auto-Precharge Option:** For a WRITE, ACTV/WRITE or a PRE/ACTV/WRITE command, the bank operations are complete once the last data octbyte has been accessed. The bank will be left with the requested row activated. For a WRITEA, ACTV/WRITEA or a PRE/ACTV/WRITEA command, there is an additional step. During the two  $t_{PACKET}$  intervals after the last data octbyte access an auto-precharge operation (requiring  $t_{RPA}$  for the row precharge; auto) is performed. This leaves the bank in a precharged state.



(a) WRITEA - RANDOM WRITE CYCLES WITHIN A PAGE



(b) ACTV/WRITEA - BANK ACTIVATE AND RANDOM WRITE CYCLES WITHIN A PAGE



(c) PRE/ACTV/WRITEA - BANK PRECHARGE/ACTIVATE AND RANDOM WRITE CYCLES IN A PAGE

Fig. 9 Write Transactions

## BYTEMASK OPERATIONS

All memory write transactions ( $OP1, OP0 = 01$ ) use the  $M7..M0$  field of the REQ packet to control byte masking of the first octbyte  $DINa$  of write data.  $M7$  controls bits  $D56..D63, E7$  while  $M0$  controls bits  $D0..D7, E0$ . A "0" means don't write and a "1" means write.

The  $M7..M0$  field should be filled with "00000000" for non-memory-write transactions.

**OP2 = 1:** When  $OP2 = 1$  for a memory write transaction, the remaining data octbytes ( $DINb, DINc, \dots$ ) are written unconditionally (all bytes are written).

**OP2 = 0:** When  $OP2 = 0$ , the remaining data octbytes ( $DINb, DINc, \dots$ ) are written with a bytemask. Each bytemask is carried on the  $DQ8$  wire, pipelined one  $t_{PACKET}$  interval ahead of the data octbyte it controls.

Figure 12 (b) shows the format of the M packet and DIN packet when  $OP2 = 0$ .  $M7$  controls bits  $D56..D63$  (of the next DIN packet) and  $M0$  controls bits  $D0..D7$  (of the next DIN packet). Figure 12 (a) summarizes the location of the M packets and the DIN packets they control.

When 16M and 64M RDRAMs are used, there is no limitation caused by the use of bytemask operations; the  $DQ8$  wire is only used for the REQ packet and M packets.

When 18MRDRAM is used, there is a limitation caused by the use of bytemask operations; the  $E7..E0$  bits of the 72 bit DIN packet may not be used when  $OP2 = 0$ . To achieve bytemasking, it will be necessary to use read-modify-write operations or single-octbyte writes with the bytemask in the REQ packet and  $OP2 = 1$ .

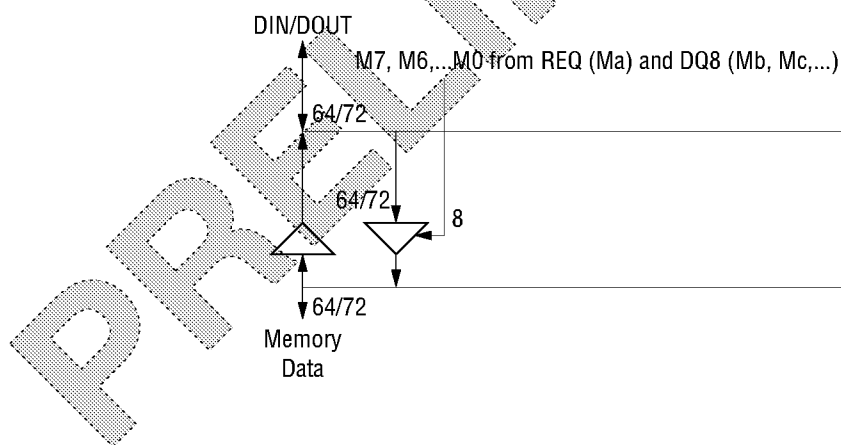


Fig. 10 Details of ByteMask Logic

**BITMASK OPERATIONS**

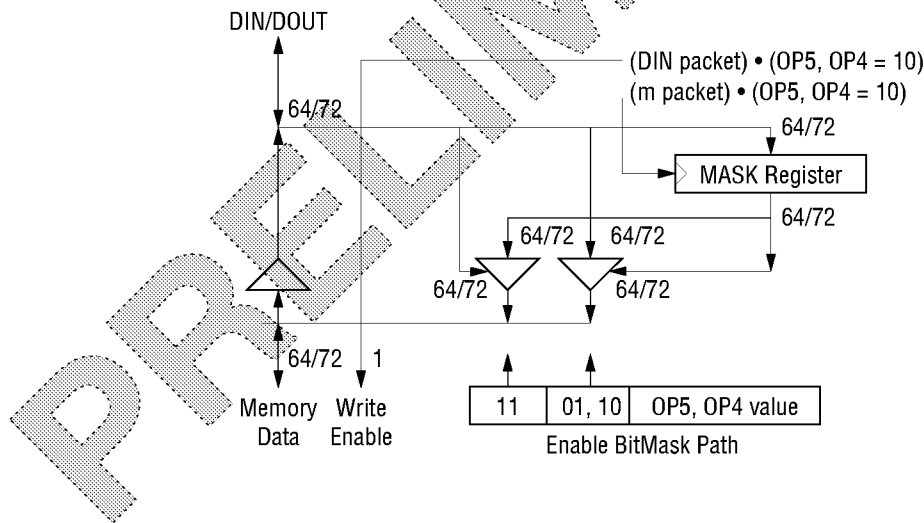
All memory write transactions (OP1,OP0 = 01) may use bitmask operations (OP5,OP4). Bitmask operations may be used simultaneously with the bytemask operations just described; a particular data bit is written only if the corresponding bytemask M and bitmask m are set.

**OP5,OP4 = 00:** This is the default option with no bitmask operation selected; all data bits are written, subject to any bytemask operation.

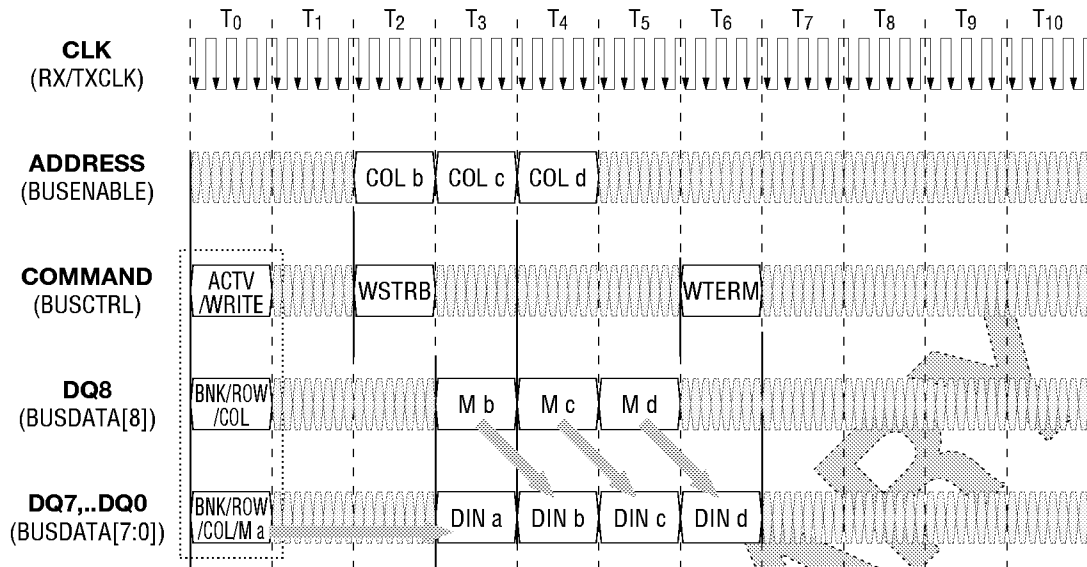
**OP5,OP4 = 01:** This is the write-per-bit option. Figure 13 (a) shows the transaction format. The 64/72-bit MASK register is used as a static bit mask, controlling whether each of the 64/72 bits of DIN octbytes is written (m = 1) or not written (m = 0). The MASK register is loaded using the dynamic bitmask operation (OP5,OP4 = 10).

**OP5,OP4 = 10:** This is the dynamic bitmask option. Figure 13 (b) shows the transaction format. Alternate octbytes (ma, mc,...) are loaded into the MASK register to be used as a bitmask for the data octbytes (DINb, DINd,...). Only the COL packets which correspond to DIN packets (COLb, COLd,...) contain a valid column address. The MASK register is left with the last bitmask that is transferred (mc in this case). The write-enable signal is asserted after DIN packet (Figure 11).

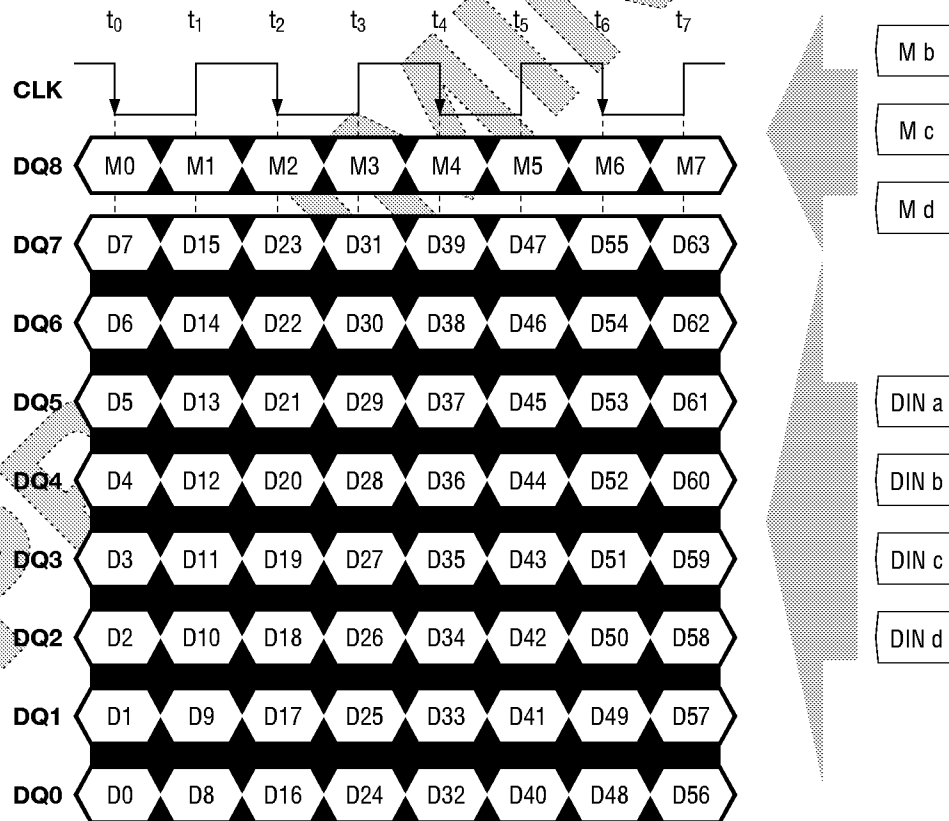
**OP5,OP4 = 11:** This is the mask-per-bit option. Figure 13 (c) shows the transaction format. The 64/72-bit MASK register is used as a static data octbyte DIN. The bitmask packets (ma, mb,...) control whether the data is written (m = 1) or not written (m = 0). The MASK register is loaded using the dynamic bitmask operation (OP5,OP4 = 10).



**Fig. 11 Details of BitMask Logic**



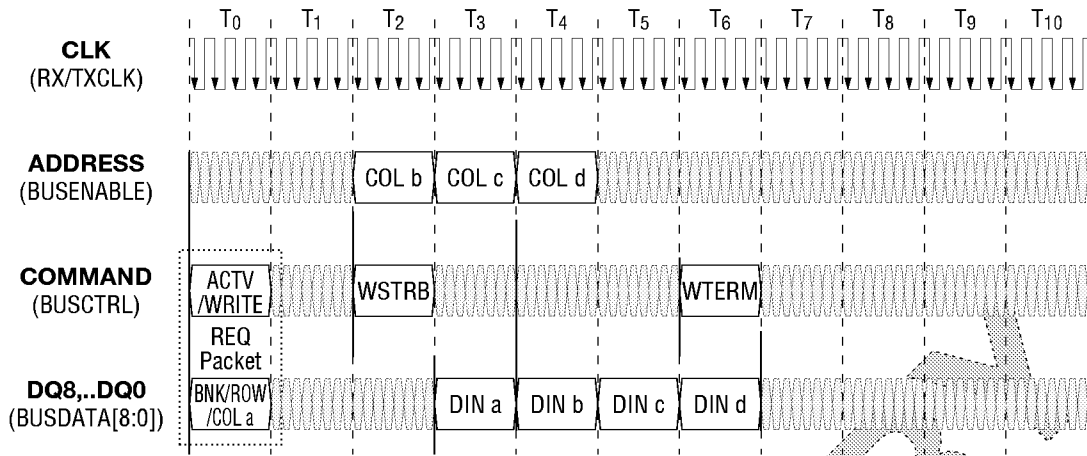
(a) OP2 = 0 - WRITE TRANSACTION WITH BYTEMASK



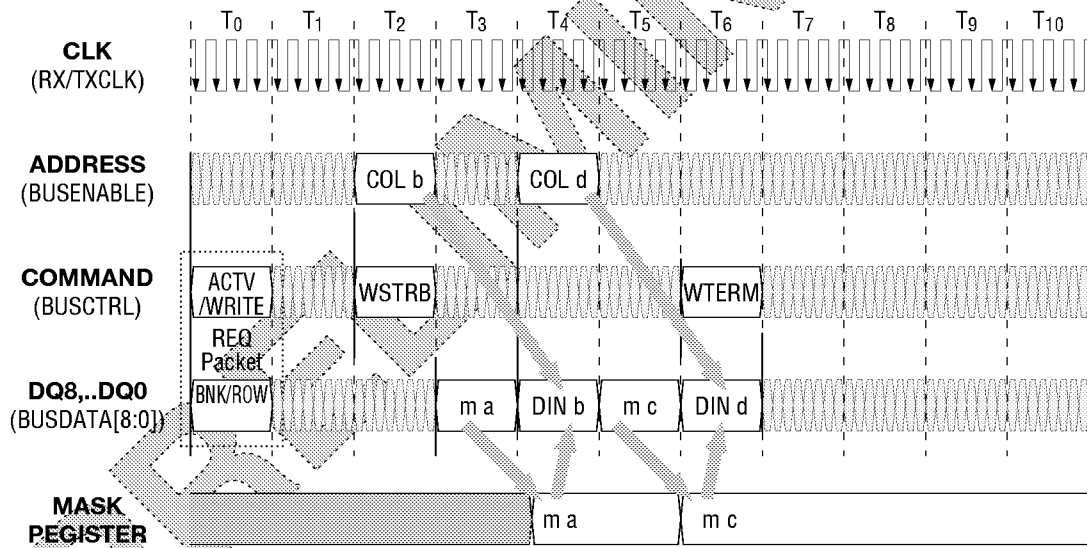
(b) OP2 = 0 - DATA AND BYTEMASK PACKET FORMATS

Fig. 12 ByteMask Operations

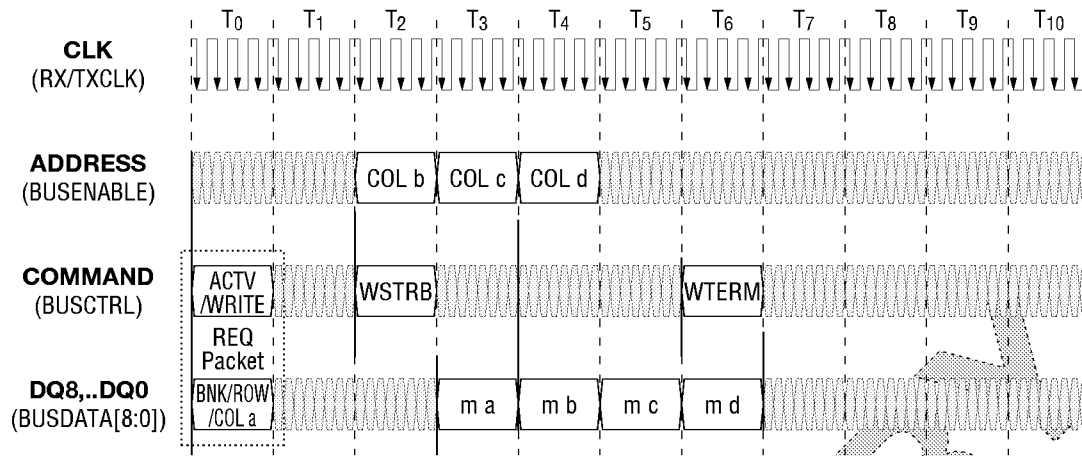




(a) OP5, OP4 = 0, 1 - BITMASK IN MASK REGISTER, DATA FROM DQ INPUTS



(b) OP5, OP4 = 1, 0 - BITMASK FROM DQ INPUTS, DATA FROM DQ INPUTS



(c) OP5, OP4 = 1, 1 - BITMASK FROM DQ INPUTS, DATA IN MASK REGISTER

Fig. 13 BitMask Operations

## REGISTERS

There are six control registers in an RDRAM. They contain read-only fields, which allow a memory controller to determine the type of RDRAM that is present. They also contain read-write fields which are used to configure the RDRAM.

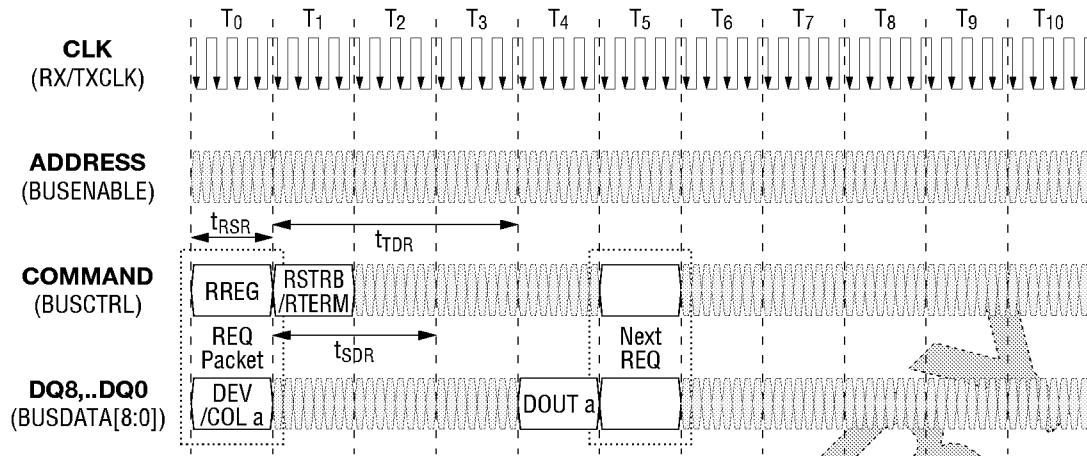
Registers are read and written with transactions that are identical to one-octbyte memory read and write transactions. These transaction formats are illustrated in Figure 14. There is one difference with respect to memory transactions; for a register write, it is necessary to allow a time of  $t_{WREG}$  to elapse before another transaction is directed to the RDRAM.

In the descriptions of some of the read-write fields, the user is instructed to set the field to a default value ("Set to 1", for example). When this is done, the suggested value is the one needed for normal operation of the RDRAM.

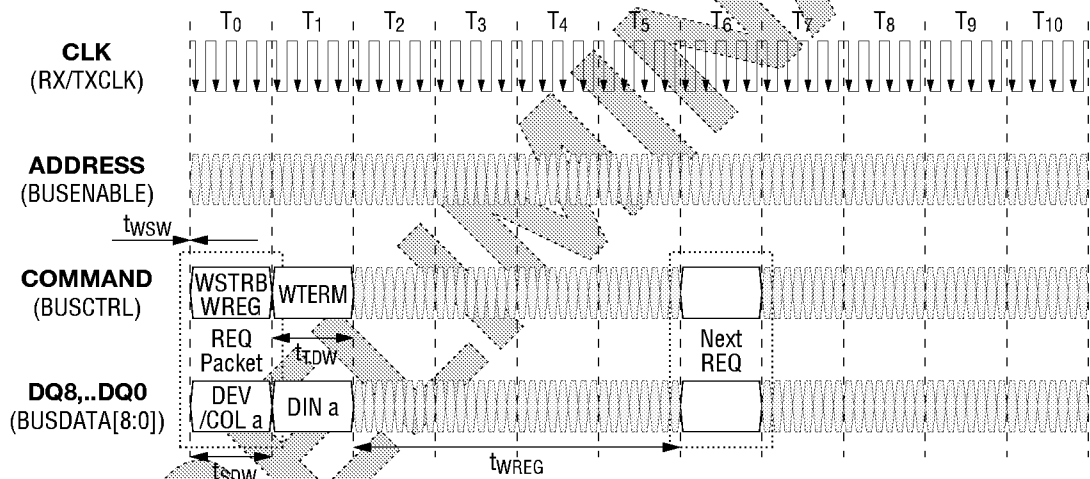
A summary of the control registers and a brief description follows

DEVICETYPE	RDRAM size, type information
DEVICEID	Set RDRAM base address
MODE	Set RDRAM operating modes
REFROW	Set refresh address for Powerdown
RASINTERVAL	Set RAS intervals
DEVICEMFGR	RDRAM manufacturer information

The control register fields are described in detail from Figure 15 to Figure 20. The format of the one octbyte DIN or DOUT packet that is written to or read from the register is shown. Gray bits are reserved, and should be written as zero. The value of the A10..A3,REGSEL field needed to access each register is also shown. The ROW and BANK address fields are not used for register read and write transactions.



(a) REGISTER READ TRANSACTION



(b) REGISTER WRITE TRANSACTION

Fig. 14 Register Transactions

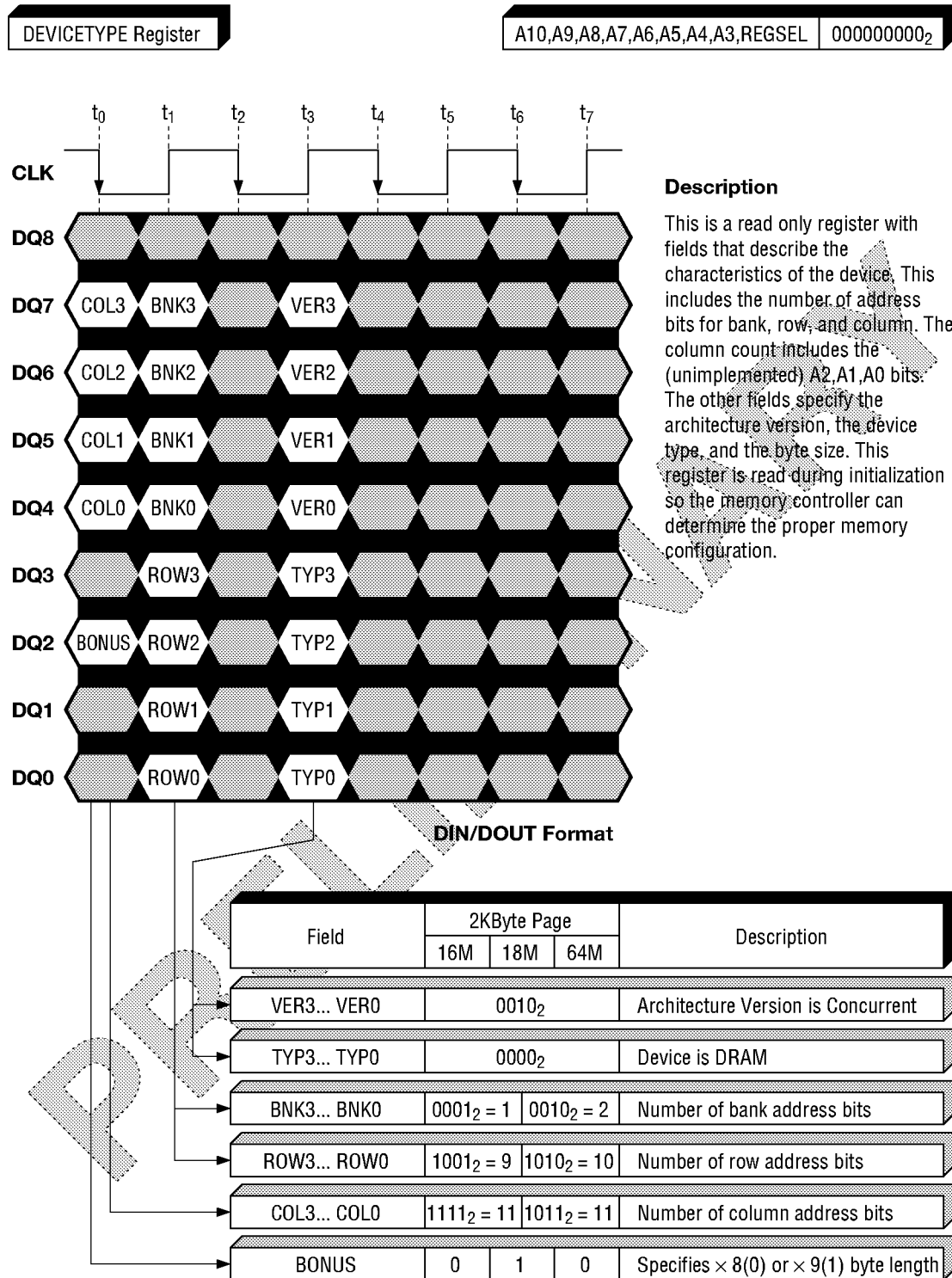


Fig. 15 DEVICETYPE Register

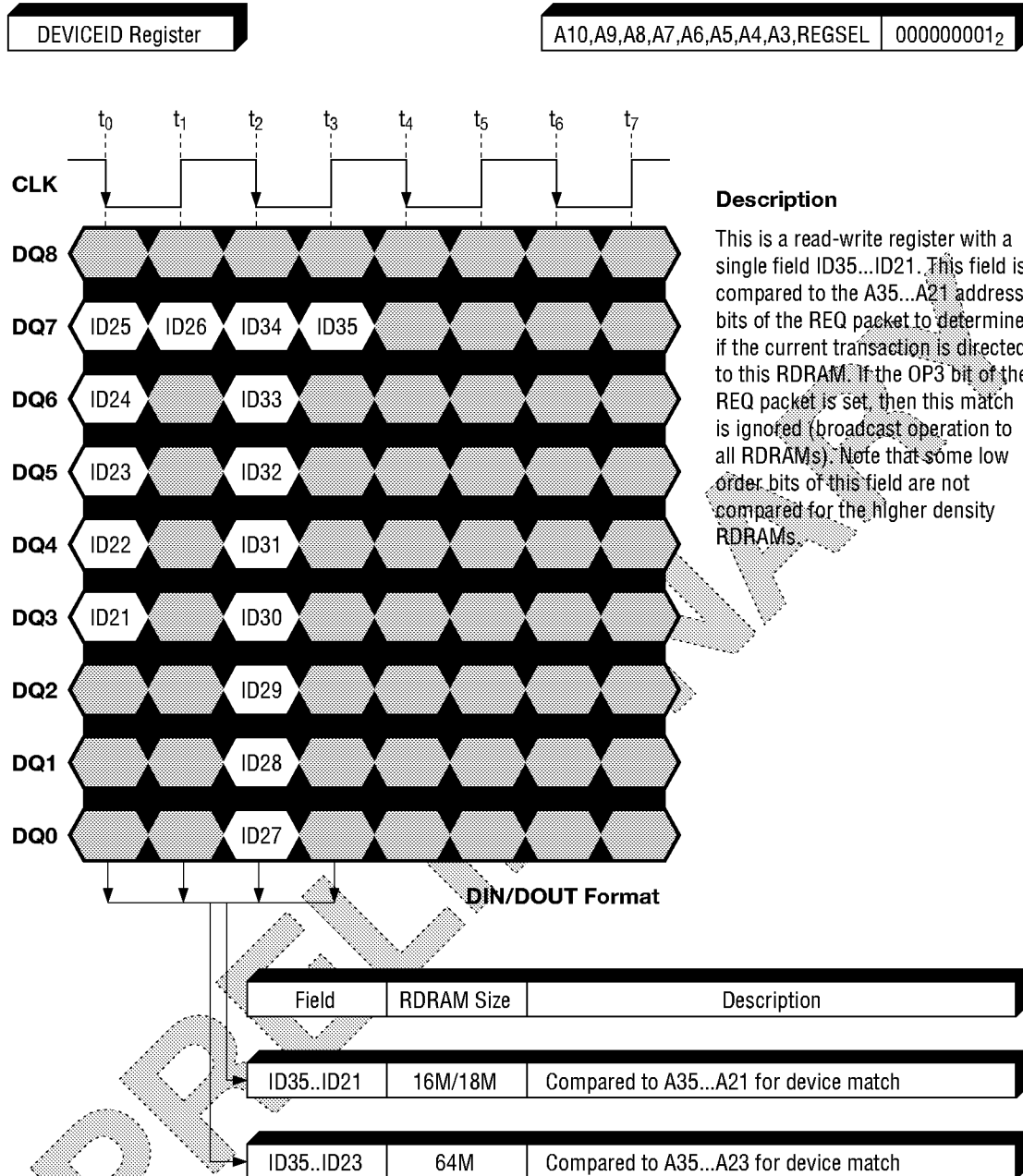


Fig. 16 DEVICEID Register

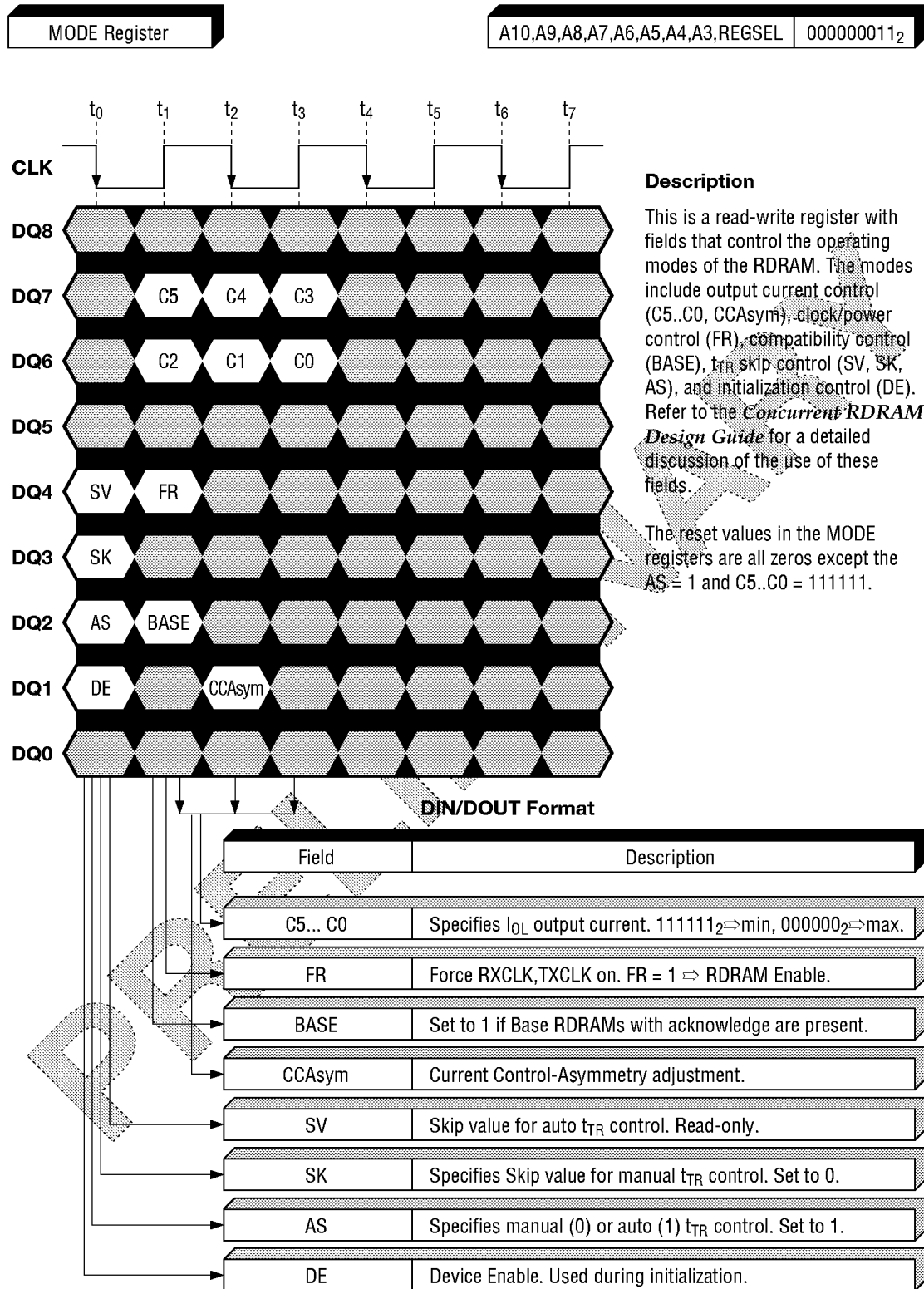


Fig. 17 MODE Register

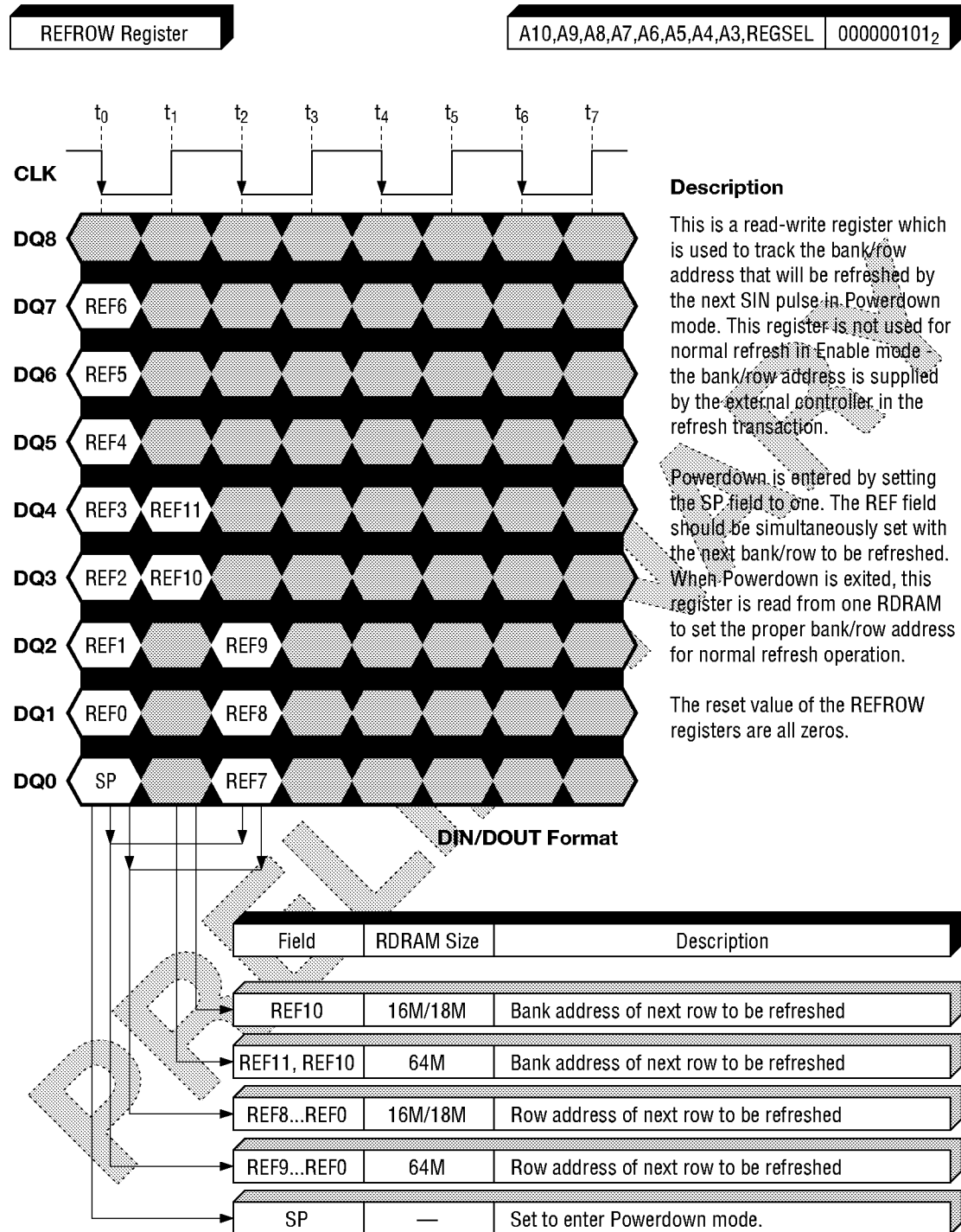


Fig. 18 REFROW Register

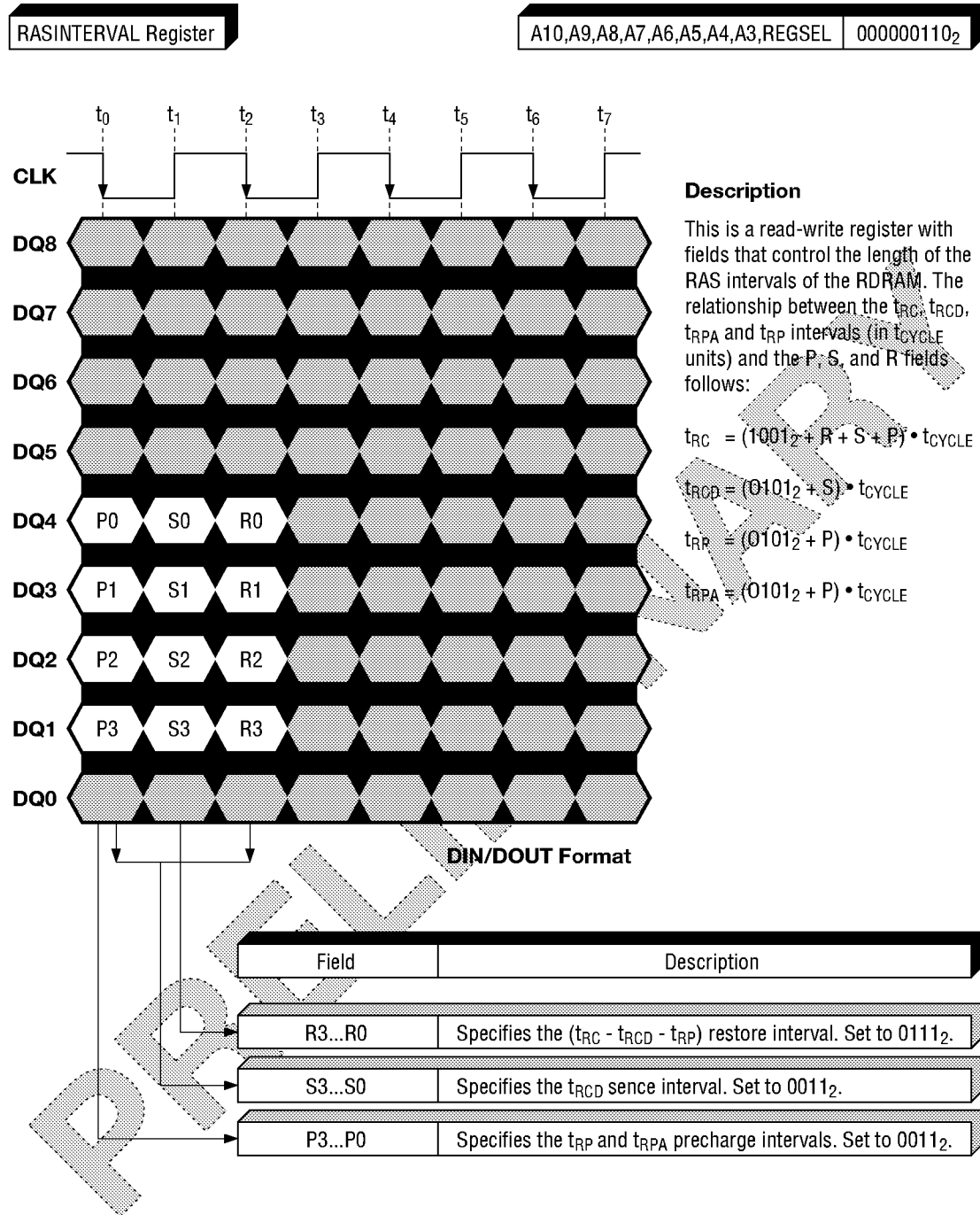


Fig. 19 RASINTERVAL Register



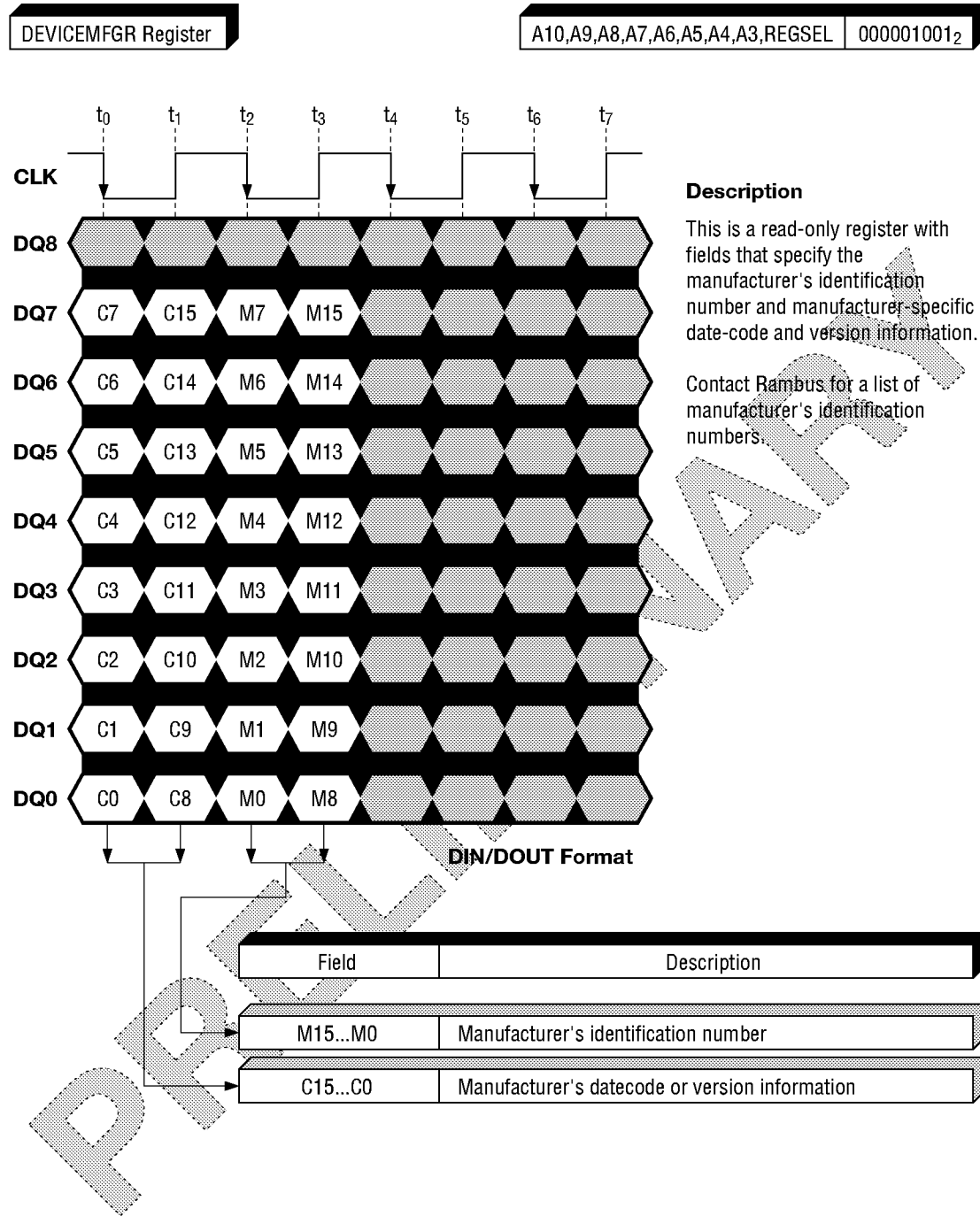


Fig. 20 DEVICEMFGR Register

## INITIALIZATION

The first step in initialization is to reset the RDRAM. This is accomplished by driving RESET packets for a time  $t_{\text{RESET}}$  or greater. This causes the RDRAM to assume a known state. This also causes the internal clocking logic (a delay-locked-loop) to begin locking to the external clock. This requires a time of  $t_{\text{LOCK}}$ . At this point, the RDRAM is ready to accept transactions. This timing sequence is shown in Figure 21 (a).

The next step for the memory controller is to read and write the six control registers, in order to determine the size and type of RDRAM that is present, and to configure it properly. A full initialization sequence is provided in the *Concurrent RDRAM Design Guide*.

## POWER MANAGEMENT

There are several power modes available in an RDRAM. These modes permit power dissipation and latency to be traded against one another.

**Enable Mode:** The simplest option is to remain permanently in Enable power mode. This is done by setting the FR field to a one in the MODE register (refer to Figure 19). The RDRAM will return to Enable mode when it is not performing a read or write transaction. This is the operating mode which has been assumed in all the transaction timing diagrams (except in Figure 21 (b)).

**Suspend Mode:** The average power can be reduced by using Suspend power mode. This is done by setting the FR field to a zero. A CKE packet must be sent a time  $t_{\text{CKE}}$  ahead of each REQ packet (this is shown in  $T_0$  in Figure 21 (b)). This causes the RDRAM to transition from Suspend to Enable mode. When the RDRAM has finished the transaction, it returns to Suspend mode. The average power of the RDRAM is reduced, but at the cost of slightly greater latency. There is no loss of effective bandwidth, since the CKE packet may be overlapped with the other packet types.

**Powerdown Mode:** The RDRAM power can be reduced to a very low level with Powerdown mode. Powerdown is entered by setting the SP field of the REFROW register to one (the REF field is simultaneously set to the next bank and row to be refreshed). As a result, most of the RDRAM's circuitry is disabled, although its memory must still be refreshed. This is accomplished by pulsing the SIN input with a cycle time of  $t_{\text{SCYCLE}}$  or less.

Powerdown mode is exited when PWRUP packets are asserted for a time  $t_{\text{PWRUP}}$  on the Command wire. The internal clocking logic will begin locking to the external clock. After a time of  $t_{\text{LOCK}}$  the RDRAM will be in Enable mode, ready for the next REQ packet. This is illustrated in Figure 21 (c).

## REFRESH

Memory refresh (when not in Powerdown) uses a one-octbyte broadcast memory write with the following REQ field values:

OP5..0	001001 <sub>2</sub>	A35..3	DEV:	0..0 (unused)
AUTO	1		BNK:	next bank
ACTV	1		ROW:	next row
PEND	000/001/010		COL:	0..0 (unused)
M7..0	0000000 <sub>2</sub>	REGSEL:	0	

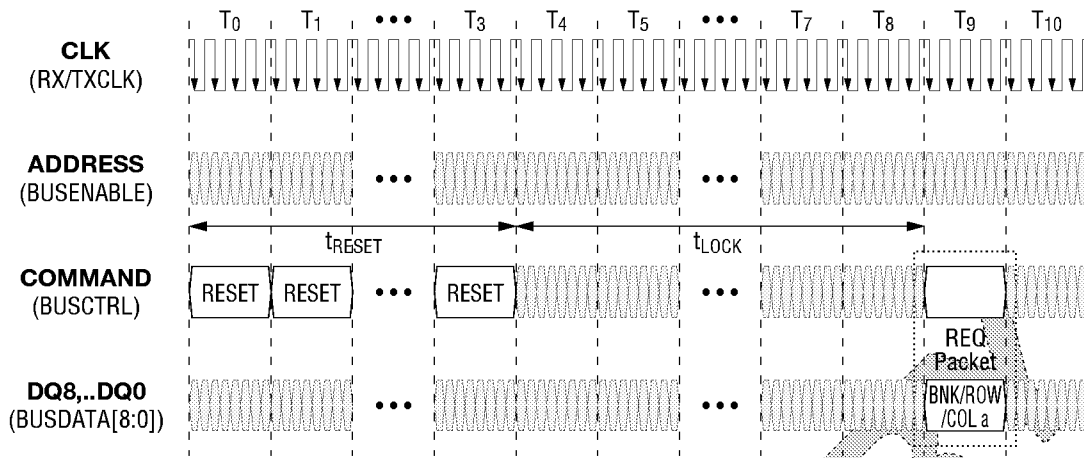
The transaction format for memory refresh is shown in Figure 22 (a). The transaction may be noninterleaved or interleaved (if interleaved, the PEND field must be properly filled). The transaction causes the requested row of the requested bank of *all* RDRAMs to be activated and then auto-precharged (note that the interval  $t_{RP} + t_{RCD}$  should elapse since the specified bank of some RDRAMs might be open). This transaction must be repeated at intervals of  $t_{REF} / (N_{BNK} \cdot N_{ROW})$ , where  $N_{BNK}$  and  $N_{ROW}$  are the number of banks and rows in the RDRAM. This interval will be the same for the different RDRAM configurations. For each refresh transaction, the bank and row field of A35..A3 must be incremented, with the bank field changing most often so the  $t_{RAS,MAX}$  parameter is not exceeded.

## CURRENT CONTROL

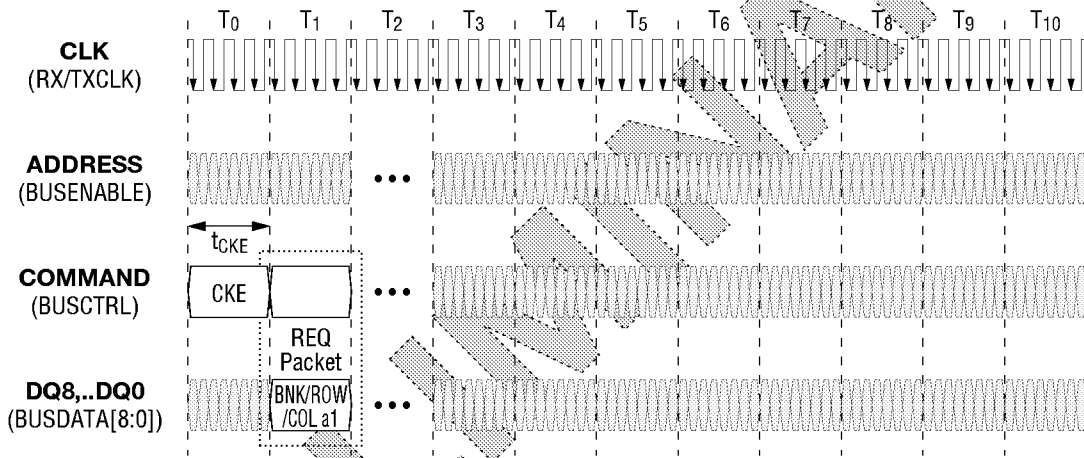
The transaction format for current control is shown in Figure 22 (b). This transaction is encoded as a directed register read operations, and is repeated at intervals of  $t_{CTRL} / N_{DEV}$ , where  $N_{DEV}$  is the number of devices on the Channel. This will maintain the optimal current control value.

OP5..0	000110 <sub>2</sub>	A35..3	DEV:	next device
AUTO	0		BNK:	0..0 (unused)
ACTV	0		ROW:	0..0 (unused)
PEND	000		COL:	00000101 <sub>2</sub>
M7..0	0000000 <sub>2</sub>	REGSEL:	0	

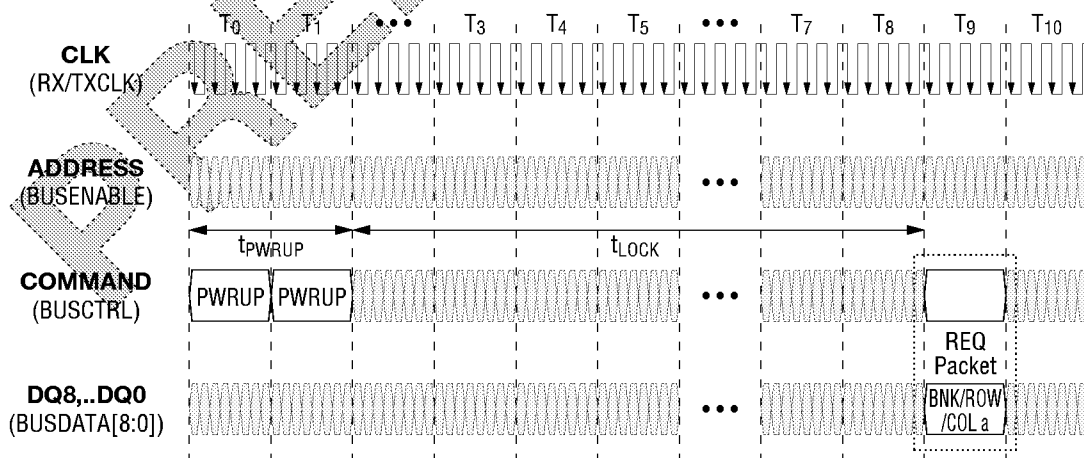
After a  $t_{LOCK}$ , a series of 64 of these current control transactions must be directed to each device on the Channel to establish the optimal current control value.



(a) RESET PACKET FOR INITIALIZATION

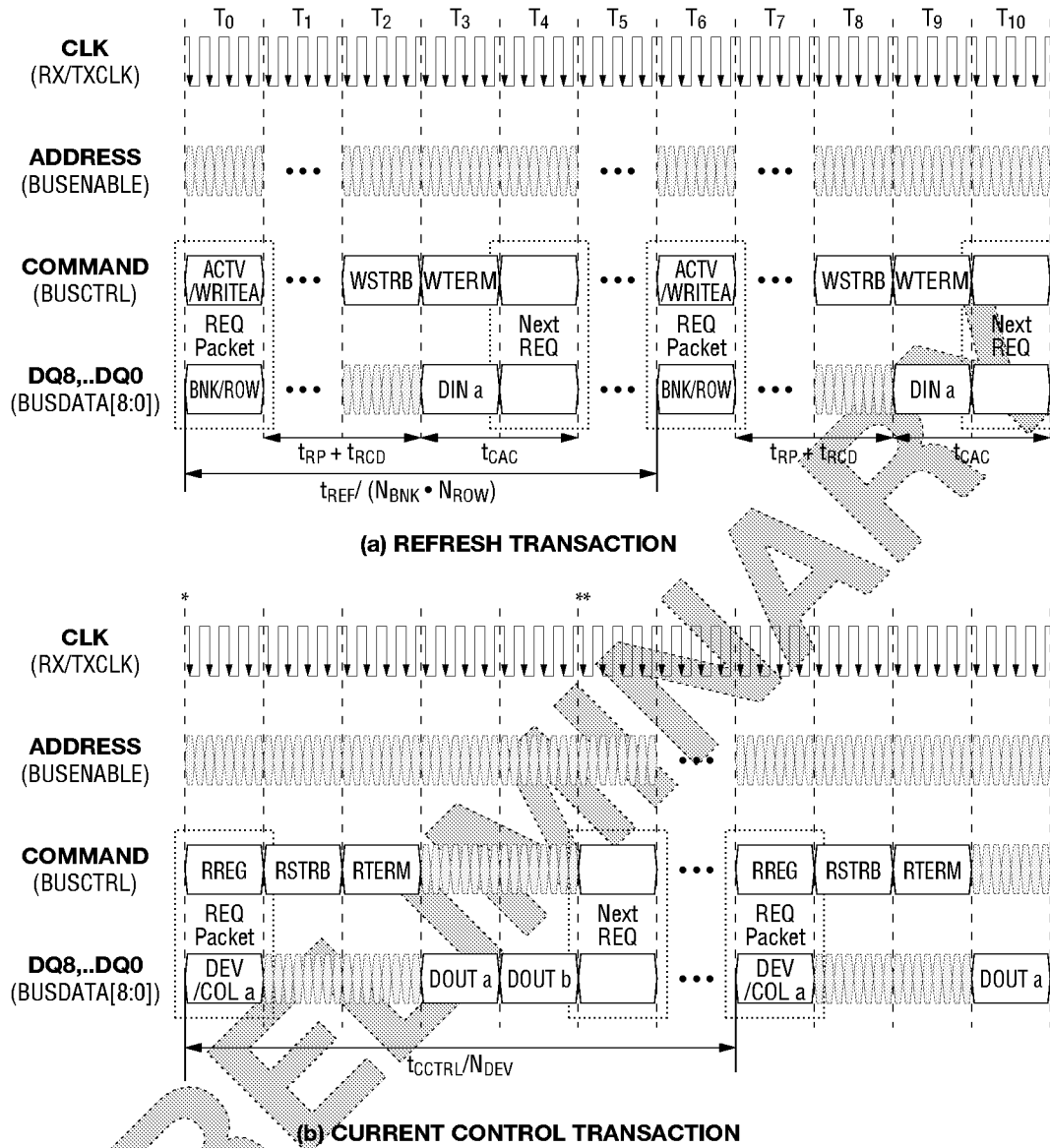


(b) CKE PACKET FOR SUSPEND-TO-ENABLE POWER MODE TRANSITION



(c) PWRUP PACKET FOR POWERDOWN-TO-ENABLE POWER MODE TRANSITION

Fig. 21 Transactions using RESET, CKE, and PWRUP Packets



**Fig. 22 Refresh and Current Control Transactions**

Due to the nature of the current control operation, a delay of 4 BusClks may be needed before and after the current control transaction.

If the request immediately before the current control request is a write request, there should be a 4 BusClks (1 Synclk) delay between the end of write data and the beginning of the RDRAM current control request (see \* in Figure 22 (b)). If the request immediately before the current control request is a read request, no delay is required.

If the current control data is followed by a request using the MODE register address, there must be a 4BusClks (1 Synclk) delay between the end of current control data transport and the subsequent requests using the MODE register addresses (see \*\* in Figure 22 (b)). Any other request may immediately follow the current control data transport.

## ABSOLUTE MAXIMUM RATINGS

The following table represents stress ratings only, and functional operation at the maximum ratings is not guaranteed. Extended exposure to the maximum ratings may affect device reliability. Although these devices contain protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Symbol	Parameter	Min.	Max.	Unit
$V_{I,ABS}$	Voltage applied to any RSL pin with respect to Gnd	-0.3	$V_{DD,MAX}+0.3$	V
$V_{I,CMOS,ABS}$	Voltage applied to any CMOS pin with respect to Gnd	-0.3	$V_{DD}+0.3$	V
$V_{DD,ABS}$	Voltage on $V_{DD}$ with respect to Gnd	-0.3	$V_{DD,MAX}+1.0$	V
$T_{J,ABS}$	Junction temperature under bias	-55	125	°C
$T_{STORE}$	Storage temperature	-55	125	°C

## THERMAL PARAMETERS

Symbol	Parameter and Conditions	Min.	Max.	Unit
$T_J$	Junction operating temperature	0	100	°C
$\Theta_{JC}$	Junction-to-Case thermal resistance	—	5	°C/Watt

## CAPACITANCE

Symbol	Parameter and Conditions	Min.	Max.	Unit
$C_I$	RSL input parasitic capacitance	1.6 <sup>a</sup> /2.0 <sup>b</sup>	2.0 <sup>a</sup> /2.5 <sup>b</sup>	pF
$L_I$	RSL input parasitic inductance	—	2.7 <sup>a</sup> /5.0 <sup>b</sup>	nH
$C_{I,CMOS}$	CMOS input parasitic capacitance	—	8	pF

Notes:

- a. 16M/18M RDRAM.
- b. 64M RDRAM.

## IDD-SUPPLY CURRENT PROFILE

( $T_a = 0^\circ\text{C}$  to  $70^\circ\text{C}$ )

Mode	Description	Min.	Max.	Unit
Powerdown	Device shut down, clock unlocked	—	1.0	mA
Suspend	Device inactive, clock locked but Suspended	—	95	mA
Enable	Device active, clock unlocked and Enabled	—	340	mA
READ	Device reading column data	—	500	mA
WRITE	Device writing column data	—	430	mA
ACTV/Enable	Device evaluating REQ packet and activating row in bank	—	330	mA
ACTV/READ	Device reading column data in bank 1 and activating row in bank 2	—	600	mA
ACTV/WRITE	Device writing column data in bank 1 and activating row in bank 2	—	580	mA

**RECOMMENDED ELECTRICAL CONDITIONS**

(Ta = 0°C to 70°C)

Symbol	Parameter and Conditions	Min.	Max.	Unit
V <sub>DD</sub> , V <sub>DDA</sub>	Supply voltage — 3.3 V version	3.15	3.45	V
V <sub>REF</sub>	Reference voltage	1.9	V <sub>DD</sub> -0.8	V
V <sub>IL</sub>	RSL Input low voltage <sup>b</sup>	V <sub>REF</sub> -0.35	V <sub>REF</sub> -0.8	V
V <sub>IH</sub>	RSL Input high voltage <sup>b</sup>	V <sub>REF</sub> +0.35	V <sub>REF</sub> +0.8	V
V <sub>IL,CMOS</sub>	CMOS input low voltage	-0.5	0.8	V
V <sub>IH,CMOS</sub>	CMOS input high voltage	1.8	V <sub>DD</sub> +0.5	V

**ELECTRICAL CHARACTERISTICS**

(Ta = 0°C to 70°C)

Symbol	Parameter and Conditions	Min.	Max.	Unit
I <sub>REF</sub>	V <sub>REF</sub> CURRENT @ V <sub>REF,MAX</sub>	-10	10	μA
I <sub>OH</sub>	RSL output high current @ (0 ≤ V <sub>OUT</sub> ≤ V <sub>DD</sub> )	-10	10	μA
I <sub>NONE</sub> (manual)	RSL I <sub>OL</sub> current @ V <sub>OUT</sub> = 1.6 V @ C[5:0] = 000000 (0 <sub>10</sub> ) <sup>a</sup>	0.0	4.0	mA
I <sub>ALL</sub> (manual)	RSL I <sub>OL</sub> current @ V <sub>OUT</sub> = 1.6 V @ C[5:0] = 111111 (63 <sub>10</sub> ) <sup>a</sup>	30.0	80.0	mA
I <sub>I,CMOS</sub>	CMOS input leakage current @ (0 ≤ V <sub>I,CMOS</sub> ≤ V <sub>DD</sub> )	-10.0	10.0	μA
V <sub>OL,CMOS</sub>	CMOS output voltage @ I <sub>OL,CMOS</sub> = 1.0 mA	0.0	0.4	V
V <sub>OH,CMOS</sub>	CMOS output high voltage @ I <sub>OH,CMOS</sub> = -0.25 mA	2.0	V <sub>DD</sub>	V

Note:

- In manual-calibration mode (CCEnable = 0) this is the value written into the C[5:0] field of the Mode register to produce the indicated I<sub>OL</sub> value. Values of I<sub>OL</sub> in between the I<sub>NONE</sub> and I<sub>ALL</sub> are produced by interpolating C[5:0] to intermediate values. For example, C[5:0] = 011111 (31<sub>10</sub>) produces an I<sub>OL</sub> in the range of 20 to 40 mA.
- I<sub>OL</sub> of Bus Data outputs is set at 30 mA when Bus Enable pin V<sub>IH</sub>/V<sub>IL</sub> value is measured.

## RECOMMENDED TIMING CONDITIONS

(Ta = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit
t <sub>CR</sub> , t <sub>CF</sub>	TXCLK and RXCLK input rise and fall times	0.3	0.8	ns
t <sub>CYCLE</sub>	TXCLK and RXCLK cycle times	3.75 <sup>a</sup> / 3.33 <sup>b</sup>	4.15 <sup>a</sup> / 4.15 <sup>b</sup>	ns
t <sub>TICK</sub>	Transfer time per bit per pin (this timing interval is synthesized by the RDRAM's clock generator)	0.5	0.5	t <sub>CYCLE</sub>
t <sub>CH</sub> , t <sub>CL</sub>	TXCLK and RXCLK high and low times	45%	55%	t <sub>CYCLE</sub>
t <sub>TR</sub>	TXCLK-RXCLK differential	0	0.7	t <sub>CYCLE</sub>
t <sub>PACKET</sub>	Transfer time for REQ, DIN, DOUT, COL, WSTRB, WTERM, RSTRB, RTERM, CKE, PWRUP and RESET packets	4	4	t <sub>CYCLE</sub>
t <sub>DR</sub> , t <sub>DF</sub>	DQ/ADDRESS/COMMAND input rise and fall times	0.3	0.6	ns
t <sub>S</sub>	DQ/ADDRESS/COMMAND-to-RXCLK setup time	0.35 <sup>c</sup>	—	ns
t <sub>H</sub>	RXCLK-to-DQ/ADDRESS/COMMAND hold time	0.35 <sup>c</sup>	—	ns
t <sub>REF</sub>	Refresh interval	—	17 <sup>d</sup> / 33 <sup>e</sup>	ms
t <sub>SCYCLE</sub>	Powerdown refresh cycle time	0.4	16.6 <sup>d</sup> / 8.0 <sup>e</sup>	μs
t <sub>SL</sub>	Powerdown refresh low time	0.2	10	μs
t <sub>SH</sub>	Powerdown refresh high time	0.2	10	μs
t <sub>CCTRL</sub>	Current control interval	—	150	ms
t <sub>RAS</sub>	RAS interval (time a row may stay activated)	—	133	μs
t <sub>LOCK</sub>	RDRAM clock-locking time for reset or powerup	—	5.0	μs

## Notes:

- a. 533 MHz RDRAM
- b. 600 MHz RDRAM
- c. 600 MHz IO timing
- d. 16M/18Mbit
- e. 64Mbit



**TIMING CHARACTERISTICS**

(Ta = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit
t <sub>PIO</sub>	SI <sub>n</sub> -to-SO <sub>u</sub> t delay @ C <sub>LOAD,CMOS</sub> = 40 pF	1	25	ns
t <sub>Q</sub>	DQ output time	-0.4 <sup>a</sup>	0.4 <sup>a</sup>	ns
t <sub>QR</sub> , t <sub>QF</sub>	DQ output rise and fall times	0.3	0.5	ns

Note:

a. 600 MHz IO timing

**RAMBUS CHANNEL TIMING**

The next table shows important timings on the Rambus channel for common operations. All timings are from the point of view of the channel master, and thus have the bus overhead delay of t<sub>CYCLE</sub> per bus transversal included where appropriate.

(Ta = 0°C to 70°C)

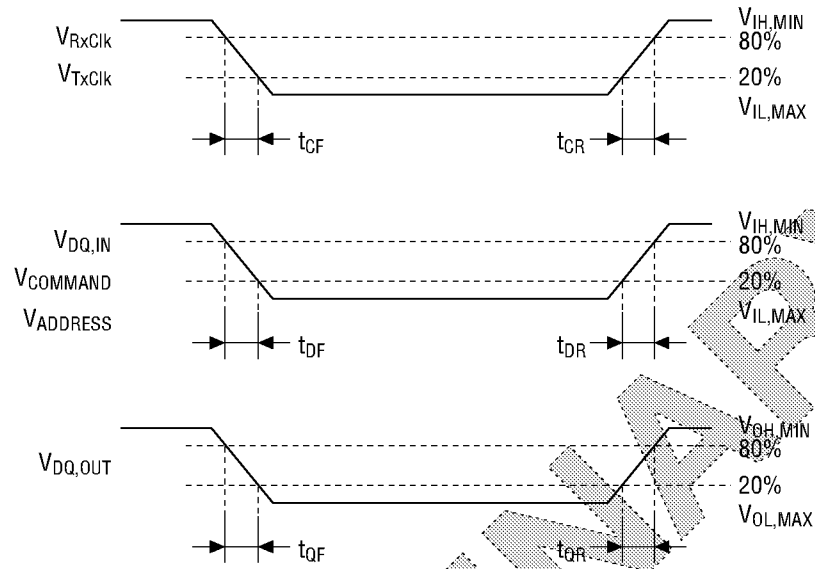
Symbol and Figure	Parameter	Min.	Max.
t <sub>CAC</sub> - Figure 8,9	Column Access time. May overlap t <sub>RCD</sub> , t <sub>RP</sub> , or t <sub>RPA</sub> to another bank	6 <sup>a</sup> / 7 <sup>b</sup>	—
t <sub>CC</sub> - Figure 8,9	Column Cycle time. May overlap t <sub>RCD</sub> , t <sub>RP</sub> , or t <sub>RPA</sub> to another bank	4	—
t <sub>RCD</sub> - Figure 8,9	Row to Column Delay. May overlap t <sub>CAC</sub> or t <sub>CC</sub> to another bank	8	—
t <sub>RP</sub> - Figure 8,9	Row Precharge time. May overlap t <sub>CAC</sub> or t <sub>CC</sub> to another bank	8	—
t <sub>RPA</sub> - Figure 8,9	Row Precharge Auto. May overlap t <sub>RPA</sub> , t <sub>CAC</sub> or t <sub>CC</sub> to another bank	8	—
t <sub>RAC</sub> - Figure 8,9	Row Access time. (t <sub>RAC</sub> = t <sub>RCD</sub> + t <sub>CAC</sub> )	15	—
t <sub>RC</sub> - Figure 8,9	Row Cycle time. (t <sub>RC</sub> = t <sub>RP</sub> + t <sub>RCD</sub> + t <sub>CAC</sub> )	23	—
t <sub>RSR</sub> - Figure 8 (a)	Start of REQ (READ) to start of RSTRB packet for Read transaction.	2	—
t <sub>ASR</sub> - Figure 8 (b)	Start of REQ (ACTV/READ) to start of RSTRB packet for Read transaction.	11	—
t <sub>PSR</sub> - Figure 8 (c)	Start of REQ (PRE/ACTV/READ) to start of RSTRB packet for Read transaction.	19	—
t <sub>CDR</sub> - Figure 8	Start of COL packet to start of DOUT packet for Read transaction.	12	12
t <sub>SDR</sub> - Figure 8	Start of RSTRB packet to start of DOUT packet for Read transaction.	8	8
t <sub>TDR</sub> - Figure 8	Start of RTERM packet to end of DOUT packet for Read transaction.	12	12
t <sub>WSW</sub> - Figure 9 (a)	Start of REQ (WRITE) to start of WSTRB packet for Write transaction.	0	—
t <sub>ASW</sub> - Figure 9 (b)	Start of REQ (ACTV/WRITE) to start of WSTRB packet for Write transaction.	5	—
t <sub>PSW</sub> - Figure 9 (c)	Start of REQ (PRE/ACTV/WRITE) to start of WSTRB packet for Write transaction.	13	—
t <sub>CDW</sub> - Figure 9	Start of COL packet to start of DIN packet for Write transaction.	8	8
t <sub>SDW</sub> - Figure 9	Start of WSTRB packet to start of DIN packet for Write transaction.	4	4
t <sub>TDW</sub> - Figure 9	Start of WTERM packet to end of DIN packet for Write transaction.	4	4
t <sub>RESET</sub> - Figure 21 (a)	Length of RESET packets to cause RDRAM to reset.	800 ns	—
t <sub>CKE</sub> - Figure 21 (b)	Start of CKE packet to start of REQ packet for Suspend-to-Enable.	4	7
t <sub>PWRUP</sub> - Figure 21 (c)	Length of PWRUP packets to cause Powerdown-to-Enable.	8	8
t <sub>WREG</sub> - Figure 14 (b)	End of DIN packet for WREG transaction to start of next REQ packet.	16	—

**Note:** All units are t<sub>CYCLE</sub> when not mentioned

- For READ, WRITE commands
- For ACTV/READ, ACTV/WRITE, PRE/ACTV/READ, PRE/ACTV/WRITE commands

**TIMING WAVEFORM**

**RSL Rise/Fall Timing**

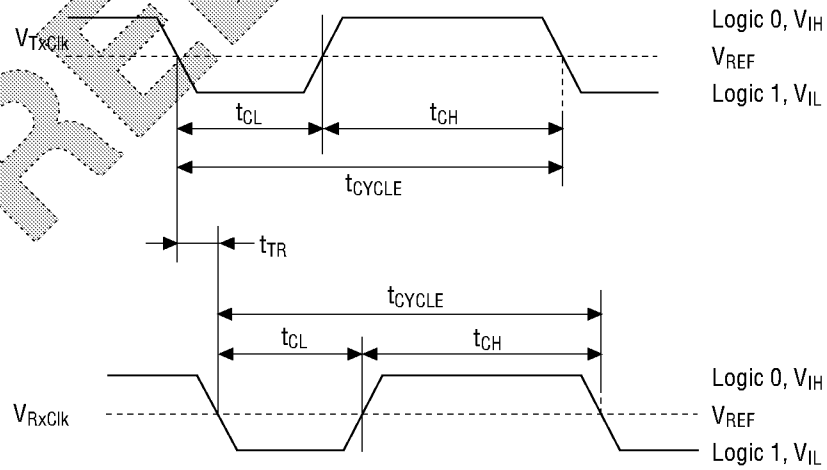


Where:

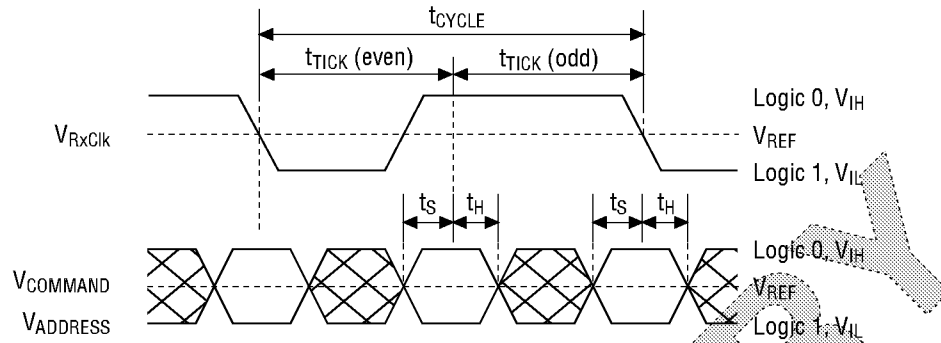
$$V_{OH,MIN} = V_{TERM,MIN}$$

$$V_{OL,MAX} = V_{TERM,MAX} - Z_0 * (I_{OL,MIN})$$

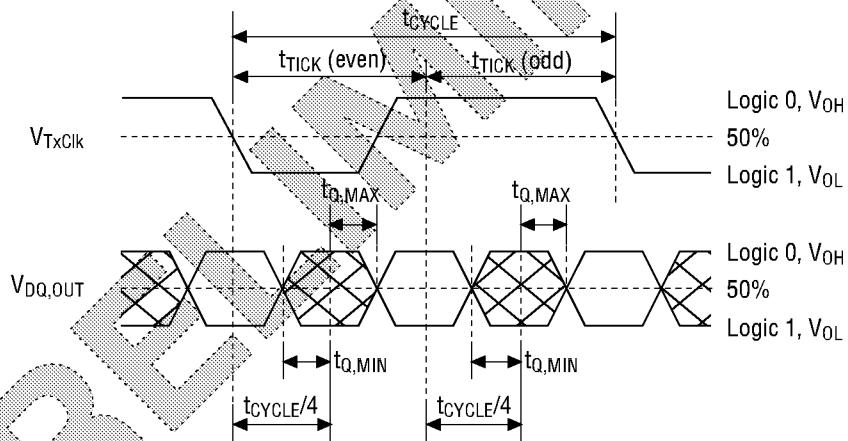
**RSL Clock Timing**



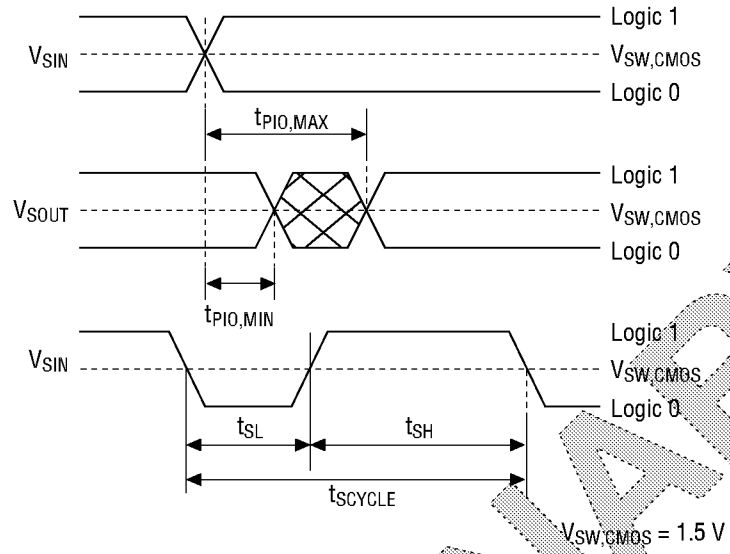
**RSL Input (Receive) Timing**



**RSL Output (Transmit) Timing**



SIN/SOUT Timing



PRELIMINARY

