FUJITSU

HARD DISK CONTROLLER

MB89341

October 1986
Edition 1.0

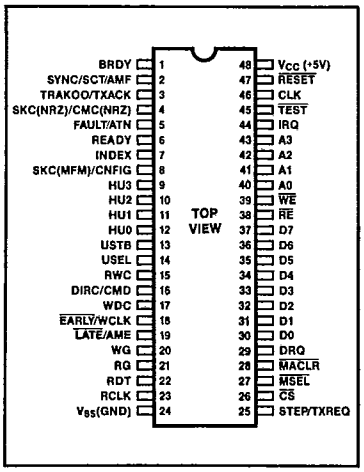
DESCRIPTION

The Fujitsu MB89341 Hard Disk Controller (HDC) interfaces with a host processor and a hard disk drive unit and provides data transfers between the two units in accordance with commands loaded from the host processor. The HDC is fabricated in CMOS and is housed in a 48-pin shrink DIP.

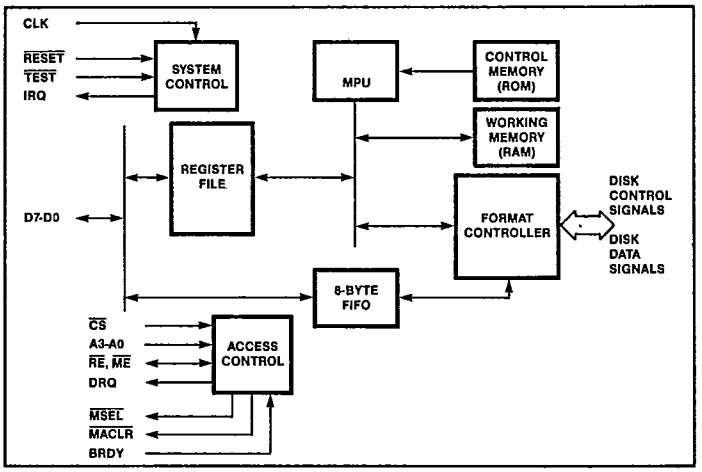
FEATURES

- Two programmable modulation modes: MFM and NRZ.
- High speed data transfers —
  MFM: Maximum of six megabits per second (typically 5 Mbps).
  NRZ: Maximum of 12 megabits per second (typically 10 Mbps).
- Programmable step rate —
  Fast: 1-to-8 μs in eight steps.
  Slow: 0.5-to-4 ms in eight steps.
- Multi-sector read/write and multi-track read/write.
- On-chip 8-byte FIFO for timing control of data transfers.
- On-chip memory buffer with arbitration logic.
- On-chip ECC with 32-bit fire code.
- Supports 16 drives and 16 head selections.
- Interface compatibility with Seagate ST506/412 specification and ESDI specification.
- CPU interface: Parallel data loading to register array.
- Silicon-gate CMOS process.
- Single +5V supply.

PIN CONFIGURATION



BLOCK DIAGRAM



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.