

# MB81C1000A-60/-70/-80/-10

## CMOS 1M x 1 BIT FAST PAGE MODE DYNAMIC RAM

### CMOS 1,048,576 X 1 Bit Fast Page Mode DRAM

The Fujitsu MB81C1000A is a CMOS, fully decoded dynamic RAM organized as 1,048,576 words x 1 bit. The MB81C1000A has been designed for mainframe memories, buffer memories, and video image memories requiring high speed and high-band width output with low power dissipation, as well as for memory systems of handheld computers which need very low power dissipation.

Fujitsu's advanced three-dimensional stacked capacitor cell technology gives the MB81C1000A high  $\alpha$ -ray soft error immunity and extended refresh time.

CMOS technology is used in the peripheral circuits to provide low power dissipation and high speed operation.

#### Features

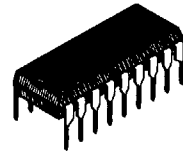
Parameter	MB81C1000A -60	MB81C1000A -70	MB81C1000A -80	MB81C1000A -10
RAS Access Time	60ns max.	70ns max.	80ns max.	100ns max.
Random Cycle Time	110ns min.	125ns min.	140ns min.	170ns min.
Address Access Time	30ns max.	35ns max.	40ns max.	50ns max.
CAS Access Time	15ns max.	20ns max.	20ns max.	25ns max.
Fast Page Mode Cycle Time	40ns min.	45ns min.	45ns min.	55ns min.
Low Power Dissipation	407mW max.	374mW max.	341mW max.	297mW max.
• Operating current • Standby current				

- 1,048,576 words x 1 bit organization
- Silicon gate, CMOS, 3D-Stacked Capacitor Cell
- All input and output are TTL compatible
- 512 refresh cycles every 8.2 ms
- Common I/O capability by using early write
- RAS only, CAS-before-RAS, or Hidden Refresh
- Fast Page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

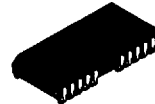
#### Absolute Maximum Ratings (See Note)

Parameter	Symbol	Value	Unit
Voltage at any pin relative to VSS	$V_{IN}, V_{OUT}$	-1 to +7	V
Voltage of $V_{CC}$ supply relative to VSS	$V_{CC}$	-1 to +7	V
Power Dissipation	PD	1.0	W
Short Circuit Output Current	—	50	mA
Storage Temperature	$T_{STG}$	-55 to +125	$^{\circ}C$

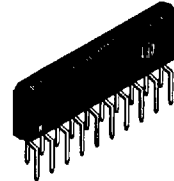
**NOTE:** Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



DIP-18P-M04



LCC-26P-M04



ZIP-20P-M02



\*FPT-24P-M04



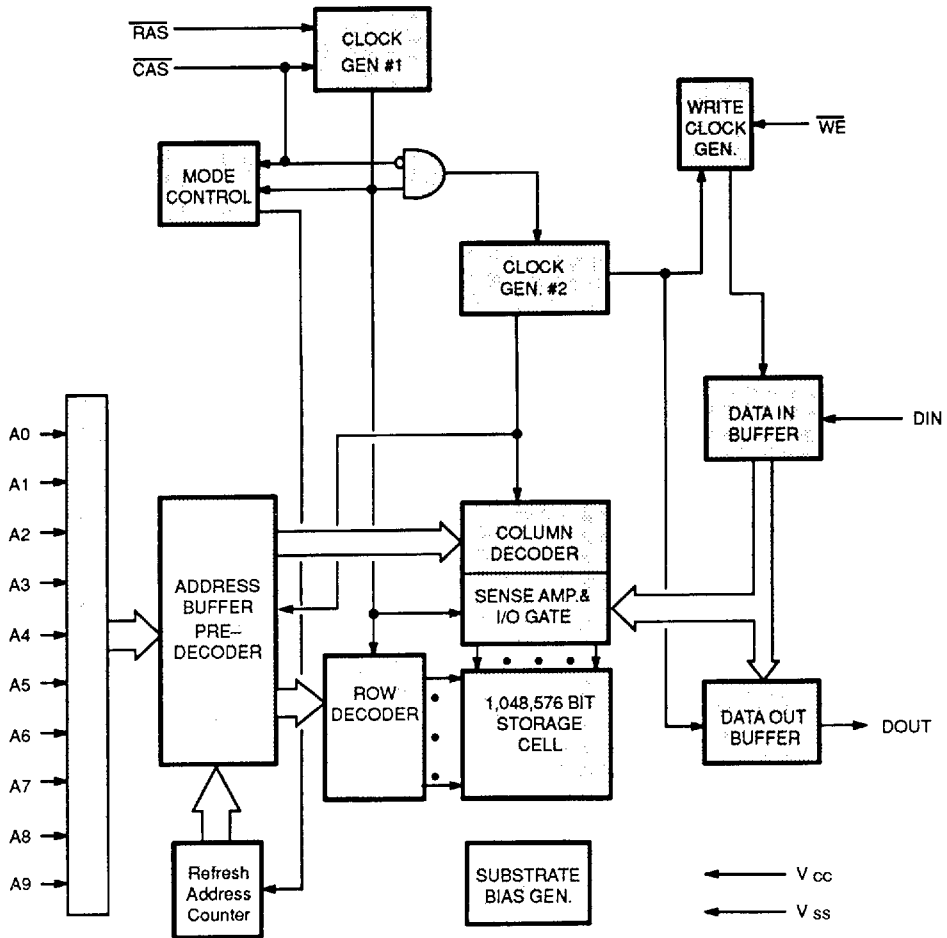
\*FPT-24P-M05

\*: Available for 70/80/100ns versions

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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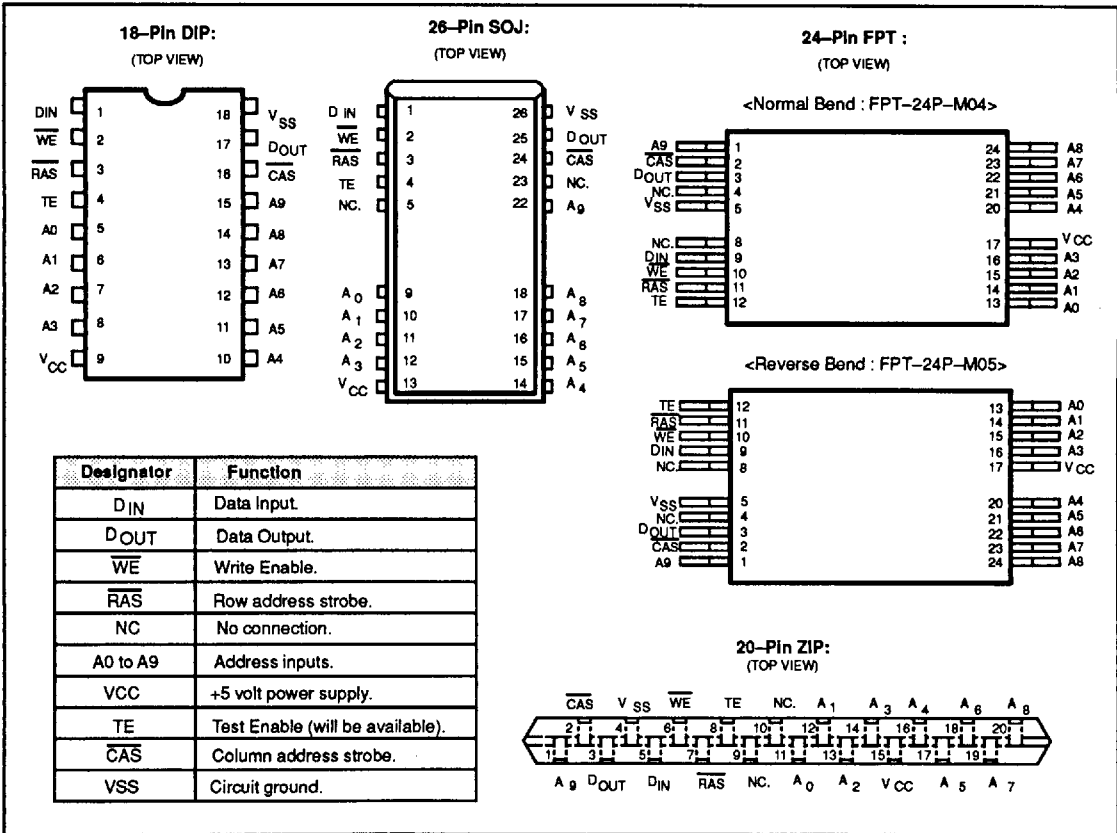
Fig. 1 — MB81C1000A DYNAMIC RAM—BLOCK DIAGRAM



**CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ )

Parameter	Symbol	Typ	Max	Unit
Input Capacitance, A0 to A9, D <sub>IN</sub>	C <sub>IN1</sub>	—	5	pF
Input Capacitance, $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$	C <sub>IN2</sub>	—	5	pF
Output Capacitance, D <sub>OUT</sub>	C <sub>OUT</sub>	—	6	pF

## PIN ASSIGNMENTS AND DESCRIPTIONS



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## RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min	Typ	Max	Unit	Ambient Operating Temp
Supply Voltage	1	V <sub>CC</sub>	4.5	5.0	5.5	V	0 °C to +70 °C
		V <sub>SS</sub>	0	0	0		
Input High Voltage, all inputs	1	V <sub>IH</sub>	2.4	—	6.5	V	
Input Low Voltage, all inputs	1	V <sub>IL</sub>	-2.0	—	0.8	V	

## FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any one of 1,048,576 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$  as shown in Figure 1. First, nine row address bits are input on pins A0 through A9 and latched with the row address strobe ( $\overline{\text{RAS}}$ ) then, ten column address bits are input and latched with the column address strobe ( $\overline{\text{CAS}}$ ). Both row and column addresses must be stable on or before the falling edge of  $\overline{\text{CAS}}$  and  $\overline{\text{RAS}}$ , respectively. The address latches are of the flow-through type; thus, address information appearing after  $t_{\text{RAH}}$  (min) +  $t_{\text{r}}$  is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of  $\overline{\text{WE}}$ . When  $\overline{\text{WE}}$  is active Low, a write cycle is initiated; when  $\overline{\text{WE}}$  is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Data is written into the MB81C1000A during write or read-modify-write cycle. The input data is strobed and latched by the later falling edge of  $\overline{\text{CAS}}$  or  $\overline{\text{WE}}$ . In an early write cycle, data input is strobed by  $\overline{\text{CAS}}$ , and set up and hold times are referenced to  $\overline{\text{CAS}}$ . In a delayed write or read-modify-write cycle,  $\overline{\text{WE}}$  is set low after  $\overline{\text{CAS}}$ . Thus, data input is strobed by  $\overline{\text{WE}}$ , and set up and hold times are referenced to  $\overline{\text{WE}}$ .

### DATA OUTPUT

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t<sub>RAC</sub>** : from the falling edge of  $\overline{\text{RAS}}$  when  $t_{\text{RCD}}$  (max) is satisfied.
- t<sub>CAC</sub>** : from the falling edge of  $\overline{\text{CAS}}$  when  $t_{\text{RCD}}$  is greater than  $t_{\text{RCD}}$ ,  $t_{\text{RAD}}$  (max).
- t<sub>AA</sub>** : from column address input when  $t_{\text{RAD}}$  is greater than  $t_{\text{RAD}}$  (max).

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Notes 3

Parameter	Notes	Symbol	Conditions	Values			Unit
				Min	Typ	Max	
Output high voltage		$V_{OH}$	$I_{OH} = -5 \text{ mA}$	2.4	—	—	V
Output low voltage		$V_{OL}$	$I_{OL} = 4.2 \text{ mA}$	—	—	0.4	
Input leakage current (any input)		$I_{IL}$	$0\text{V} \leq V_{IN} \leq 5.5\text{V};$ $4.5\text{V} \leq V_{CC} \leq 5.5\text{V};$ $V_{SS}=0\text{V};$ All other pins not under test = 0V	-10	—	10	$\mu\text{A}$
Output leakage current		$I_{OL}$	$0\text{V} \leq V_{OUT} \leq 5.5\text{V};$ Data out disabled	-10	—	10	
Operating current (Average power supply current) 2	MB81C1000A-60	$ICC_1$	$\overline{RAS}$ & $\overline{CAS}$ cycling; $t_{RC} = \text{min}$	—	—	74	mA
	MB81C1000A-70					68	
	MB81C1000A-80					62	
	MB81C1000A-10					54	
Standby current (Power supply current)	TTL level	$ICC_2$	$\overline{RAS}=\overline{CAS}=V_{IH}$	—	—	2.0	mA
	CMOS level		$\overline{RAS}=\overline{CAS} \geq V_{CC}-0.2\text{V}$			1.0	
Refresh current #1 (Average power supply current) 2	MB81C1000A-60	$ICC_3$	$\overline{CAS}=V_{IH}, \overline{RAS}$ cycling; $t_{RC} = \text{min}$	—	—	74	mA
	MB81C1000A-70					68	
	MB81C1000A-80					62	
	MB81C1000A-10					54	
Fast Page Mode current 2	MB81C1000A-60	$ICC_4$	$\overline{RAS} = V_{IL}, \overline{CAS}$ cycling; $t_{PC} = \text{min}$	—	—	61	mA
	MB81C1000A-70					56	
	MB81C1000A-80					56	
	MB81C1000A-10					46	
Refresh current #2 (Average power supply current) 2	MB81C1000A-60	$ICC_5$	$\overline{RAS}$ cycling ; $\overline{CAS}$ -before- $\overline{RAS}$ ; $t_{RC} = \text{min}$	—	—	74	mA
	MB81C1000A-70					68	
	MB81C1000A-80					62	
	MB81C1000A-10					54	

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MB81C1000A-60  
 MB81C1000A-70  
 MB81C1000A-80  
 MB81C1000A-10

## AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000A-60		MB81C1000A-70		MB81C1000A-80		MB81C1000A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
1	Time Between Refresh		$t_{REF}$	—	8.2	—	8.2	—	8.2	—	8.2	ms
2	Random Read/Write Cycle Time		$t_{RC}$	110	—	125	—	140	—	170	—	ns
3	Read-Modify-Write Cycle Time		$t_{RWC}$	130	—	145	—	165	—	200	—	ns
4	Access Time from $\overline{RAS}$	6,9	$t_{RAC}$	—	60	—	70	—	80	—	100	ns
5	Access Time from $\overline{CAS}$	7,9	$t_{CAC}$	—	15	—	20	—	20	—	25	ns
6	Column Address Access Time	8,9	$t_{AA}$	—	30	—	35	—	40	—	50	ns
7	Output Hold Time		$t_{OH}$	0	—	0	—	0	—	0	—	ns
8	Output Buffer Turn on Delay Time		$t_{ON}$	0	—	0	—	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	10	$t_{OFF}$	—	15	—	15	—	20	—	20	ns
10	Transition Time		$t_T$	2	50	2	50	2	50	2	50	ns
11	$\overline{RAS}$ Precharge Time		$t_{RP}$	40	—	45	—	50	—	60	—	ns
12	$\overline{RAS}$ Pulse Width		$t_{RAS}$	60	100000	70	100000	80	100000	100	100000	ns
13	$\overline{RAS}$ Hold Time		$t_{RSH}$	15	—	20	—	20	—	25	—	ns
14	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		$t_{CRP}$	0	—	0	—	0	—	0	—	ns
15	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	11,12	$t_{RCD}$	20	45	20	50	20	60	25	75	ns
16	$\overline{CAS}$ Pulse Width		$t_{CAS}$	15	—	20	—	20	—	25	—	ns
17	$\overline{CAS}$ Hold Time		$t_{CSH}$	60	—	70	—	80	—	100	—	ns
18	$\overline{CAS}$ Precharge Time (C-B-R cycle)	17	$t_{CPN}$	10	—	10	—	10	—	10	—	ns
19	Row Address Set Up Time		$t_{ASR}$	0	—	0	—	0	—	0	—	ns
20	Row Address Hold Time		$t_{RAH}$	10	—	10	—	10	—	15	—	ns
21	Column Address Set Up Time		$t_{ASC}$	0	—	0	—	0	—	0	—	ns
22	Column Address Hold Time		$t_{CAH}$	12	—	12	—	15	—	15	—	ns
23	$\overline{RAS}$ to Column Address Delay Time	13	$t_{RAD}$	15	30	15	35	15	40	20	50	ns
24	Column Address to $\overline{RAS}$ Lead Time		$t_{RAL}$	30	—	35	—	40	—	50	—	ns
25	Read Command Set Up Time		$t_{RCS}$	0	—	0	—	0	—	0	—	ns
26	Read Command Hold Time Referenced to $\overline{RAS}$	14	$t_{RRH}$	0	—	0	—	0	—	0	—	ns
27	Read Command Hold Time Referenced to $\overline{CAS}$	14	$t_{RCH}$	0	—	0	—	0	—	0	—	ns
28	Write Command Set Up Time	15	$t_{WCS}$	0	—	0	—	0	—	0	—	ns
29	Write Command Hold Time		$t_{WCH}$	10	—	10	—	12	—	15	—	ns
30	$\overline{WE}$ Pulse Width		$t_{WP}$	10	—	10	—	12	—	15	—	ns
31	Write Command to $\overline{RAS}$ Lead Time		$t_{RWL}$	15	—	15	—	20	—	25	—	ns
32	Write Command to $\overline{CAS}$ Lead Time		$t_{CWL}$	12	—	12	—	15	—	20	—	ns
33	DIN Set Up Time		$t_{DS}$	0	—	0	—	0	—	0	—	ns
34	DIN Hold Time		$t_{DH}$	10	—	10	—	12	—	15	—	ns

## AC CHARACTERISTICS (Continued)

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81C1000A-60		MB81C1000A-70		MB81C1000A-80		MB81C1000A-10		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
35	RAS to WE Delay Time	15	$t_{RWD}$	60	—	70	—	80	—	100	—	ns
36	CAS to WE Delay Time	15	$t_{CWD}$	15	—	20	—	20	—	25	—	ns
37	Column Address to WE Delay Time	15	$t_{AWD}$	30	—	35	—	40	—	50	—	ns
38	RAS Precharge Time to CAS Active Time (Refresh Cycles)		$t_{RPC}$	0	—	0	—	0	—	0	—	ns
39	CAS Set Up Time for CAS-before-RAS Refresh		$t_{CSR}$	0	—	0	—	0	—	0	—	ns
40	CAS Hold Time for CAS-before-RAS Refresh		$t_{CHR}$	10	—	10	—	12	—	15	—	ns
50	Fast Page Mode Read/Write Cycle Time		$t_{PC}$	40	—	45	—	45	—	55	—	ns
51	Fast Page Mode Read-Modify-Write Cycle Time		$t_{PRWC}$	57	—	62	—	65	—	80	—	ns
52	Access Time from CAS Precharge	9,16	$t_{CPA}$	—	35	—	40	—	40	—	50	ns
53	Fast Page Mode CAS Precharge Time		$t_{CP}$	10	—	10	—	10	—	10	—	ns

### Notes:

- Referenced to VSS
- ICC depends on the output load conditions and cycle rates; The specified values are obtained with the output open.  
ICC depends on the number of address change as  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  
ICC1, ICC3 and ICC5 are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .  
ICC4 is specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{CAS} = V_{IH}$ .
- An Initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200 $\mu$ s is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
- AC characteristics assume  $t_r = 5$ ns.
- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Also transition times are measured between  $V_{IH}$  (min) and  $V_{IL}$  (max).
- Assumes that  $t_{RCD} \leq t_{RCD}(\max)$ ,  $t_{RAD} \leq t_{RAD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig. 2 and 3.
- If  $t_{RCD} \geq t_{RCD}(\max)$ ,  $t_{RAD} \geq t_{RAD}(\max)$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{CAC}$ .
- If  $t_{RAD} \geq t_{RAD}(\max)$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{AA}$ .
- Measured with a load equivalent to two TTL loads and 100 pF.
- $t_{OFF}$  and  $t_{OEZ}$  is specified that output buffer change to high impedance state.
- Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
- $t_{RCD}(\min) = t_{RAH}(\min) + 2t_T + t_{ASC}(\min)$ .
- Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
- Either  $t_{TRH}$  or  $t_{TRC}$  must be satisfied for a read cycle.
- $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$  and  $t_{AWD}$  are not a restrictive operating parameter. They are included in the data sheet as an electrical characteristic only. If  $t_{WCS} > t_{WCS}(\min)$ , the cycle is an early write cycle and  $D_{out}$  pin will maintain high impedance state throughout the entire cycle. If  $t_{CWD} > t_{CWD}(\min)$ ,  $t_{RWD} > t_{RWD}(\min)$ , and  $t_{AWD} > t_{AWD}(\min)$ , the cycle is a read modify-write cycle and data from the selected cell will appear at the  $D_{out}$  pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the  $D_{out}$  pin, and write operation can be executed by satisfying  $t_{RWL}$ ,  $t_{CWL}$ , and  $t_{RAL}$  specifications.
- $t_{CPA}$  is access time from the selection of a new column address (that is caused by changing  $\overline{CAS}$  from "L" to "H"). Therefore, if  $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA}(\max)$ .
- Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh only.

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Fig. 2 -  $t_{RAC}$  vs.  $t_{RCD}$

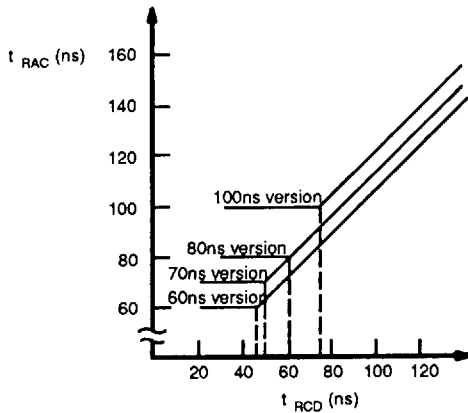
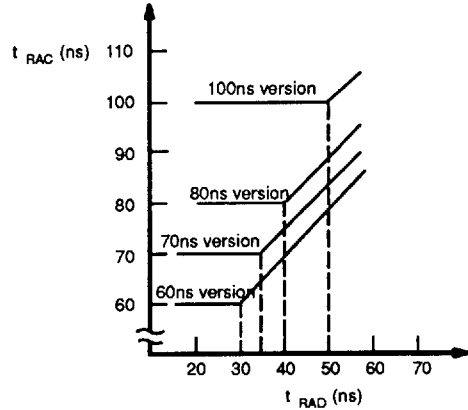


Fig. 3 -  $t_{RAC}$  vs.  $t_{RAD}$



## FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input			Address Input		Data		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row	Column	Input	Output		
Standby	H	H	X	—	—	—	High-Z	—	
Read Cycle	L	L	H	Valid	Valid	—	Valid	Yes *1	$t_{RCS} \geq t_{RCS}(\text{min})$
Write Cycle (Early Write)	L	L	L	Valid	Valid	Valid	High-Z	Yes *1	$t_{WCS} \geq t_{WCS}(\text{min})$
Read-Modify-Write Cycle	L	L	H → L	Valid	Valid	X → Valid	Valid	Yes *1	$t_{CWD} \geq t_{CWD}(\text{min})$
$\overline{RAS}$ -only Refresh Cycle	L	H	X	Valid	—	—	High-Z	Yes	
$\overline{CAS}$ -before- $\overline{RAS}$ Refresh Cycle	L	L	X	—	—	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}(\text{min})$
Hidden Refresh Cycle	H → L	L	X	—	—	—	Valid	Yes	Previous data is kept

**Notes:**

X : "H" or "L"

\*1: It is impossible in Fast Page Mode.





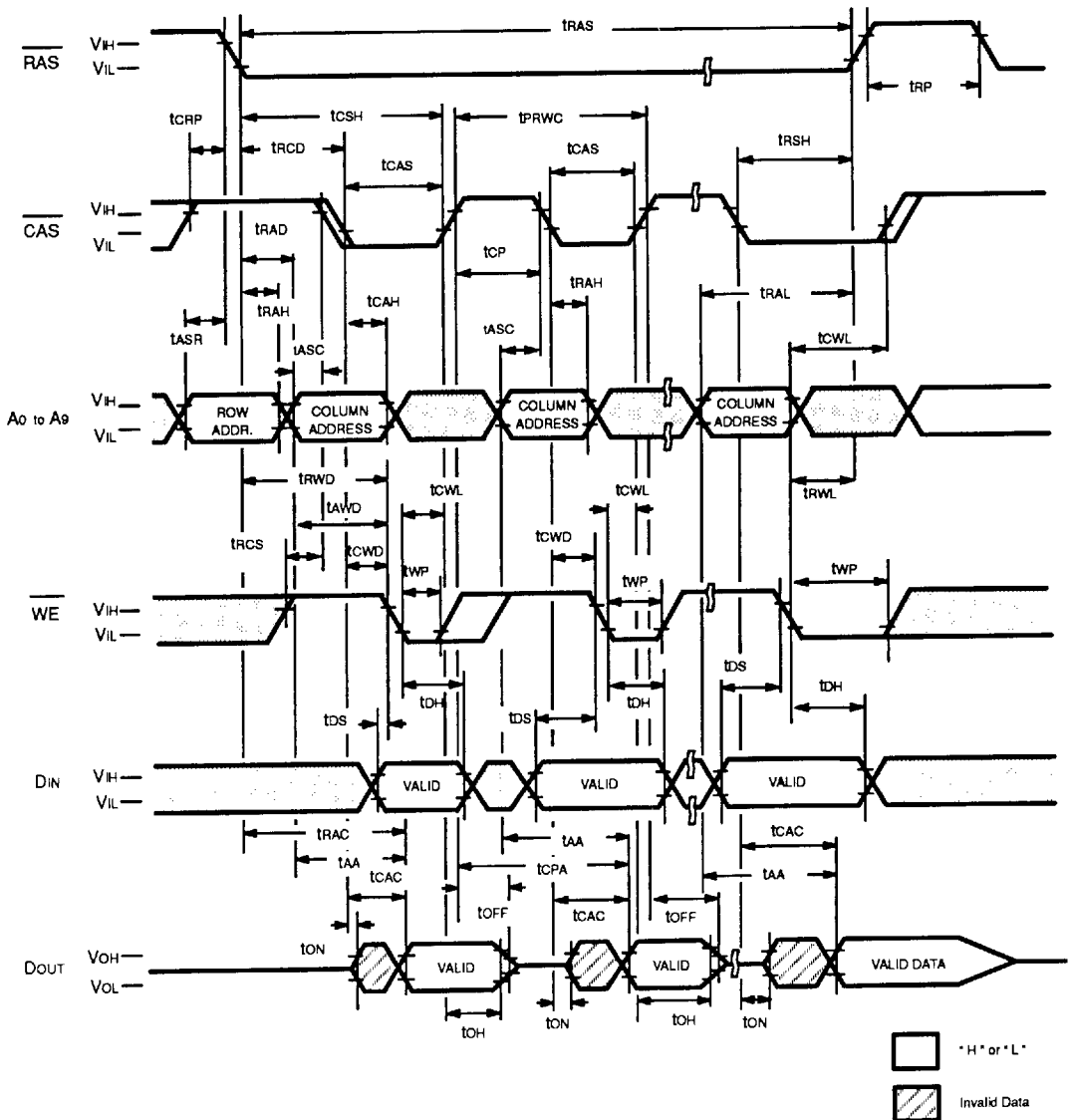








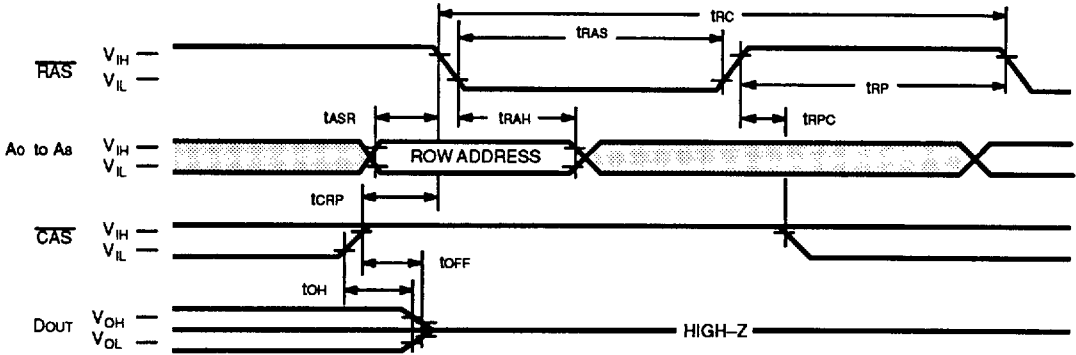
Fig. 9 - FAST PAGE MODE READ-MODIFY-WRITE CYCLE



DESCRIPTION

During fast page mode, the read-modify-write cycle can be executed by changing WE high to low after the data appears at DOUT pin as well as normal cycle. Any of the 1024 bits belonging to each row can be accessed.

Fig. 10 -  $\overline{\text{RAS}}$ -ONLY REFRESH CYCLE  
 NOTE: A9,  $\overline{\text{WE}}$ , DIN = "H" or "L"



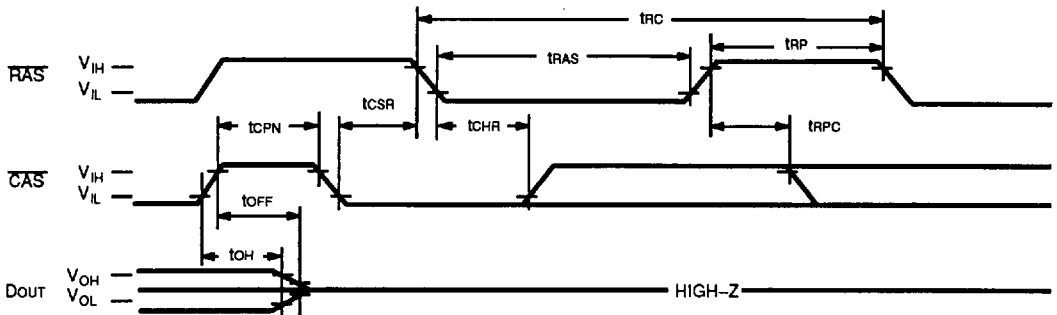
DESCRIPTION



Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 512 row addresses every 8.2-milliseconds. Three refresh modes are available:  $\overline{\text{RAS}}$ -only refresh,  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh, and hidden refresh.

$\overline{\text{RAS}}$ -only refresh is performed by keeping  $\overline{\text{RAS}}$  Low and  $\overline{\text{CAS}}$  High throughout the cycle; the row address to be refreshed is latched on the falling edge of  $\overline{\text{RAS}}$ . During  $\overline{\text{RAS}}$ -only refresh, DOUT pin is kept in a high-impedance state.

Fig. 11 -  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH CYCLE  
 NOTE: A0 to A9,  $\overline{\text{WE}}$ , DIN = "H" or "L"

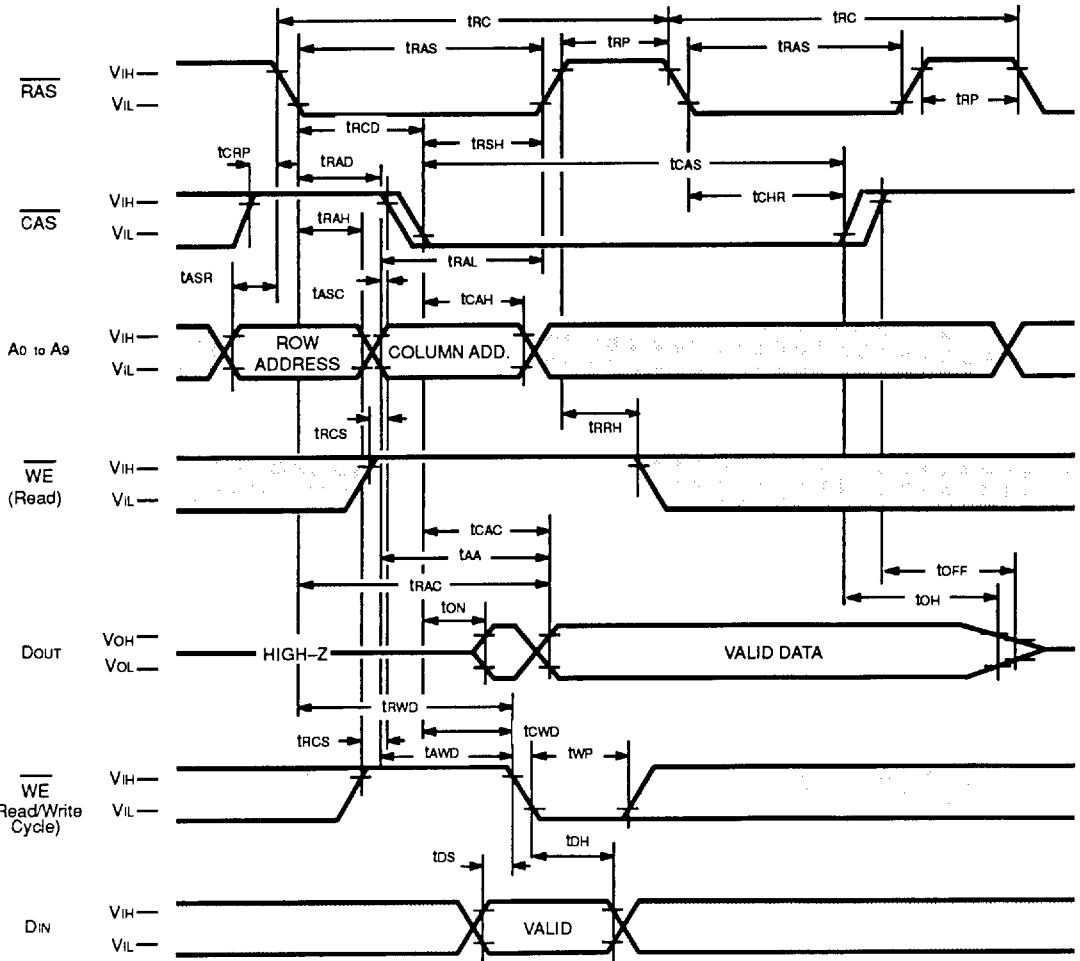


DESCRIPTION

$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If  $\overline{\text{CAS}}$  is held Low for the specified setup time ( $t_{\text{CSR}}$ ) before  $\overline{\text{RAS}}$  goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh operation.

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Fig. 12 - HIDDEN REFRESH CYCLE



□ "H" or "L"

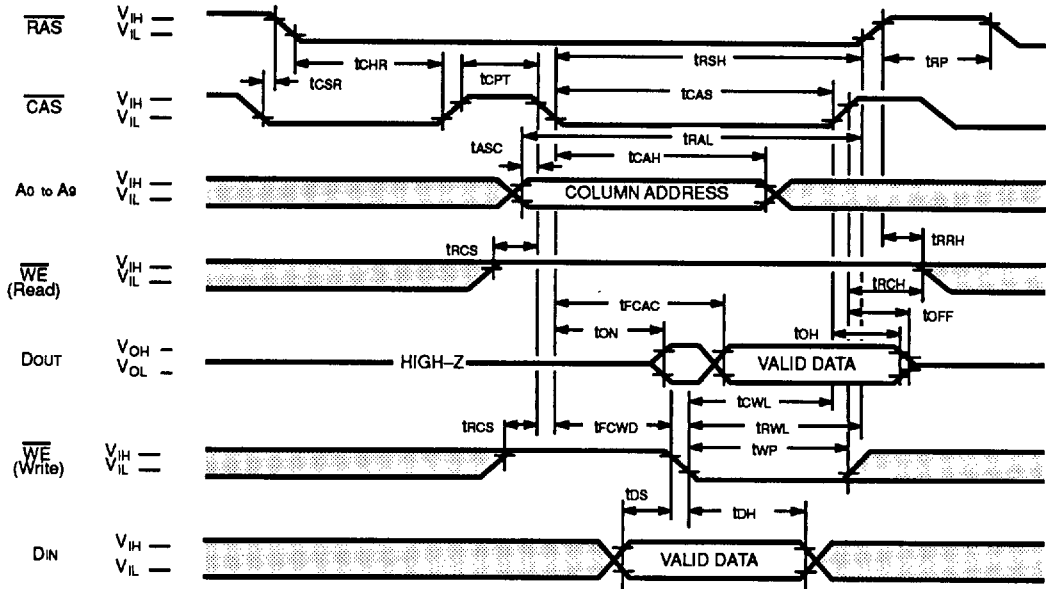
DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{CAS}$  and cycling  $\overline{RAS}$ . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{CAS}$ -before- $\overline{RAS}$  refresh capability.

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Fig. 13 –  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH COUNTER TEST CYCLE



   \*H\* or \*L\*

**DESCRIPTION**

A special timing sequence using the  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle provides a convenient method to verify the functionality of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh circuitry. If, after a  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycle,  $\overline{\text{CAS}}$  makes a transition from High to Low while  $\overline{\text{RAS}}$  is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

- Row Address: Bits A0 through A9 are defined by the on-chip refresh counter. The bit A9 is set high internally.
- Column Address: Bits A0 through A9 are defined by latching levels on A0–A9 at the second falling edge of  $\overline{\text{CAS}}$ .

The  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Counter Test procedure is as follows :

- 1) Initialize the internal refresh address counter by using 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh cycles.
- 2) Use the same column address throughout the test.
- 3) Write "0" to all 512 row addresses at the same column address by using normal write cycles.
- 4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test (read-modify-write cycles). Repeat this procedure 512 times with addresses generated by the internal refresh address counter.
- 5) Read and check data written in procedure 4) by using normal read cycle for all 512 memory locations.
- 6) Complement test pattern and repeat procedures 3), 4), and 5).

(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81C1000A-60		MB81C1000A-70		MB81C1000A-80		MB81C1000A-10		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
90	Access Time from $\overline{\text{CAS}}$	$t_{\text{FCAC}}$	—	40	—	45	—	50	—	60	ns
91	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	$t_{\text{FCWD}}$	40	—	45	—	50	—	60	—	ns
92	$\overline{\text{CAS}}$ Precharge Time	$t_{\text{CPT}}$	20	—	20	—	20	—	20	—	ns

Note . Assumes that  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  refresh counter test cycle only.

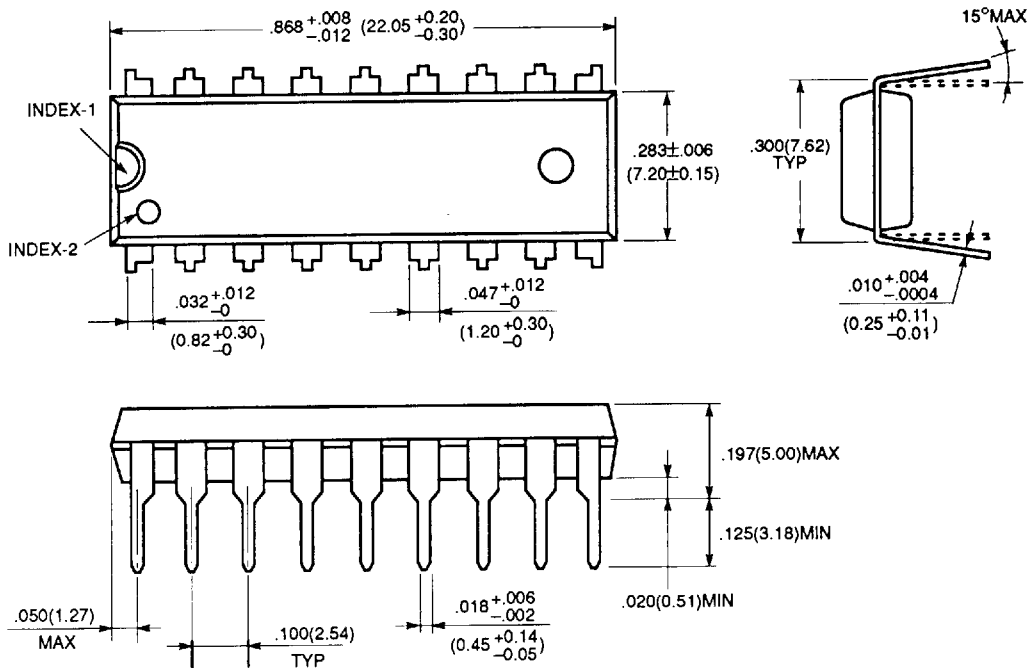
1

MB81C1000A-60  
MB81C1000A-70  
MB81C1000A-80  
MB81C1000A-10

## PACKAGE DIMENSIONS

(Suffix: -P)

18-LEAD PLASTIC DUAL IN-LINE PACKAGE  
(CASE No.: DIP-18P-M04)



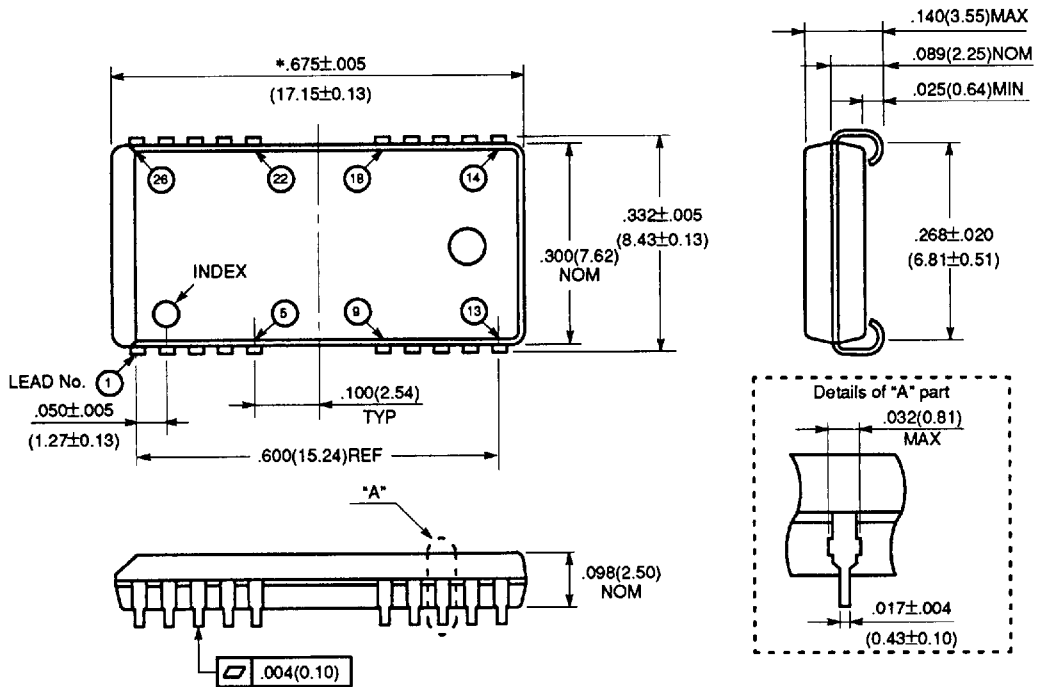
©1991 FUJITSU LIMITED D18015S-4C

Dimensions in  
inches (millimeters)

# PACKAGE DIMENSIONS (Continued)

(Suffix: -PJ)

## 26-LEAD PLASTIC LEADED CHIP CARRIER (CASE No.: LCC-26P-M04)



- Note:**
1. \*: This dimension includes resin protrusion. (Each side:  $.006$  (0.15) MAX)
  2. Although this package has 20 leads only, its pin positions are the same as that of 26-lead package.
  3. Dimensions in inches (millimeters)

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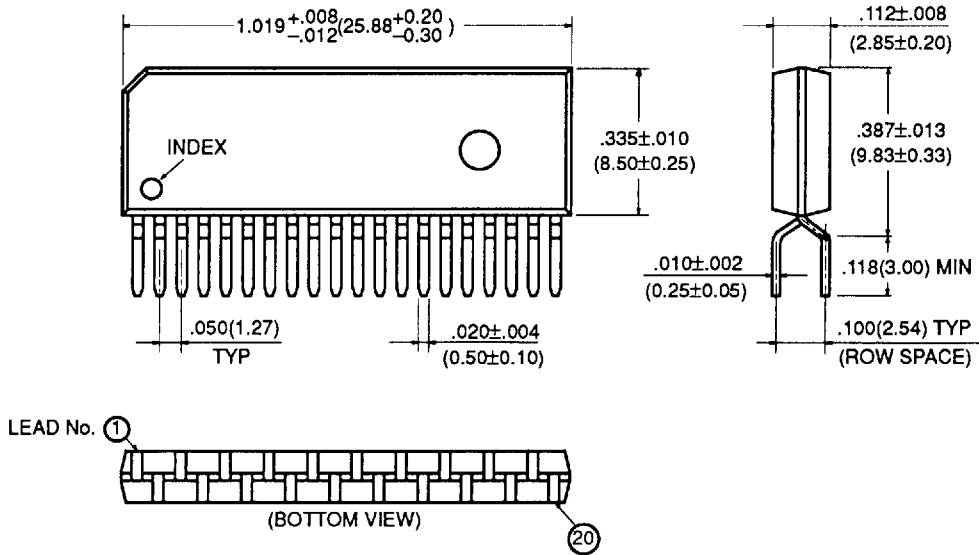
1

MB81C1000A-60  
MB81C1000A-70  
MB81C1000A-80  
MB81C1000A-10

# PACKAGE DIMENSIONS (Continued)

(Suffix: -PSZ)

## 20-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE (CASE No.: ZIP-20P-M02)



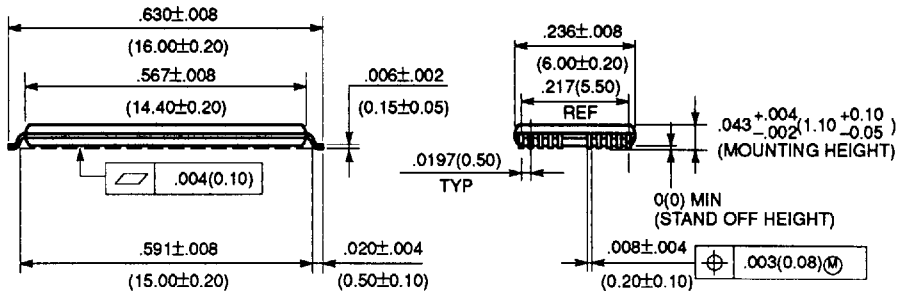
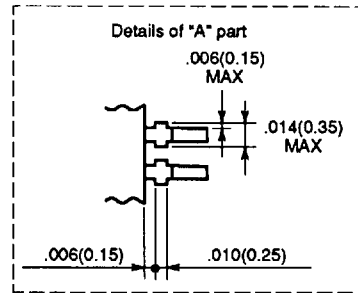
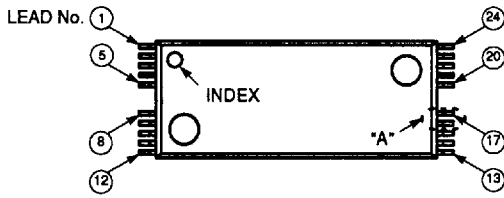
©1991 FUJITSU LIMITED Z20002S-4C

Dimensions in  
inches (millimeters)

# PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTN)

## 24-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-24P-M04)



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Dimensions in  
 inches (millimeters)

1

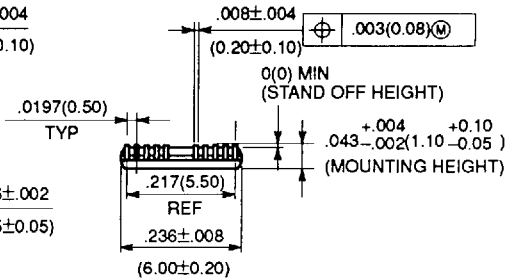
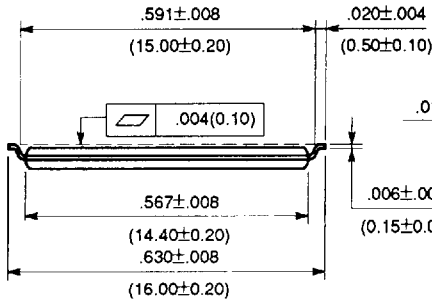
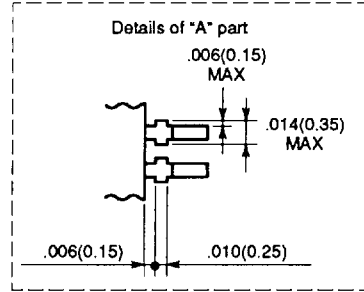
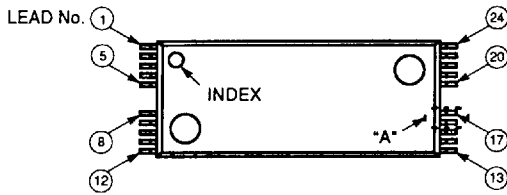
MB81C1000A-60  
 MB81C1000A-70  
 MB81C1000A-80  
 MB81C1000A-10

# PACKAGE DIMENSIONS (Continued)

(Suffix: -PFTR)

1

## 24-LEAD PLASTIC FLAT PACKAGE (CASE No.: FPT-24P-M05)



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Dimensions in  
 inches (millimeters)

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