CPC7583
Line Card Access Switch

Features
- Small 28 pin surface mount SOIC package
- Monolithic IC reliability
- Low matched RDS_{ON}
- Eliminates the need for zero cross switching
- Flexible switch timing to transition from ringing mode to idle/talk mode
- Clean, bounce free switching
- Tertiary protection consisting of integrated current limiting, thermal shutdown and SLIC protection
- 5V operation with power consumption <10mW
- Intelligent battery monitor
- Latched logic level inputs, no drive circuitry
- Pin to pin compatible to the Lucent 7583 family

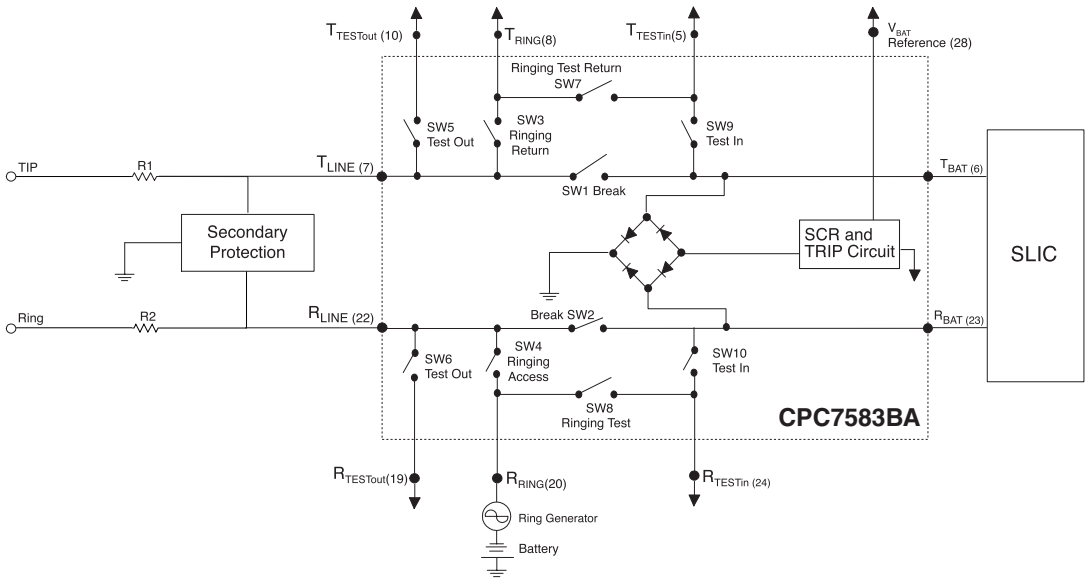
Applications
- Central office (CO)
- Digital Loop Carrier (DLC)
- PBX Systems
- Digitally Added Main Line (DAML)
- Hybrid Fiber Coax (HFC)
- Fiber in the Loop (FITL)
- Pair Gain System
- Channel Banks

Description
The CPC7583 is a monolithic solid state switch in a 28 pin surface mount SOIC package. It provides the necessary functions to replace three 2-Form-C electromechanical relays on analog line cards found in Central Office, Access and PBX equipment. The device contains solid state switches for tip and ring line break, ring injection/ring return, line test access, test in access and ringing generator testing. The CPC7583 requires only a +5V supply and offers “break-before-make” or “make-before-break” switch operation using simple logic level input control. The CPC7583 has 4 versions. The CPC7583BA and the CPC7583BC contain the integrated protection SCR while the CPC7583BC and the CPC7583BD contain an extra logic state which is detailed in later sections.

Ordering Information

Part #	Description
CPC7583BA	10 Pole with protection SCR
CPC7583BB	10 Pole without protection SCR
CPC7583BC	10 Pole extra logic state with protection SCR
CPC7583BD	10 Pole extra logic state without protection SCR
CPC7583BATR	Tape and Reel Version
CPC7583BBTR	Tape and Reel Version
CPC7583BCTR	Tape and Reel Version
CPC7583BDTR	Tape and Reel Version

Block Diagram



Parameter	Min	Max	Units
Operating Temperature Range	-40	+110	˚C
Storage Temperature Range	-40	+150	˚C
Relative Humidity Range	5	95	%
Pin Soldering Temperature (t=10 s max)	-	+260	˚C
+5V Power Supply	-	7	V
Battery Supply	-	-85	V
Logic Input Voltage	-	7	V
Logic Input to Switch Output Isolation	-	330	V
Switch Isolation (SW1, SW2, SW3, SW5, SW6, SW7, SW9,SW10)	-	330	V
Switch Isolation (SW4)	-	480	V
Switch Isolation (SW8)	-	235	V

Absolute Maximum Ratings are stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this data sheet is not implied. Exposure of the device to the absolute maximum ratings for extended period may degrade the device and effect its reliability.

Electrical Characteristics TA = -40°C to +85°C (unless otherwise specified)

Minimum and maximum values are production testing requirements. Typical values are characteristic of the device and are the result of engineering evaluations. Typical values are provided for information purposes only and are not part of the testing requirements.

Power Supply Specifications

Supply	Min	Typ	Max	Unit
V_{DD}	+4.5	+5.0	+5.5	V
V_{BAT} [1]	-19	-	-72	V

[1] V_{BAT} is used only as a reference for internal protection circuitry.
If V_{BAT} rises above -10V, the device will enter an all off state and will remain in the all off state until the battery voltage drops below -15V.

ESD Rating (HBM Model)
1000

Table 1. Break Switch, SW1 and SW2

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Off-state Leakage Current:						
+25°C	Vsw (differential)= -320V to Gnd Vsw (differential)= -60V to +260V	Isw	-	0.1	1	µA
+85°C	Vsw (differential)= -330V to Gnd Vsw (differential)= -60V to +270V	Isw	-	0.3	1	µA
-40°C	Vsw (differential)= -310V to Gnd Vsw (differential)= -60V to +250V	Isw	-	0.1	1	µA
RDS_{ON} (SW1,SW2):						
+25°C	T_{LINE}= +/-10 mA, +/-40mA, T_{BAT}= -2V	Δ V	-	14.5	-	Ω
+85°C	T_{LINE}= +/-10 mA, +/-40mA, T_{BAT}= -2V	Δ V	-	20.5	28	Ω
-40°C	T_{LINE}= +/-10 mA, +/-40mA, T_{BAT}= -2V	Δ V	-	10.5	-	Ω
RDS_{ON} Match	Per ON-resistance Test Condition of SW1, SW2	Magnitude R_{ON} SW1-R_{ON}SW2	-	0.15	0.8	Ω
DC Current Limit:						
+25°C	Vsw (on) = +/- 10V	Isw	-	225	-	mA
+85°C	Vsw (on) = +/- 10V	Isw	80	150	-	mA
-40°C	Vsw (on) = +/- 10V	Isw	-	400	425	mA
Dynamic Current Limit: (t=<0.5µs)	Break switches in ON state, ringing access switches OFF, apply +/- 1000V at 10/1000µs pulse, appropriate secondary protection in place.	Isw	-	2.5	-	A
Logic Input to Switch Output Isolation:						
+25°C	Vsw (T_{LINE}, R_{LINE}) = +/-320V Logic Inputs = Gnd	Isw	-	0.1	1	µA
+85°C	Vsw (T_{LINE}, R_{LINE}) = +/-330V Logic Inputs = Gnd	Isw	-	0.3	1	µA
-40°C	Vsw (T_{LINE}, R_{LINE}) = +/-310V Logic Inputs = Gnd	Isw	-	0.1	1	µA
dv/dt Sensitivity[1]	-	-	-	200	-	V/µs

[1] Applied voltage is 100 Vp-p square wave at 100Hz.

Table 2. Ring Return Switch, SW3

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Off-state Leakage Current						
+25°C	Vsw (differential)= -320V to Gnd Vsw (differential)= -60V to +260V	Isw	-	0.1	1	µA
+85°C	Vsw (differential)= -330V to Gnd Vsw (differential)= -60V to +270V	Isw	-	0.3	1	µA
-40°C	Vsw (differential)= -310V to Gnd Vsw (differential)= -60V to +250V	Isw	-	0.1	1	µA
DC Current Limit						
+25°C	Vsw (on) = +/- 10V	Isw	-	120	-	mA
+85°C	Vsw (on) = +/- 10V	Isw	-	80	-	mA
-40°C	Vsw (on) = +/- 10V	Isw	-	210	-	mA
Dynamic Current Limit: (t=<0.5µs)	Break switches in ON state, Ringing access switches OFF, Apply +/- 1000V at 10/1000µs pulse, Appropriate secondary protection in place.	Isw	-	2.5	-	A
RDS_{ON}						
+25˚C	Isw (on) = +/-0mA, +/-10mA	Δ V	-	60	-	Ω
+85˚C	Isw (on) = +/-0mA, +/-10mA	Δ V	-	85	100	Ω
-40˚C	Isw (on) = +/-0mA, +/-10mA	Δ V	-	45	-	Ω
Logic Input to Switch Output Isolation:						
+25°C	Vsw (T_{RING}, T_{LINE}) = +/-320V Logic Inputs = Gnd	Isw	-	0.1	1	µA
+85°C	Vsw (T_{RING}, T_{LINE}) = +/-330V Logic Inputs = Gnd	Isw	-	0.3	1	µA
-40°C	Vsw (T_{RING}, T_{LINE}) = +/-310V Logic Inputs = Gnd	Isw	-	0.1	1	µA

Table 3. Ringing Access Switch, SW4

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Off-state Leakage Current						
+25°C	Vsw (differential)= -255V to +210V Vswitch (differential)= +255V to -210V	Isw	-	.05	1	µA
+85°C	Vsw (differential)= -270V to +210V Vsw (differential)= +270V to -210V	Isw	-	0.1	1	µA
-40°C	Vsw (differential)= -245V to +210V Vsw (differential)= +245V to -210V	Isw	-	.05	1	µA
ON Voltage	Isw (on) = +/- 1mA	-	-	1.5	3	V
Ring Generator Current During Ring	Vcc = 5V, IN_{TESTin} = 0 $IN_{TESTout}$ = 0	I_R	-	0.1	0.25	mA
Surge Current	-	-	-	-	2	A
Release Current	-	-	-	450	-	µA
ON-resistance	Isw (on) = +/-70mA, +/-80mA	Δ V	-	8.5	12	Ω
Logic Input to Switch Output Isolation:						
+25°C	Vsw (R_{RING}, R_{LINE}) = +/-320V Logic Inputs = Gnd	Isw	-	.05	1	µA
+85°C	Vsw (R_{RING}, R_{LINE}) = +/-330V Logic Inputs = Gnd	Isw	-	0.1	1	µA
-40°C	Vsw (R_{RING}, R_{LINE}) = +/-310V Logic Inputs = Gnd	Isw	-	.05	1	µA

Table 4. Loop Access Switches, SW5 and SW6

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Off-state Leakage Current:						
+25°C	Vsw (differential) = -320V to +Gnd Vsw (differential) = -60V to +260V	Isw	-	0.1	1	µA
+85°C	Vsw (differential) = -330V to Gnd Vsw (differential) = -60V to +270V	Isw	-	0.3	1	µA
-40°C	Vsw (differential) = -310V to +Gnd Vsw (differential) = -60V to +250V	Isw	-	0.1	1	µA
RDS_{ON}:						
+25°C +85°C -40°C	Isw (on) = +/-5mA, +/-10mA Isw (on) = +/-5mA, +/-10mA Isw (on) = +/-5mA, +/-10mA	Δ V Δ V Δ V	- - -	35 50 26	- 70 -	Ω Ω Ω
DC Current Limit:						
+25°C +85°C -40°C	Vsw (on) = +/-10V Vsw (on) = +/-10V Vsw (on) = +/-10V	Isw Isw Isw	 80 -	140 100 210	- - 250	mA mA mA
Dynamic Current LImit (t=<0.5µs)	Break switches in ON state; ringing access switches OFF; apply +/-1000V at 10/1000µs pulse; appropriate secondary protection in place.	Isw	-	2.5	-	A
Logic Input to Switch Output Isolation:						
+25°C	Vsw ($T_{TESTout}$, T_{LINE}, $R_{TESTout}$, R_{LINE}) = +/-320V Logic Inputs = Gnd	Isw	-	0.1	1	µA
+85°C	Vsw ($T_{TESTout}$, T_{LINE}, $R_{TESTout}$, R_{LINE}) = +/-330V Logic Inputs = Gnd	Isw	-	0.3	1	µA
-40°C	Vsw ($T_{TESTout}$, T_{LINE}, $R_{TESTout}$, R_{LINE}) = +/-310V Logic Inputs = Gnd	Isw	-	0.1	1	µA

Table 5. Ringing Test Return Switch SW7

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Off-state Leakage Current:						
+25°C	Vsw (differential)= -320V to Gnd Vsw (differential)= -60V to +260V	Isw	-	0.1	1	µA
+85°C	Vsw (differential)= -330V to Gnd Vsw (differential)= -60V to +270V	Isw	-	0.3	1	µA
-40°C	Vsw (differential)= -310 to Gnd Vsw (differential)= -60V to +250V	Isw	-	0.1	1	µA
RDS_{ON}						
+25°C	Isw (on) = +/-0mA, +/-10mA	Δ V	-	60	-	Ω
+85°C	Isw (on) = +/-0mA, +/-10mA	Δ V	-	85	100	Ω
-40°C	Isw (on) = +/-0mA, +/-10mA	Δ V	-	45	-	Ω
DC Current Limit						
+25°C	Vsw (on) = +/- 10V	Isw	-	120	-	mA
+85°C	Vsw (on) = +/- 10V	Isw	-	80	-	mA
-40°C	Vsw (on) = +/- 10V	Isw	-	210	-	mA
Logic Input to Switch Output Isolation:						
+25°C	Vsw (T_{RING}, T_{TESTin}) = +/-320V Logic Inputs = Gnd	Isw	-	0.1	1	µA
+85°C	Vsw (T_{RING}, T_{TESTin}) = +/-330V Logic Inputs = Gnd	Isw	-	0.3	1	µA
-40°C	Vsw (T_{RING}, T_{TESTin}) = +/-310V Logic Inputs = Gnd	Isw	-	0.1	1	µA

Table 6. Ringing Test Switch SW8

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Off-state Leakage Current:						
+25°C	Vsw (differential)= -60V to +175V Vsw (differential)= +60V to -175V	Isw	-	.05	1	µA
+85°C	Vsw (differential)= -60V to +175V Vsw (differential)= +60V to -175V	Isw	-	0.1	1	µA
-40°C	Vsw (differential)= -60V to +175V Vsw (differential)= +60V to -175V	Isw	-	.05	1	µA
ON-resistance	Isw (on) = +/-70 mA, +/-80mA	Δ V	-	6	20	Ω
ON- voltage	Isw (on) = +/-1mA	-	-	0.75	1.5	V
Release Current	-	-	-	450	-	µA
Logic Input to Switch Output Isolation:						
+25°C	Vsw (R_{RING}, R_{TESTin}) = +/-320V Logic Inputs = Gnd	Isw	-	.05	1	µA
+85°C	Vsw (R_{RING}, R_{TESTin}) = +/-330V Logic Inputs = Gnd	Isw	-	0.1	1	µA
-40°C	Vsw (R_{RING}, R_{TESTin}) = +/-310V Logic Inputs = Gnd	Isw	-	.05	1	µA

* Choice of secondary protector and series current-limit resistor should ensure these ratings are not exceeded.

Table 7. Test in Switches, SW9 and SW10

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Off-state Leakage Current:						
+25°C	Vsw (differential)= -320V to Gnd Vsw (differential)= -60V to +260V	Isw	-	0.1	1	µA
+85°C	Vsw (differential)= -330V to Gnd Vsw (differential)= -60V to +270V	Isw	-	0.3	1	µA
-40°C	Vsw (differential)= -310V to Gnd Vsw (differential)= -60V to +250V	Isw	-	0.1	1	µA
RDS_{ON}:						
+25°C	Isw(on) = +/-5 mA, +/-10mA	Δ V	-	35	-	Ω
+85°C	Isw(on) = +/-5 mA, +/-10mA	Δ V	-	50	70	Ω
-40°C	Isw(on) = +/-5 mA, +/-10mA	Δ V	-	26	-	Ω
DC Current Limit:						
+25°C	Vsw (On) = +/-10V	Isw	-	160	-	mA
+85°C	Vsw (On) = +/-10V	Isw	80	110	-	mA
-40°C	Vsw (On) = +/-10V	Isw	-	210	250	mA
Logic Input to Switch Output Isolation:						
+25°C	Vsw (T_{TESTin}, R_{TESTin}) = +/-320V Logic Inputs = Gnd	Isw	-	0.1	1	µA
+85°C	Vsw (T_{TESTin}, R_{TESTin}) = +/-330V Logic Inputs = Gnd	Isw	-	0.3	1	µA
-40°C	Vsw (T_{TESTin}, R_{TESTin}) = +/-310V Logic Inputs = Gnd	Isw	-	0.1	1	µA

Table 8. Additional Electrical Characteristics

PARAMETERS	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Digital Input Characteristics						
Input Low Voltage	-	-	-	-	1.5	V
Input High Voltage	-	-	3.5	-	-	V
Input Leakage Current (High)	V_{DD} = 5.5V, V_{BAT} = -75V, V_{log} = 5V	I_{log}	-	0.1	1	µA
Input Leakage Current (Low)	V_{DD} = 5.5V, V_{BAT} = -75V, V_{log} = 0V	I_{log}	-	0.1	1	µA
Power Requirements						
Power Dissipation	V_{DD} = 5V, V_{BAT} = -48V,					
	Idle/Talk State or All Off State	I_{DD}, I_{BAT}	-	5.0	7.5	mW
	Ringing State or Test State	I_{DD}	-	6.0	10	mW
V_{DD} Current	V_{DD} = 5V,					
	Idle/Talk State or All Off State	I_{DD}	-	1.0	1.5	mA
	Ringing State or Test State	I_{DD}	-	1.2	1.9	mA
V_{BAT} Current	V_{BAT} = -48V,					
	Idle/Talk State or All Off State	I_{BAT}	-	4	10	µA
	Ringing State or Test State	I_{BAT}	-	4	10	µA
Temperature Shutdown Requirements[1]						
Shutdown Activation Temperature	-	-	110	125	150	°C
Shutdown Circuit Hysteresis	-	-	10	-	25	°C

[1] Temperature shutdown flag (TSD) will be high during normal operation and low during temperature shutdown state.

Table 9. Make-Before-Break Operation (Ringing to Idle/Talk Transition)

Ring	Testin	Testout	TSD	State	Timing	Break Switches 1 & 2	Ring Return Switch 3	Ring Access Switch 4	All Other Test Switches
5V	0V	0V	Float	Ringing	-	Open	Closed	Closed	Open
0V	0V	0V	Float	Make-before-break	SW4 waiting for next zero current crossing to turn off. Maximum time is half of ringing. In this transition state, current that is limited to the dc break switch current limit value will be sourced from the ring node of the SLIC	Closed	Open	Closed	Open
0V	0V	0V	Float	Idle / Talk	Zero cross current has occurred	Closed	Open	Open	Open

Table 10. Break-Before-Make Operation (Ringing to Idle/Talk Transition)

Ring	Testin	Testout	TSD	State	Timing	Break Switches 1 & 2	Ring Return Switch 3	Ring Access Switch 4	All Other Access Switches
5V	0V	0V	Float	Ringing	-	Open	Closed	Closed	Open
5V	0V	5V	Float	All Off	Hold this state for </= 25ms. SW4 waiting for zero current to turn off.	Open	Open	Closed	Open
5V	0V	5V	Float	All Off	Zero current has occurred. SW4 has opened.	Open	Open	Open	Open
0V	0V	0V	Float	Idle/Talk	Release Break Switches	Closed	Open	Open	Open

Alternate "Break-Before-Make" Operation

Note that the break-before-make operation can also be achieved using TSD as an input. In lines 2 & 3 of Table 10, instead of using the logic input pins to force the "all off" state, force TSD to ground. This will override the logic inputs and also force the all off state. Hold this state for 25 ms. During this 25 ms all off state, toggle the inputs from the 10 (ringing state) to 00 (idle/talk state). After 25 ms, release TSD to return switch control to the input pins which will set the idle talk state.

When using the CPC7583 in this mode, forcing TSD to ground will override the INPUT pins and force an all off state. Setting TSD to +5V will allow switch control via the logic INPUT pins. However, setting TSD to +5V will also disable the thermal shutdown mechanism. This is not recommended. Therefore, to allow switch control via the logic INPUT pins, allow TSD to float.

Thus when using TSD as an input, the two recommended states are 0 (overrides logic input pins and forces all off state) and float (allows switch control via logic input pins and thermal shutdown mechanism is active). This may require use of an open collector buffer.

Table 11. Electrical Specifications, Protection Circuitry

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Parameters Related to Diodes (in Diode Bridge)						
Voltage Drop @ Continuous Current (50/60 Hz)	Apply +/-dc current limit of break switches	Forward Voltage	-	2.8	3.5	V
Voltage Drop @ Surge Current	Apply +/-dynamic current limit of break swithces	Forward Voltage	-	5	-	V
Parameters Related to Protection SCR[1]						
Surge Current	-	-	-	-	*	A
Trigger Current (25˚C)	-	I_{TRIG}	-	60	-	mA
Hold Current (25˚C)	-	I_{HOLD}	-	110	-	mA
Trigger Current (85˚C)	-	I_{TRIG}	-	35	-	mA
Hold Current (85˚C)	-	I_{HOLD}	60	70	-	mA
Gate Trigger Voltage	Trigger Current	-	V_{BAT} - 4	-	V_{BAT} - 2	V
Reverse Leakage Current	V_{BAT}	-	-	-	1.0	µA
ON State Voltage[1]	0.5A t = 0.5 ms	V_{on}	-	-3	-	V
	2.0A t = 0.5 ms	-	-	-5	-	V

[1] Only for the CPC7583BA and CPC7583BC.
* Passes GR1089 and ITU-T K.20 with appropriate secondary protection in place.

Table 12. Truth Table for the CPC7583BA and CPC7583BB

INring	INtestin	INtestout	TSD	TESTin Switches	Break Switches	RingTest Switches	Ring Switches	TESTout Switches
0V	0V	0V	5V/Float[1]	Off	On	Off	Off	Off[3]
0V	0V	5V	5V/Float[1]	Off	Off	Off	Off	On[4]
0V	5V	0V	5V/Float[1]	On	Off	Off	Off	Off[5]
5V	0V	0V	5V/Float[1]	Off	Off	Off	On	Off[6]
5V	5V	0V	5V/Float[1]	Off	Off	On	Off	Off[7]
0V	5V	5V	5V/Float[1]	On	Off	Off	Off	On[8]
5V	0V	5V	5V/Float[1]	Off	Off	Off	Off	Off[9]
5V	5V	5V	5V/Float[1]	Off	Off	Off	Off	Off[9]
Don't Care	Don't Care	Don't Care	0V[2]	Off	Off	Off	Off	Off[9]

[1] If TSD = 5V, the thermal shutdown mechanism is disabled.
If TSD if floating, the thermal shutdown mechanism is active.
[2] Forcing TSD to ground overrides the logic input pins and forces an all off state.
[3] Idle/Talk State.
[4] TESTout state.
[5] TESTin state.
[6] Power Ringing State.
[7] Ringing generator test state.
[8] Simultaneous TESTout and TESTin state.
[9] All OFF State

A parallel in/parallel out data latch is integrated into the CPC7583. Operation of the data latch is controlled by the logic level input pin LATCH. The data input to the latch is the INPUT pin of the CPC7583 and the output of the data latch is an internal node used for state control.

When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly from INPUT, through the data latch to state control. Any changes in INPUT will be reflected in the state of the switches.

When the LATCH control pin is at logic 1, the data latch is active; the CPC7583 will no longer react to changes at the INPUT control pin. The state of the switches is now latched; that is, the state of the switches will remain as they were when the LATCH input transitioned from logic 0 to logic 1. The switches will not respond to changes in INPUT as long as LATCH is held high.

Note that the Tsd input is not tied to the data latch. Tsd is not affected by the LATCH input. Tsd input will override state control via INPUT and LATCH.

Table 13. Truth Table for the CPC7583BC and CPC7583BD

INring	INtestin	INtestout	TSD	TESTin Switches	Break Switches	RingTest Switches	Ring Switches	TESTout Switches
0V	0V	0V	5V/Float[1]	Off	On	Off	Off	Off[3]
0V	0V	5V	5V/Float[1]	Off	Off	Off	Off	On[4]
0V	5V	0V	5V/Float[1]	On	Off	Off	Off	Off[5]
5V	0V	0V	5V/Float[1]	Off	Off	Off	On	Off[6]
5V	5V	0V	5V/Float[1]	Off	Off	On	Off	Off[7]
0V	5V	5V	5V/Float[1]	On	Off	Off	Off	On[8]
5V	0V	5V	5V/Float[1]	Off	Off	Off	Off	Off[9]
5V	5V	5V	5V/Float[1]	Off	Off	On	Off	On[10]
Don't Care	Don't Care	Don't Care	0V[2]	Off	Off	Off	Off	Off[9]

[1] If TSD = 5V, the thermal shutdown mechanism is disabled.
If TSD if floating, the thermal shutdown mechanism is active.
[2] Forcing TSD to ground overrides the logic input pins and forces an all off state.
[3] Idle/Talk State.
[4] TESTout state.
[5] TESTin state.
[6] Power Ringing State.
[7] Ringing generator test state.
[8] Simultaneous TESTout and TESTin state.
[9] All OFF State
[10] Simultaneous TESTout - Ring Test state.

A parallel in/parallel out data latch is integrated into the CPC7583. Operation of the data latch is controlled by the logic level input pin LATCH. The data input to the latch is the INPUT pin of the CPC7583 and the output of the data latch is an internal node used for state control.

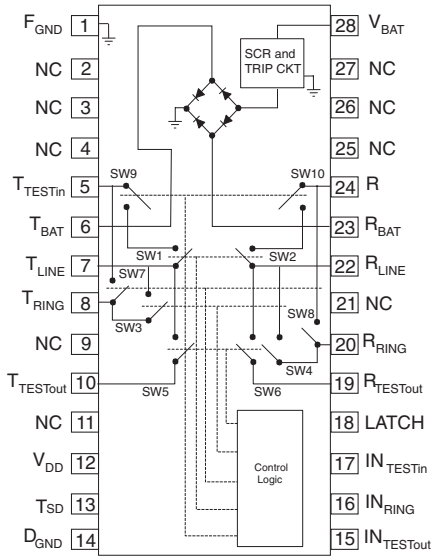
When the LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly from INPUT, through the data latch to state control. Any changes in INPUT will be reflected in the state of the switches.

When the LATCH control pin is at logic 1, the data latch is active; the CPC7583 will no longer react to changes at the INPUT control pin. The state of the switches is now latched; that is, the state of the switches will remain as they were when the LATCH input transitioned from logic 0 to logic 1. The switches will not respond to changes in INPUT as long as LATCH is held high.

Note that the Tsd input is not tied to the data latch. Tsd is not affected by the LATCH input. Tsd input will override state control via INPUT and LATCH.

Package Pinout

CPC7583



* Only the CPC7583BA and CPC7583BC contain the protection SCR

SOG	Symbol	Description
1	F_{GND}	Fault ground.
2	NC	No Connection.
3	NC	No Connection.
4	NC	No Connection.
5	T_{TESTin}	Test (in) access on TIP.
6	T_{BAT}	Connect to TIP on SLIC side.
7	T_{LINE}	Connect to TIP on line side.
8	T_{RING}	Connect to return ground for ringing generator.
9	NC	No connection.
10	$T_{TESTout}$	Test (out) access on TIP.
11	NC	No connection.
12	V_{DD}	5V supply
13	T_{SD}	Temperature shutdown pin. Can be used as a logic level input or an output. See Tables 9, 10, 12 and13 for more details. As an output, will read 5V when the device is in its operational mod and 0V in the thermal shutdown mode. To disable the thermal shutdown mode mechanism, tie this pin to 5V (not recommended).
14	D_{GND}	Digital ground
15	$IN_{TESTout}$	Logic level switch input control.
16	IN_{RING}	Logic level switch input control.
17	IN_{TESTin}	Logic level switch input control.
18	LATCH	Data input control, active-high, transparent low.
19	$R_{TESTout}$	Test (out) access on RING.
20	R_{RING}	Connect to ringing generator.
21	NC	No connection.
22	R_{LINE}	Connect to RING on line side.
23	R_{BAT}	Connect to RING on SLIC side.
24	R_{TESTin}	Test (in) access on RING.
25	NC	No connection.
26	NC	No connection.
27	NC	No connection
28	V_{BAT}	Battery voltage. Used as a reference for protection circuit.

Functional Description

Introduction

The CPC7583 has eight distinct states. Please consult the truth tables in table 12 and 13 for version differences.

- Idle/talk state (line break switches SW1, and SW2 closed). All other switches open.
- Ringing state, (ringing switches SW3, SW4 closed). All other switches open.
- Loop access (loop access switches SW5, SW6 closed). All other switches open.
- Ring generator test state (SW7, SW8 closed). All other switches open.
- SLIC test state Testin switches closed (SW9, SW10).
- Simultaneous Loop and SLIC access state. (SW9, SW10, SW5 and SW6 closed). All other switches open.
- Simultaneous test out and ring test (SW5, SW6, SW7, SW8 closed). All other switches open on the "BC" abd "BD" version.
- All Off state (all switches open).

The CPC7583 offers break-before-make and make-before-break switching with simple logic level input control. Solid state switch construction means no impulse noise is generated when switching during ring cadence or ring trip, thus eliminating the need for external "zero cross" switching circuitry. State control is via logic level input so no additional driver circuitry is required. The line break switches SW1 and SW2 are linear switches that have exceptionally low RDS_{ON} and excellent matching characteristics. The ringing access switch SW4 has a breakdown voltage rating of >480V which is sufficiently high, with proper protection, to prevent breakdown in the presence of a transient fault condition. (i.e., passing the transient on to the ring generator)

Integrated into the CPC7583 is a diode bridge clamping circuit, current limiting and thermal shutdown mechanism to provide protection to the SLIC device during a fault condition. Positive and negative surges are reduced by the current limiting circuitry and steered to ground via diodes. Power cross transients are also reduced by the current limiting and thermal shutdown circuits.

To protect the CPC7583 from an overvoltage fault condition, use of a secondary protector is required. The secondary protector must limit the voltage seen at the tip and ring terminals to a level below the max breakdown voltage of the switches. To minimize the stress on the solid-state contacts, use of a foldback or crowbar type secondary protector is recommended. With proper selection of the secondary protector, a line card using the CPC7583 will meet all relevant ITU, LSSGR, FCC or UL protection requirements.

The CPC7583 operates from a +5V supply only. This gives the device extremely low idle and active power dissipation and allows use with virtually any range of battery voltage. A battery voltage is also used by the CP7583 as a reference for the integrated protection circuit. In the event of a loss of battery voltage, the CPC7583 will enter an "all off" state.

Switch Timing

The CPC7583 provides, when switching from the ringing state to the idle/talk state, the ability to control the timing when the ringing access switches SW3 and SW4 are released relative to the state of the line break switches SW1 and SW2 using simple logic level input. This is referred to as a "make before break" or "break before make" operation. When the line break switch contacts (SW1, SW2) are closed (or made) before the ringing access switch contact (SW3, SW4) is opened (or broken), this is referred to a 'make-before-break' operation. Break-before-make operation occurs when the ringing access contact (SW3, SW4) is opened (broken) before the line break switch contacts (SW1, SW2) are closed (made). With the CPC7583 the "make before break" and "break before make" operations can easily be selected by applying logic level inputs to $IN_{TESTout}$, IN_{RING} and IN_{TESTin} of the device.

The logic sequences for either mode of operation are given in Tables 9 and 10. Logic states and explanations are given in Tables 12 and 13.

Break-before make operation can also be achieved using pin 13 (TSD) as an input. In table 10 lines 2 and 3 it is possible to induce the switches to "all off" by grounding pin 13 (TSD) instead of apply logic input to the pins. This has the effect of overriding the logic inputs and forcing the device to the "all off" state. Hold this input state for 25ms. During this hold period, toggle the inputs from the ringing state to the idle/talk state. After the 25ms release pin 13 (TSD) to return the switch control to the input $IN_{TESTout}$, IN_{RING}, IN_{TESTin} and reset the device to the idle/talk state.

Setting pin 13 (TSD) to +5V will allow switch control using the logic inputs. This setting, however, will also disable the thermal shutdown circuit and is therefore not recommended. When using logic controls via the input pins ($IN_{TESTout}$, IN_{RING} and IN_{TESTin}), pin 13 (TSD) should be allowed to float. As a result the two recommended states when using pin 13

(TSD) as a control are 0 which forces the device to the "all off state" or float which allow logic inputs to remain active. This may require use of an open collector buffer.

Ring Access Switch Zero Cross Current Turn Off

After the application of a logic input to turn SW4 off, the ring access switch is designed to delay the change in state until the next zero crossing. Once on, the switch requires a zero current cross to turn off and therefore should not be used to switch a pure DC signal. The switch will remain in the on state no matter what logic input until the next zero crossing. These switching characteristics will reduce and possibly eliminate overall system impulse noise normally associated with ringing access switches. The attributes of ringing access switch may make it possible to eliminate the need for a zero cross switching scheme. A minimum impedance of 300Ω in series with the ring generator is recommended.

Power Supplies

Both a +5V supply and battery voltage are connected to the CPC7583. CPC7583 switch state control is powered exclusively by the +5V supply. As a result, the CPC7583 exhibits extremely low power dissipation during both active and idle states.

Battery Voltage Monitor

The CPC7583 also uses the voltage reference to monitor battery voltage. If battery voltage is lost, the CPC7583 will immediately enter the "all off" state and remain in this state until the battery voltage is restored. The device will also enter the "all off" state if the battery voltage rises above –10V and will remain there until the battery voltage drops below –15V. This battery monitor feature draws a small current from the battery (<1μA) and will add slightly to the device's overall power dissipation.

Protection

Diode Bridge/SCR

The CPC7583 uses a combination of current limited break switches, a diode bridge/SCR clamping circuit and a thermal shutdown mechanism to protect the SLIC device or other associated circuitry from damage during line transient events such as lightning. During a positive transient condition, the fault current is conducted through the diode bridge and to ground. During a negative transient of two or four volts more negative than the battery, the SCR conducts and faults are shunted to ground via the SCR and diode bridge.

Also, in order for the SCR to crowbar or foldback, the on voltage (see Table 11) of the SCR must be less negative than the battery reference voltage. If the battery voltage is less negative the SCR on voltage, the SCR will not crowbar, however it will conduct fault currents to ground.

For power induction or power cross fault conditions, the positive cycle of the transient is clamped to the diode drop above ground and the fault current directed to ground. The negative cycle of the transient will cause the SCR to conduct when the voltage exceeds the battery reference voltage by two to four volts, steering the current to ground.

Current Limiting function

If a lightning strike transient occurs when the device in the talk/idle state, the current is passed along the line to the integrated protection circuitry and limited by the dynamic current limit response of break switches SW1 and SW2. When a 1000V 10x1000 pulse (LSSGR lightning) is applied to the line though a properly clamped external protector, the current seen at pins 6 (T_{BAT}) and pin 23 (R_{BAT}) will be a pulse with a typical magnitude and duration of 2.5A and < 0.5ms.

If a power cross fault occurs with device in the talk/idle state, the current is passed though the break switches SW1 and SW2 on to the integrated protection circuit and is limited by the dynamic DC current limit response of the two break switches. The DC current limit, specified over temperature, is between 80mA and 400mA and the circuitry has a negative temperature coefficient. As a result, if the device is subjected to extended heating due to power cross fault, the measured current at pin 6 (T_{BAT}) and pin 23 (R_{BAT}) will decrease as the device temperature increases. If the device temperature rises sufficiently, the temperature shutdown mechanism will activate and the device will default to the "all off" state.

Temperature Shutdown

The thermal shutdown mechanism will activate when the device temperature reaches a minimum of 110ϒC placing the device in the "all off" state regardless of logic input. During this thermal shutdown mode, pin 13 (TSD) will read 0V. Normal output of TSD is $+V_{DD}$.

If presented with a short duration transient such as a lightning event, the thermal shutdown feature will not typically activate. But in an extended power cross transient, the device temperature will rise and the thermal shutdown will activate forcing the switches to an "all off" state. At this point the current measured at pin 6 (T_{BAT}) and pin 23 (R_{BAT}) will drop to zero. Once the device enters thermal shutdown it will remain in the "all off" state until the temperature of the device drops below the activation level of the thermal shutdown circuit. This will return the device to the state prior to thermal shutdown. If the transient has not passed, current will flow at the value allowed by the dynamic DC current limiting of the switches and heating will begin again, reactivating the thermal shutdown mechanism. This cycle

of entering and exiting the thermal shutdown mode will continue as long as the fault condition persists. If the magnitude of the fault condition is great enough, the external secondary protector could activate and shunt all current to ground.

The thermal shutdown mechanism of the CPC7583 can be disable by applying $+V_{DD}$ to pin 13 (TSD)

External Protection Elements

The CPC7583 requires only one overvoltage secondary protector on the loop side of the device. The integrated protection feature described above negates the need for protection on the line side. The purpose of the secondary protector is to limit voltage transients to levels that do not exceed the breakdown voltage or input-output isolation barrier of the CPC7583. A foldback or crowbar type protector is recommended to minimize stresses on the device.

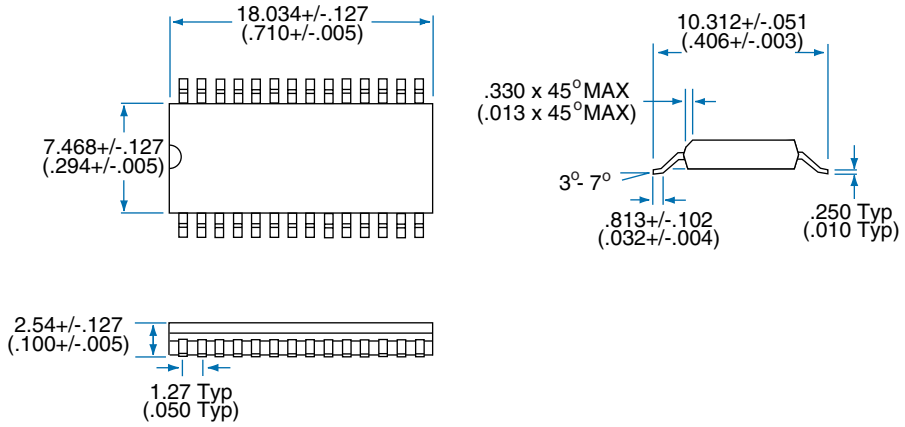
Consult Clare's app note, AN-100, "Designing Surge and Power Fault Protection Circuits for Solid State Subscriber Line Interfaces" for equations related to the specifications of external secondary protectors, fused resistors, and PTCs.

Data Latch

The CPC7583 has an integrated data latch. The latch operation is controlled by logic level input pin 18 (LATCH). The data input of the latch is pin 15 ($IN_{TESTout}$), pin 16 (IN_{RING}) and pin 17 (IN_{TESTin}) of the device while the output of the data latch is an internal node used for state control. When LATCH control pin is at logic 0, the data latch is transparent and data control signals flow directly through to state control. A change in input will be reflected in a change is switch state. When LATCH control pin is at logic 1, the data latch is now active and a change in input control will not affect switch state. The switches will remain in the position they were in when the LATCH changed from logic 0 to logic 1 and will not respond to changes in input as long as the latch is at logic 1. In addition, TSD input is not tied to the data latch. Therefore, TSD is not affected by the LATCH input and TSD input will override state control via pin 15 ($IN_{TESTout}$), pin 16 (IN_{RING}) and pin 17 (IN_{TESTin}) and the LATCH.

Mechanical Dimensions

28 Pin SOIC



Dimensions
mm
(Inches)

Notes:

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Specification: DS-CPC7583-RE

8/1/01