74HC4053; 74HCT4053

Triple 2-channel analog multiplexer/demultiplexer

Rev. 04 — 9 May 2006 Product data sheet

1. General description

The 74HC4053; 74HCT4053 is a high-speed Si-gate CMOS device and is pin compatible with the HEF4053B. It is specified in compliance with JEDEC standard no. 7A.

The 74HC4053; 74HCT4053 is triple 2-channel analog multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (nY0 and nY1), a common input/output (nZ) and three digital select inputs (Sn).

With $\overline{E}$ LOW, one of the two switches is selected (low-impedance ON-state) by S1 to S3. With $\overline{E}$ HIGH, all switches are in the high-impedance OFF-state, independent of S1 to S3.

V_{CC} and GND are the supply voltage pins for the digital control inputs (S1 to S3 and $\overline{E}$). The V_{CC} to GND ranges are 2.0 V to 10.0 V for 74HC4053 and 4.5 V to 5.5 V for 74HCT4053. The analog inputs/outputs (nY0 and nY1, and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit. $V_{CC} - V_{EE}$ may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND (typically ground).

2. Features

- Low ON resistance:
  - 80 Ω (typical) at $V_{CC} - V_{EE}$ = 4.5 V
  - 70 Ω (typical) at $V_{CC} - V_{EE}$ = 6.0 V
  - 60 Ω (typical) at $V_{CC} - V_{EE}$ = 9.0 V
- Logic level translation:
  - To enable 5 V logic to communicate with ±5 V analog signals
- Typical ‘break before make’ built in
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

PHILIPS

3. Applications

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

4. Quick reference data

Table 1: Quick reference data

V_{EE} = GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
74HC4053							
t_{PZH}, t_{PZL}	turn-ON time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V					
	$\overline{E}$ to V_{os}			-	17	-	ns
	Sn to V_{os}			-	21	-	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V					
	$\overline{E}$ to V_{os}			-	18	-	ns
	Sn to V_{os}			-	17	-	ns
C_i	input capacitance			-	3.5	-	pF
C_S	switch capacitance						
	independent I/O (nYn)			-	5	-	pF
	common I/O (nZ)			-	8	-	pF
C_{PD}	power dissipation capacitance	per switch; V_I = GND to V_{CC}	[1]	-	36	-	pF
74HCT4053							
t_{PZH}, t_{PZL}	turn-ON time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V					
	$\overline{E}$ to V_{os}			-	23	-	ns
	Sn to V_{os}			-	21	-	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V					
	$\overline{E}$ to V_{os}			-	20	-	ns
	Sn to V_{os}			-	19	-	ns
C_i	input capacitance			-	3.5	-	pF
C_S	switch capacitance						
	independent I/O (nYn)			-	5	-	pF
	common I/O(nZ)			-	8	-	pF
C_{PD}	power dissipation capacitance	per switch; V_I = GND to (V_{CC} − 1.5 V)	[1]	-	36	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;
C_S = maximum switch capacitance in pF;
V_{CC} = supply voltage in V.

5. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4053				
74HC4053N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-4
74HC4053D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4053DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4053PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4053BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4053				
74HCT4053N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-4
74HCT4053D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4053DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HCT4053PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4053BQ	–40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

6. Functional diagram

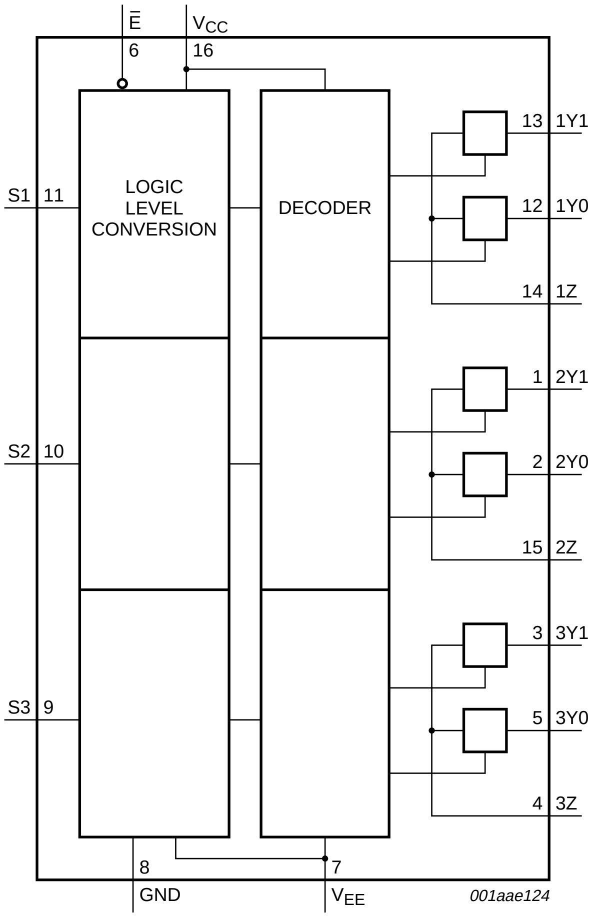


Fig 1. Functional diagram

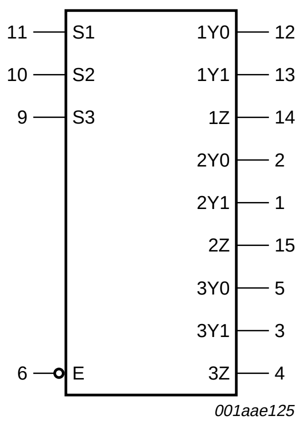


Fig 2. Logic symbol

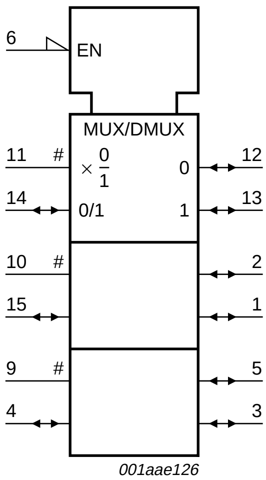


Fig 3. IEC logic symbol

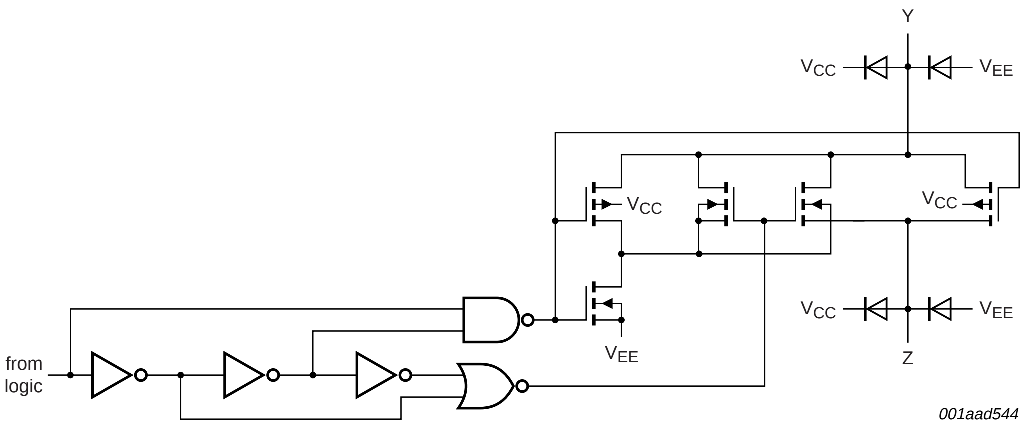


Fig 4. Schematic diagram (one switch)

7. Pinning information

7.1 Pinning

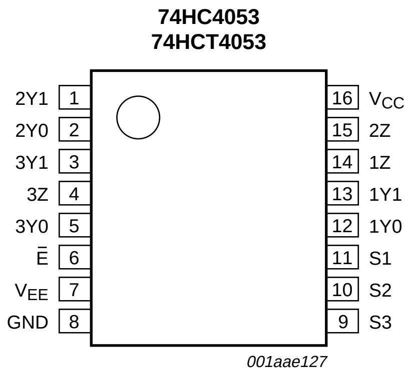
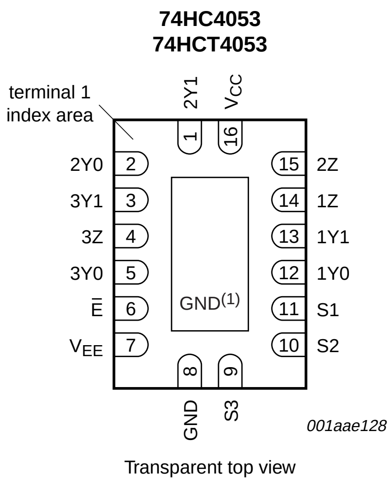


Fig 5. Pin configuration DIP16, SO16 and (T)SSOP16



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input.

Fig 6. Pin configuration DHVQFN16

7.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
2Y1	1	2 independent input/output 1
2Y0	2	2 independent input/output 0
3Y1	3	3 independent input/output 1
3Z	4	3 common input/output
3Y0	5	3 independent input/output 0
$\overline{E}$	6	enable input (active LOW)
V_{EE}	7	negative supply voltage
GND	8	ground (0 V)
S3	9	select input 3
S2	10	select input 2
S1	11	select input 1
1Y0	12	1 independent input/output 0
1Y1	13	1 independent input/output 1
1Z	14	1 common input/output
2Z	15	2 common input/output
V_{CC}	16	supply voltage

8. Functional description

8.1 Function table

Table 4: Function table [1]

Control		Channel on
$\overline{E}$	Sn	
L	L	nY0 to nZ
	H	nY1 to nZ
H	X	none

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

9. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{EE} = GND (ground = 0 V). [1]

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+11.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{SK}	switch clamping current	$V_S < -0.5$ V or $V_S > V_{CC} + 0.5$ V	-	±20	mA

Table 5: Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{EE} = GND (ground = 0 V). [1]

Symbol	Parameter	Conditions		Min	Max	Unit
I_S	switch current	$-0.5 V < V_S < V_{CC} + 0.5 V$		-	±25	mA
I_{EE}	negative supply current			-	–20	mA
I_{CC}	quiescent supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to + 125 °C				
	DIP16 package		[2]	-	750	mW
	SO16 package		[3]	-	500	mW
	SSOP16 package		[4]	-	500	mW
	TSSOP16 package		[4]	-	500	mW
	DHVQFN16 package		[5]	-	500	mW
P_S	power dissipation per switch			-	100	mW

[1] To avoid drawing V_{CC} current out of terminals nZ, when switch current flows in terminals nYn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminals nZ, no V_{CC} current will flow out of terminals nYn. In this case there is no limit for the voltage drop across the switch, but the voltages at nYn and nZ may not exceed V_{CC} or V_{EE}.

[2] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

[5] For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

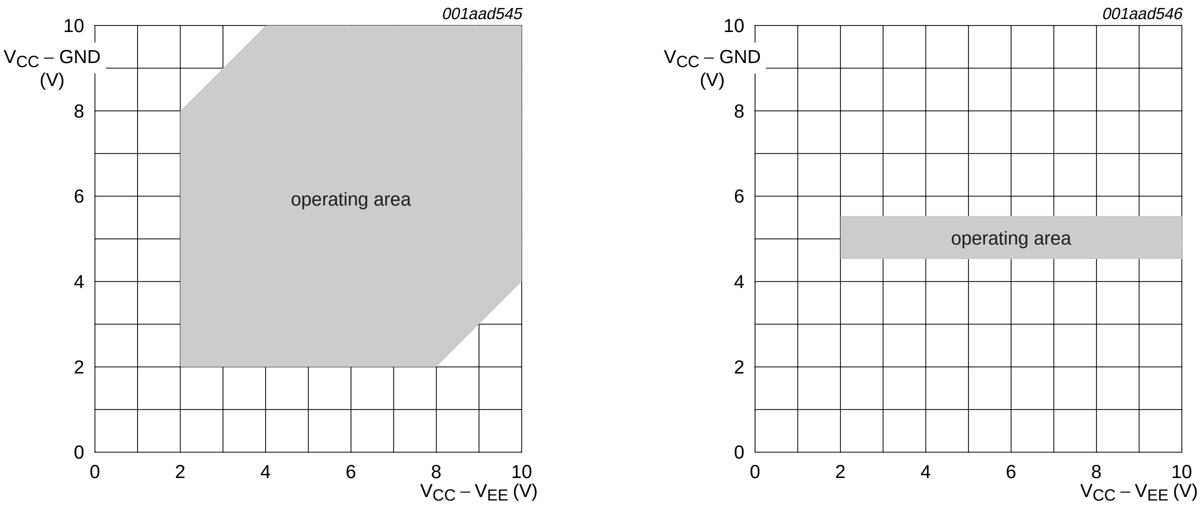
10. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74HC4053						
ΔV_{CC}	supply voltage difference	see Figure 7				
	V_{CC} – GND		2.0	5.0	10.0	V
	$V_{CC} - V_{EE}$		2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	V
V_S	switch voltage		V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	-	6.0	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	6.0	400	ns
		V_{CC} = 10.0 V	-	6.0	250	ns
74HCT4053						
ΔV_{CC}	supply voltage difference	see Figure 7				
	V_{CC} – GND		4.5	5.0	5.5	V
	$V_{CC} - V_{EE}$		2.0	5.0	10.0	V

Table 6: Recommended operating conditions *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	input voltage		GND	-	V_{CC}	V
V_S	switch voltage		V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 4.5 V	-	6.0	500	ns



a. Type 74HC4053

b. Type 74HCT4053

Fig 7. Guaranteed operating area as a function of the supply voltages

11. Static characteristics

Table 7: R_{ON} resistance per switch 74HC4053 and 74HCT4053

For test circuit see Figure 8.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

74HC4053 supply voltages: V_{CC} – GND or V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

74HCT4053 supply voltages: V_{CC} – GND = 4.5 V or 5.5 V; V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
$R_{ON(peak)}$	ON resistance (peak)	V_{is} = V_{CC} to V_{EE}; V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA [1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA	-	100	180	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA	-	90	160	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA	-	70	130	Ω

Table 7: R_{ON} resistance per switch 74HC4053 and 74HCT4053 *…continued*

For test circuit see Figure 8.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

74HC4053 supply voltages: V_{CC} – GND or V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

74HCT4053 supply voltages: V_{CC} – GND = 4.5 V or 5.5 V; V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$; $V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	80	140	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	70	120	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	60	105	Ω
		$V_{is} = V_{CC}$; $V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	150	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	90	160	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	80	140	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	65	120	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to V_{EE}; $V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V; V_{EE} = 0 V	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V		-	9	-	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V		-	8	-	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	6	-	Ω
T_{amb} = –40 °C to +85 °C							
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE}; $V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	225	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	200	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	165	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$; $V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	175	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	150	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	130	Ω
		$V_{is} = V_{CC}$; $V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	200	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S= 1000 μA		-	-	175	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	150	Ω
T_{amb} = –40 °C to +125 °C							
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE}; $V_I = V_{IH}$ or V_{IL}					
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA	[1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	270	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA		-	-	240	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA		-	-	195	Ω

Table 7: R_{ON} resistance per switch 74HC4053 and 74HCT4053 *…continued*

For test circuit see Figure 8.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

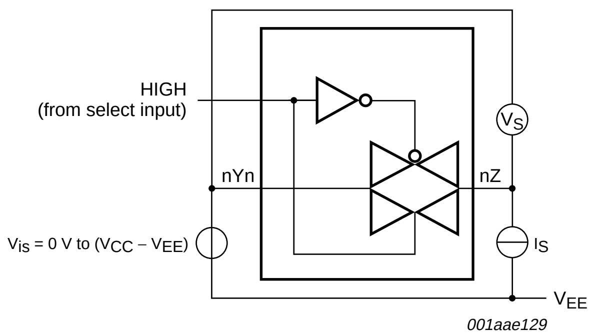
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

74HC4053 supply voltages: V_{CC} – GND or V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

74HCT4053 supply voltages: V_{CC} – GND = 4.5 V or 5.5 V; V_{CC} – V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

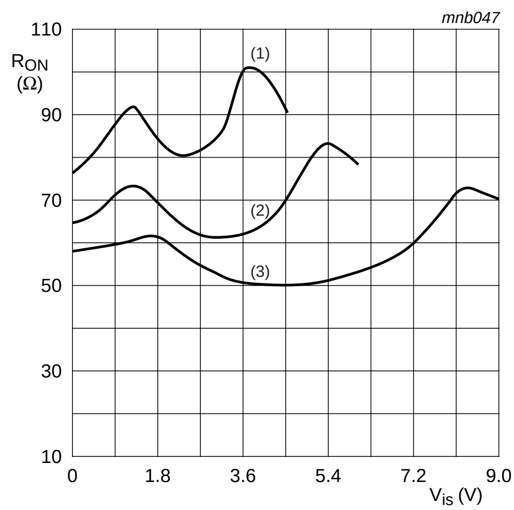
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$; $V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA [1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA	-	-	210	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA	-	-	180	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA	-	-	160	Ω
		$V_{is} = V_{CC}$; $V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_S = 100 μA [1]	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_S = 1000 μA	-	-	240	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_S = 1000 μA	-	-	210	Ω
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; I_S = 1000 μA	-	-	180	Ω

[1] At supply voltages (V_{CC} – V_{EE}) approaching 2.0 V the analog switch ON resistance becomes extremely non-linear. Therefore, it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.



$R_{ON} = V_S / I_S$.

Fig 8. Test circuit for measuring R_{ON}



V_{is} = 0 V to (V_{CC} – V_{EE}).

(1) V_{CC} = 4.5 V

(2) V_{CC} = 6 V

(3) V_{CC} = 9 V

Fig 9. Typical R_{ON} as a function of input voltage V_{is}

Table 8: Static characteristics 74HC4053

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
		V_{CC} = 9.0 V	6.3	4.7	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
		V_{CC} = 9.0 V	-	4.3	2.7	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{EE} = 0 V				
		V_{CC} = 6.0 V	-	-	±0.1	µA
		V_{CC} = 10.0 V	-	-	±0.2	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} – V_{EE}; see Figure 10				
		per channel	-	-	±0.1	µA
		all channels	-	-	±0.1	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} – V_{EE}; see Figure 11	-	-	±0.1	µA
I_{CC}	quiescent supply current	V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}; V_I = V_{CC} or GND; V_{EE} = 0 V				
		V_{CC} = 6.0 V	-	-	8.0	µA
		V_{CC} = 10.0 V	-	-	16.0	µA
C_i	input capacitance		-	3.5	-	pF
C_S	switch capacitance					
	independent I/O (nYn)		-	5	-	pF
	common I/O (nZ)		-	8	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
		V_{CC} = 9.0 V	6.3	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
		V_{CC} = 9.0 V	-	-	2.7	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{EE} = 0 V				
		V_{CC} = 6.0 V	-	-	±1.0	µA
		V_{CC} = 10.0 V	-	-	±2.0	µA

Table 8: Static characteristics 74HC4053 *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} – V_{EE}; see Figure 10				
		per channel	-	-	±1.0	μA
		all channels	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} – V_{EE}; see Figure 11	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}; V_I = V_{CC} or GND; V_{EE} = 0 V				
		V_{CC} = 6.0 V	-	-	80.0	μA
		V_{CC} = 10.0 V	-	-	160.0	μA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
		V_{CC} = 9.0 V	6.3	-	-	V
V_{IL}	LOW-state input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
		V_{CC} = 9.0 V	-	-	2.7	V
I_{LI}	input leakage current	V_I = V_{CC} or GND; V_{EE} = 0 V				
		V_{CC} = 6.0 V	-	-	±1.0	μA
		V_{CC} = 10.0 V	-	-	±2.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} – V_{EE}; see Figure 10				
		per channel	-	-	±1.0	μA
		all channels	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\|V_S\|$ = V_{CC} – V_{EE}; see Figure 11	-	-	±1.0	μA
I_{CC}	quiescent supply current	V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}; V_I = V_{CC} or GND; V_{EE} = 0 V				
		V_{CC} = 6.0 V	-	-	160.0	μA
		V_{CC} = 10.0 V	-	-	320.0	μA

Table 9: Static characteristics 74HCT4053

Voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	μA
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	μA

Table 9: Static characteristics 74HCT4053 *…continued*

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_{EE} = 0 V; V_I = V_{CC} or GND	-	-	±0.1	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\lvert V_S \rvert$ = V_{CC} – V_{EE}; see Figure 10				
		per channel	-	-	±0.1	µA
		all channels	-	-	±0.1	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\lvert V_S \rvert$ = V_{CC} – V_{EE}; see Figure 11	-	-	±0.1	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	8.0	µA
		V_{CC} = 5.0 V; V_{EE} = –5.0 V	-	-	16.0	µA
ΔI_{CC}	additional quiescent supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V; V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND	-	50	180	µA
C_i	input capacitance		-	3.5	-	pF
C_S	switch capacitance					
	independent I/O (nYn)		-	5	-	pF
	common I/O (nZ)		-	8	-	pF
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	µA
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	µA
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_{EE} = 0 V; V_I = V_{CC} or GND	-	-	±1.0	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\lvert V_S \rvert$ = V_{CC} – V_{EE}; see Figure 10				
		per channel	-	-	±1.0	µA
		all channels	-	-	±1.0	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_I = V_{IH} or V_{IL}; V_{EE} = 0 V; $\lvert V_S \rvert$ = V_{CC} – V_{EE}; see Figure 11	-	-	±1.0	µA
I_{CC}	quiescent supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	80.0	µA
		V_{CC} = 5.0 V; V_{EE} = –5.0 V	-	-	160.0	µA
ΔI_{CC}	additional quiescent supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V; V_I = V_{CC} – 2.1 V; other inputs at V_{CC} or GND	-	-	225	µA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-state input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	µA
V_{IL}	LOW-state input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	µA
I_{LI}	input leakage current	V_{CC} = 5.5 V; V_{EE} = 0 V; V_I = V_{CC} or GND	-	-	±1.0	µA

Table 9: Static characteristics 74HCT4053 *...continued*

Voltages are referenced to GND (ground = 0 V).

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; $V_I = V_{IH}$ or V_{IL}; V_{EE} = 0 V; $\lvert V_S \rvert = V_{CC} - V_{EE}$; see Figure 10				
		per channel	-	-	±1.0	μA
		all channels	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; $V_I = V_{IH}$ or V_{IL}; V_{EE} = 0 V; $\lvert V_S \rvert = V_{CC} - V_{EE}$; see Figure 11	-	-	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	160.0	μA
		V_{CC} = 5.0 V; V_{EE} = –5.0 V	-	-	320.0	μA
ΔI_{CC}	additional quiescent supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND	-	-	245	μA

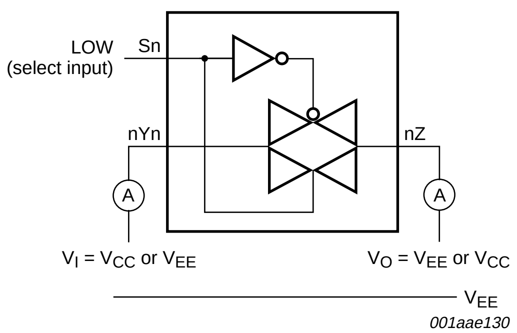


Fig 10. Test circuit for measuring OFF-state leakage current

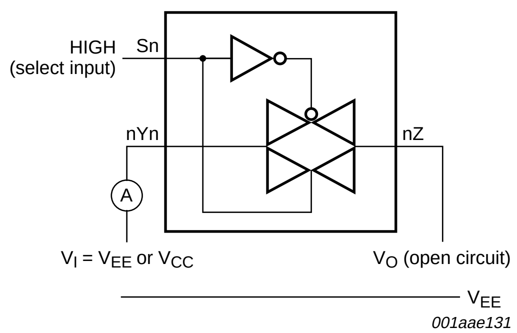


Fig 11. Test circuit for measuring ON-state leakage current

12. Dynamic characteristics

Table 10: Dynamic characteristics type 74HC4053

Voltages are referenced to GND (ground = 0 V); $t_r = t_f$ = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 14.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	$R_L = \infty\ \Omega$; see Figure 12				
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	15	60	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	5	12	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	4	10	ns
		V_{CC} = 4.5 V; V_{EE} = –4.5 V	-	4	8	ns

Table 10: Dynamic characteristics type 74HC4053 *...continued*

Voltages are referenced to GND (ground = 0 V); $t_r = t_f = 6$ ns; $C_L = 50$ pF unless otherwise specified; for test circuit see Figure 14.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{PZH}, t_{PZL}	turn-ON time	$R_L = 1\ k\Omega$; see Figure 13					
	$\overline{E}$ to V_{os}	$V_{CC} = 2.0$ V; $V_{EE} = 0$ V		-	60	220	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V		-	20	44	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V		-	16	37	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V		-	15	31	ns
		$V_{CC} = 5$ V; $V_{EE} = 0$ V; $C_L = 15$ pF		-	17	-	ns
	Sn to V_{os}	$V_{CC} = 2.0$ V; $V_{EE} = 0$ V		-	75	220	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V		-	25	44	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V		-	20	37	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V		-	15	31	ns
		$V_{CC} = 5$ V; $V_{EE} = 0$ V; $C_L = 15$ pF		-	21	-	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	$R_L = 1\ k\Omega$; see Figure 13					
	$\overline{E}$ to V_{os}	$V_{CC} = 2.0$ V; $V_{EE} = 0$ V		-	63	210	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V		-	21	42	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V		-	17	36	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V		-	15	29	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF		-	18	-	ns
	Sn to V_{os}	$V_{CC} = 2.0$ V; $V_{EE} = 0$ V		-	60	210	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V		-	20	42	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V		-	16	36	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V		-	15	29	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF		-	17	-	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to V_{CC}	[1]	-	36	-	pF
T_{amb} = −40 °C to +85 °C							
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	$R_L = \infty\ \Omega$; see Figure 12					
		$V_{CC} = 2.0$ V; $V_{EE} = 0$ V		-	-	75	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V		-	-	15	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V		-	-	13	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V		-	-	10	ns

Table 10: Dynamic characteristics type 74HC4053 *...continued*

Voltages are referenced to GND (ground = 0 V); t_r = t_f = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 14.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PZH}, t_{PZL}	turn-ON time	R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	275	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	55	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	47	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	-	39	ns
	Sn to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	275	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	55	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	47	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	-	39	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	265	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	53	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	45	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	-	36	ns
	Sn to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	265	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	53	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	45	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	-	36	ns
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	R_L = ∞ Ω; see Figure 12				
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	90	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	18	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	15	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	-	12	ns
t_{PZH}, t_{PZL}	turn-ON time	R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	330	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	66	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	56	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	-	47	ns
	Sn to V_{os}	V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	330	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	-	66	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	56	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	-	47	ns

Table 10: Dynamic characteristics type 74HC4053 *...continued*

Voltages are referenced to GND (ground = 0 V); $t_r = t_f = 6$ ns; $C_L = 50$ pF unless otherwise specified; for test circuit see Figure 14.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	turn-OFF time	$R_L = 1$ kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	$V_{CC} = 2.0$ V; $V_{EE} = 0$ V	-	-	315	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	-	63	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V	-	-	54	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	-	44	ns
	Sn to V_{os}	$V_{CC} = 2.0$ V; $V_{EE} = 0$ V	-	-	315	ns
		$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	-	63	ns
		$V_{CC} = 6.0$ V; $V_{EE} = 0$ V	-	-	54	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	-	44	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_S = maximum switch capacitance in pF;

V_{CC} = supply voltage in V.

Table 11: Dynamic characteristics type 74HCT4053

Voltages are referenced to GND (ground = 0 V); $t_r = t_f = 6$ ns; $C_L = 50$ pF unless otherwise specified; for test circuit see Figure 14.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = 25$ °C						
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	$V_{CC} = 4.5$ V; $R_L = \infty$ Ω; see Figure 12				
		$V_{EE} = 0$ V	-	5	12	ns
		$V_{EE} = -4.5$ V	-	4	8	ns
t_{PZH}, t_{PZL}	turn-ON time	$R_L = 1$ kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	27	48	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	16	34	ns
		$V_{CC} = 5$ V; $V_{EE} = 0$ V; $C_L = 15$ pF	-	23	-	ns
	Sn to V_{os}	$V_{CC} = 4.5$ V; $V_{EE} = 0$ V	-	25	48	ns
		$V_{CC} = 4.5$ V; $V_{EE} = -4.5$ V	-	16	34	ns
		$V_{CC} = 5$ V; $V_{EE} = 0$ V; $C_L = 15$ pF	-	21	-	ns

Table 11: Dynamic characteristics type 74HCT4053 *…continued*

Voltages are referenced to GND (ground = 0 V); t_r = t_f = 6 ns; C_L = 50 pF unless otherwise specified; for test circuit see Figure 14.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	turn-OFF time	R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{CC} = 4.5 V; V_{EE} = 0 V	-	24	44	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	15	31	ns
		V_{CC} = 5 V; V_{EE} = 0 V; C_L = 15 pF	-	20	-	ns
	Sn to V_{os}	V_{CC} = 4.5 V; V_{EE} = 0 V	-	22	44	ns
		V_{CC} = 4.5 V; V_{EE} = −4.5 V	-	15	31	ns
		V_{CC} = 5 V; V_{EE} = 0 V; C_L = 15 pF	-	19	-	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to (V_{CC} − 1.5 V) [1]	-	36	-	pF
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	V_{CC} = 4.5 V; R_L = ∞ Ω; see Figure 12				
		V_{EE} = 0 V	-	-	15	ns
		V_{EE} = −4.5 V	-	-	10	ns
t_{PZH}, t_{PZL}	turn-ON time	V_{CC} = 4.5 V; R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{EE} = 0 V	-	-	60	ns
		V_{EE} = −4.5 V	-	-	43	ns
	Sn to V_{os}	V_{EE} = 0 V	-	-	60	ns
		V_{EE} = −4.5 V	-	-	43	ns
t_{PHZ}, t_{PLZ}	turn-OFF time	V_{CC} = 4.5 V; R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{EE} = 0 V	-	-	55	ns
		V_{EE} = −4.5 V	-	-	39	ns
	Sn to V_{os}	V_{EE} = 0 V	-	-	55	ns
		V_{EE} = −4.5 V	-	-	39	ns
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay V_{is} to V_{os}	V_{CC} = 4.5 V; R_L = ∞ Ω; see Figure 12				
		V_{EE} = 0 V	-	-	18	ns
		V_{EE} = −4.5 V	-	-	12	ns
t_{PZH}, t_{PZL}	turn-ON time	V_{CC} = 4.5 V; R_L = 1 kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	V_{EE} = 0 V	-	-	72	ns
		V_{EE} = −4.5 V	-	-	51	ns
	Sn to V_{os}	V_{EE} = 0 V	-	-	72	ns
		V_{EE} = −4.5 V	-	-	51	ns

Table 11: Dynamic characteristics type 74HCT4053 *...continued*

Voltages are referenced to GND (ground = 0 V); $t_r = t_f = 6$ ns; $C_L = 50$ pF unless otherwise specified; for test circuit see Figure 14.

V_{is} is the input voltage at a nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at a nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHZ}, t_{PLZ}	turn-OFF time	$V_{CC} = 4.5$ V; $R_L = 1$ kΩ; see Figure 13				
	$\overline{E}$ to V_{os}	$V_{EE} = 0$ V	-	-	66	ns
		$V_{EE} = -4.5$ V	-	-	47	ns
	Sn to V_{os}	$V_{EE} = 0$ V	-	-	66	ns
		$V_{EE} = -4.5$ V	-	-	47	ns

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

$\Sigma\{(C_L + C_S) \times V_{CC}^2 \times f_o\}$ = sum of outputs;

C_L = output load capacitance in pF;

C_S = maximum switch capacitance in pF;

V_{CC} = supply voltage in V.

13. Waveforms

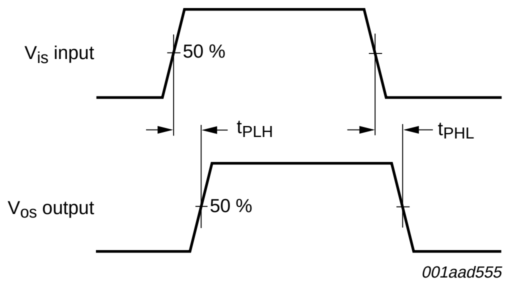
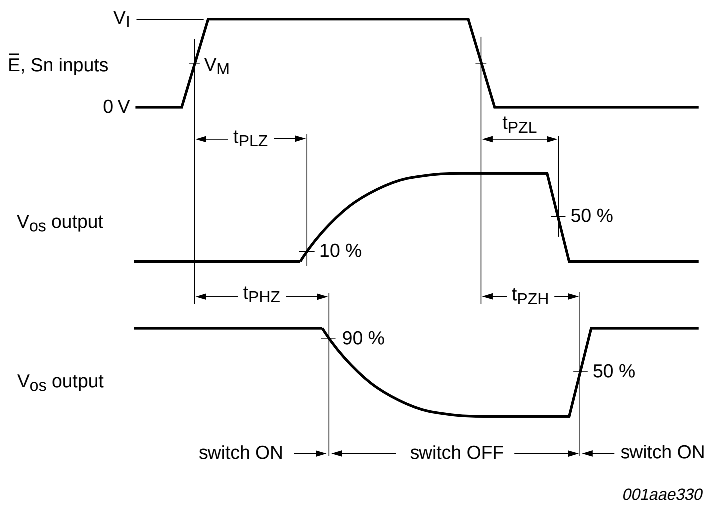


Fig 12. Propagation delay input (V_{is}) to output (V_{os})

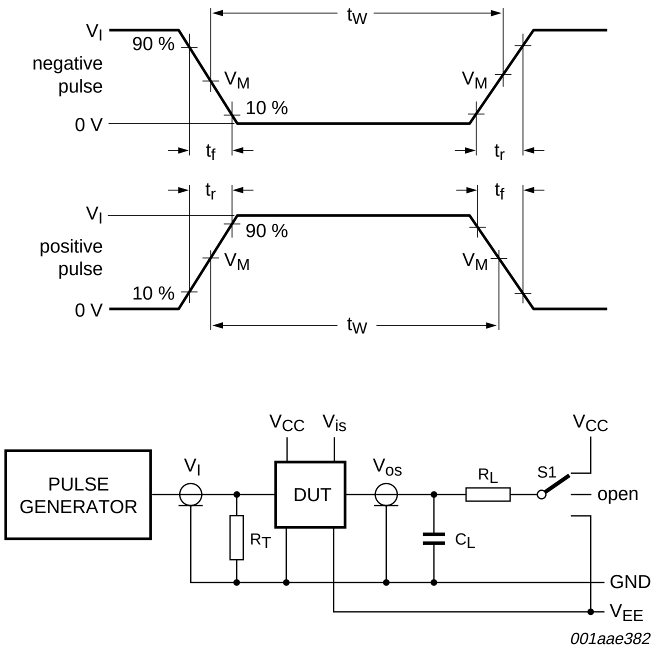


(1) Measurement points are given in Table 12.

Fig 13. Turn-ON and turn-OFF times

Table 12: Measurement points

Type	Input
	V_M
74HC4053	$0.5V_{CC}$
74HCT4053	1.3 V



Test data is given in Table 13.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

S1 = Test selection switch.

Fig 14. Load circuitry for switching times

Table 13: Test data

Test	Input				Load		S1 position
	V_I	V_{is}	t_r, t_f		C_L	R_L	
			at f_{max}	other			
t_{PHL}, t_{PLH}	[1]	pulse	< 2 ns	6 ns	15 pF, 50 pF	1 kΩ	open
t_{PZH}, t_{PHZ}	[1]	V_{CC}	< 2 ns	6 ns	15 pF, 50 pF	1 kΩ	V_{EE}
t_{PZL}, t_{PLZ}	[1]	V_{EE}	< 2 ns	6 ns	15 pF, 50 pF	1 kΩ	V_{CC}

[1] V_I values:

a) For 74HC4053: $V_I = V_{CC}$.

b) For 74HCT4053: V_I = 3 V.

14. Additional dynamic characteristics

Table 14: Additional dynamic characteristics 74HC4053 and 74HCT4053

GND = 0 V; T_{amb} = 25 °C.

V_{is} is the input voltage at an nYn or nZ terminal, whichever is assigned as an input.

V_{os} is the output voltage at an nYn or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
d_{sin}	sine wave distortion	R_L = 10 kΩ; C_L = 50 pF; see Figure 15					
		f_i = 1 kHz					
		V_{CC} = 2.25 V; V_{EE} = –2.25 V; V_{is} = 4.0 V (p-p)		-	0.04	-	%
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; V_{is} = 8.0 V (p-p)		-	0.02	-	%
		f_i = 10 kHz					
		V_{CC} = 2.25 V; V_{EE} = –2.25 V; V_{is} = 4.0 V (p-p)		-	0.12	-	%
		V_{CC} = 4.5 V; V_{EE} = –4.5 V; V_{is} = 8.0 V (p-p)		-	0.06	-	%
$\alpha_{(OFF)(ft)}$	OFF-state feed-through attenuation	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 16	[1]				
		V_{CC} = 2.25 V; V_{EE} = –2.25 V		-	–50	-	dB
		V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	–50	-	dB
$V_{ct(sw-sw)}$	crosstalk between switches	R_L = 600 Ω; C_L = 50 pF; f_i = 1 MHz; see Figure 17	[1]				
		V_{CC} = 2.25 V; V_{EE} = –2.25 V		-	–60	-	dB
		V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	–60	-	dB
$V_{ct(d-sw)}$	crosstalk between digital inputs and switch	V_{CC} = 4.5 V; R_L = 600 kΩ; C_L = 50 pF; f_i = 1 MHz; see Figure 18	[2]				
		V_{EE} = 0 V		-	110	-	mV
		V_{EE} = –4.5 V		-	220	-	mV
$f_{(-3dB)}$	–3 dB frequency response	R_L = 50 Ω; C_L = 10 pF; see Figure 19	[3]				
		V_{CC} = 2.25 V; V_{EE} = –2.25 V		-	160	-	MHz
		V_{CC} = 4.5 V; V_{EE} = –4.5 V		-	170	-	MHz

[1] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

[2] Control input $\overline{E}$ or Sn, with square-wave between V_{CC} and GND.

[3] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).

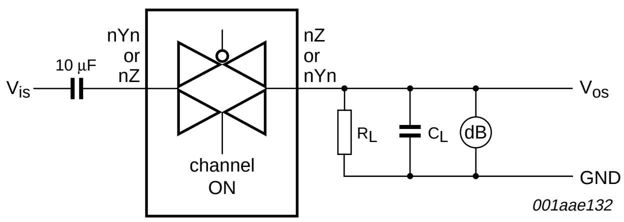
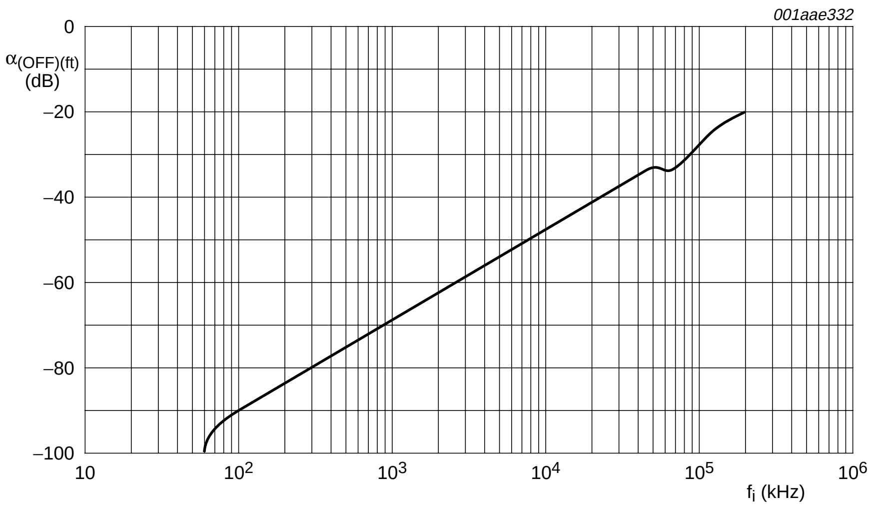
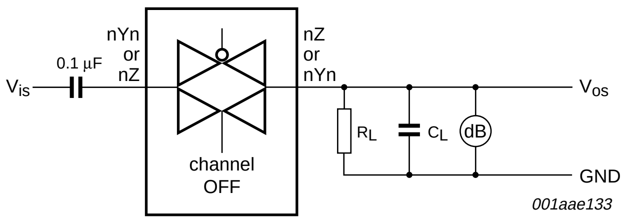


Fig 15. Test circuit for measuring sine wave distortion

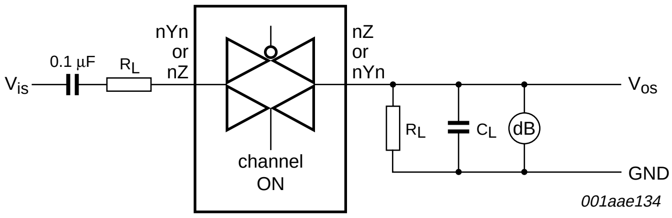


a. Feed-through as function of the frequency

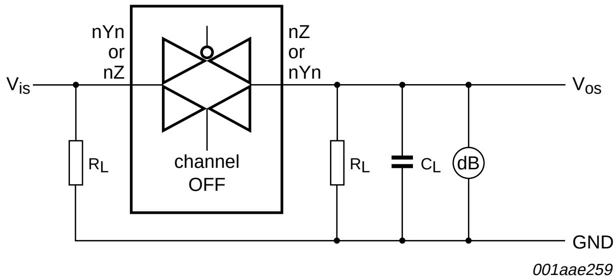


b. Test circuit

Fig 16. Typical switch OFF signal feed-through as a function of frequency



a. Switch ON



b. Switch OFF

Fig 17. Test circuits for measuring crosstalk between any two switches

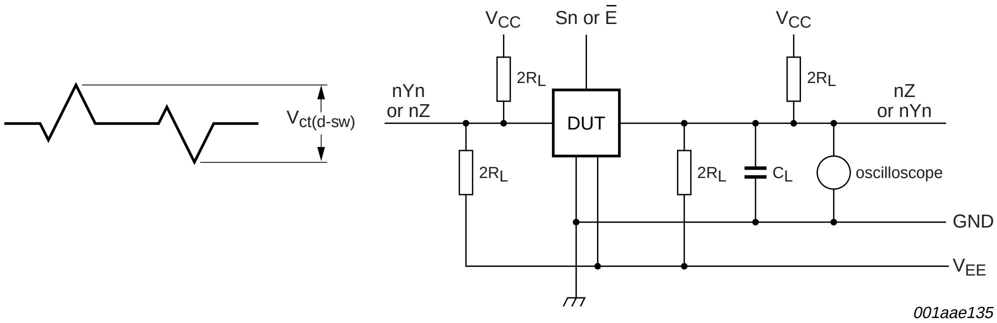
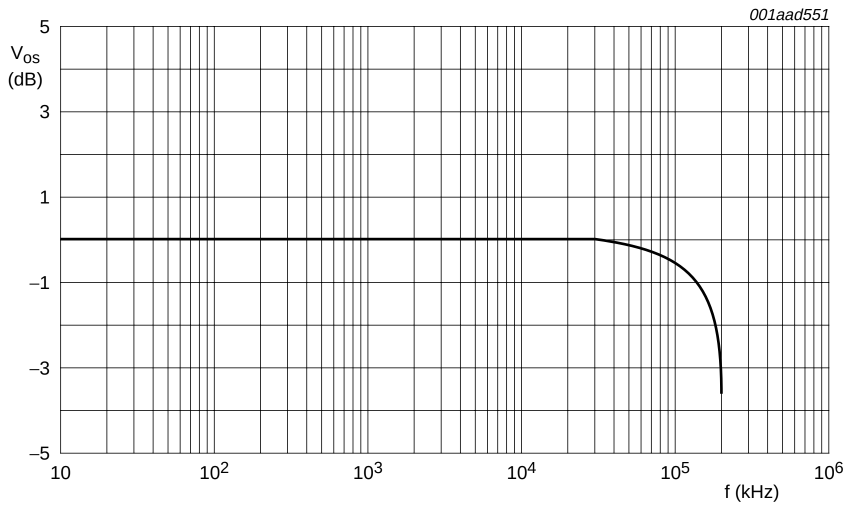
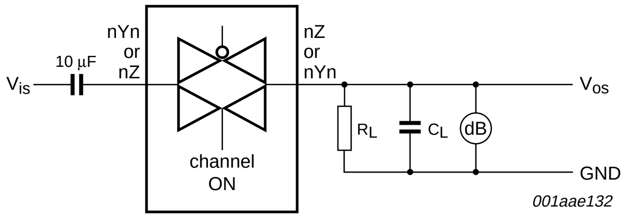


Fig 18. Test circuit for measuring crosstalk between digital inputs and switch



a. Typical frequency response

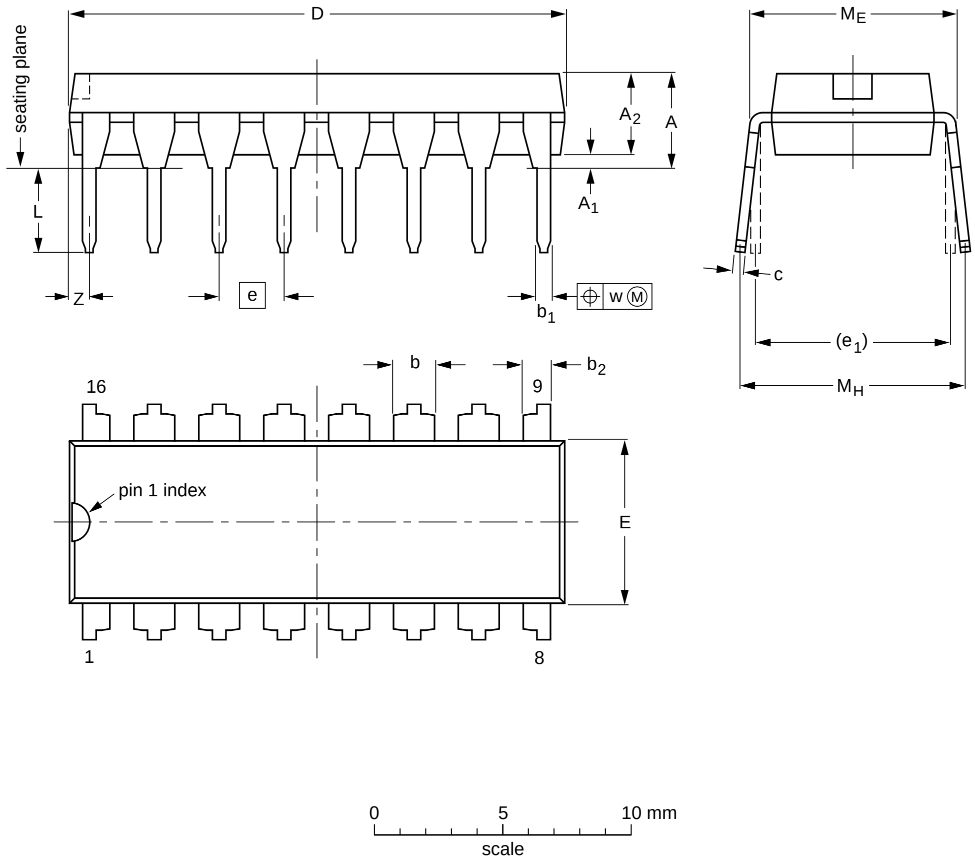


b. Test circuit

Fig 19. Typical frequency response

15. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

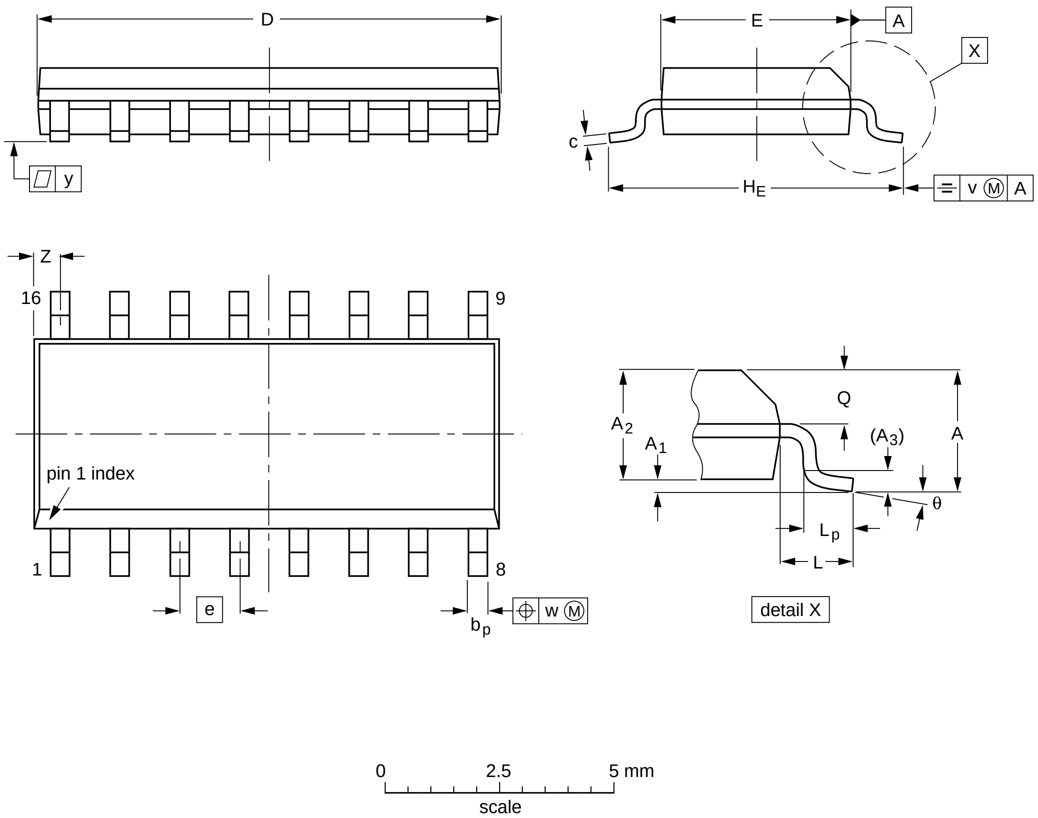
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 20. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

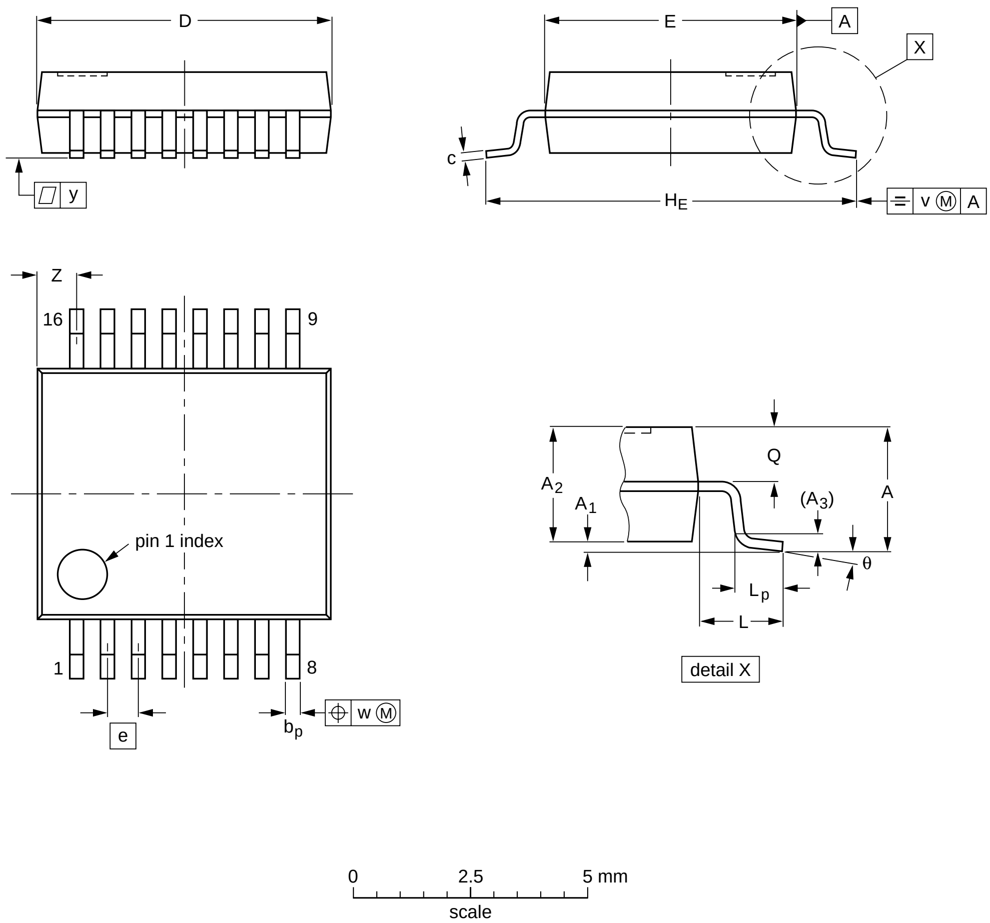
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 21. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

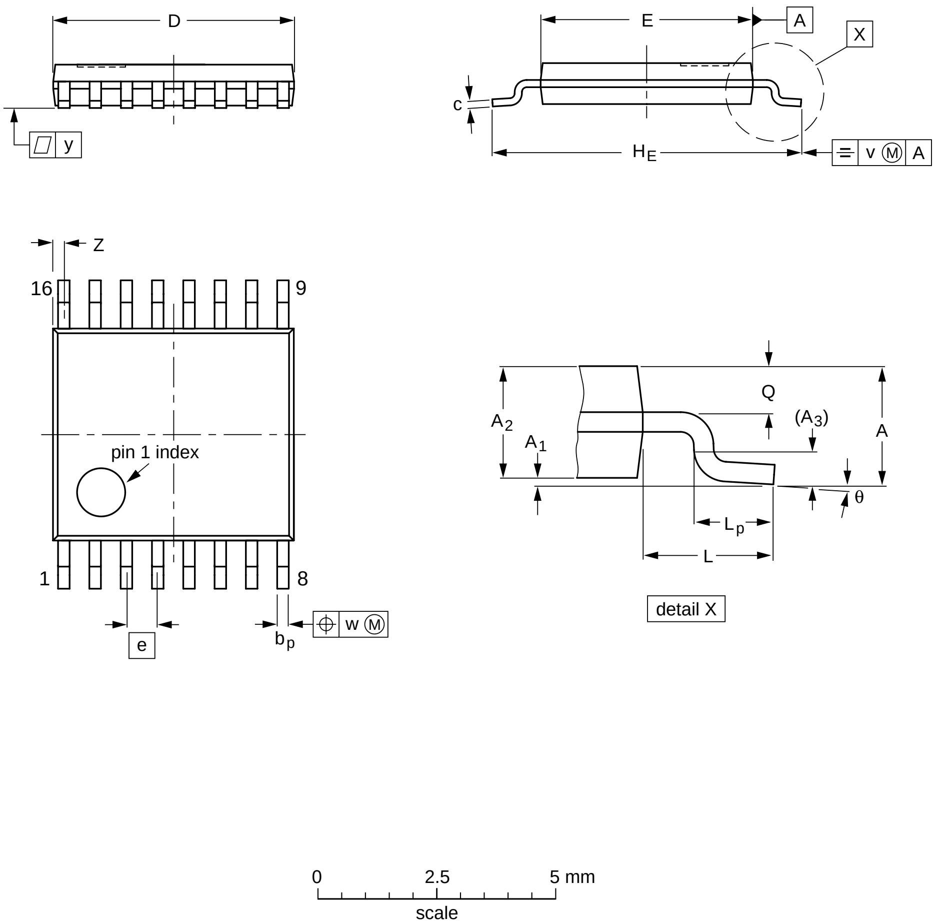
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 22. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

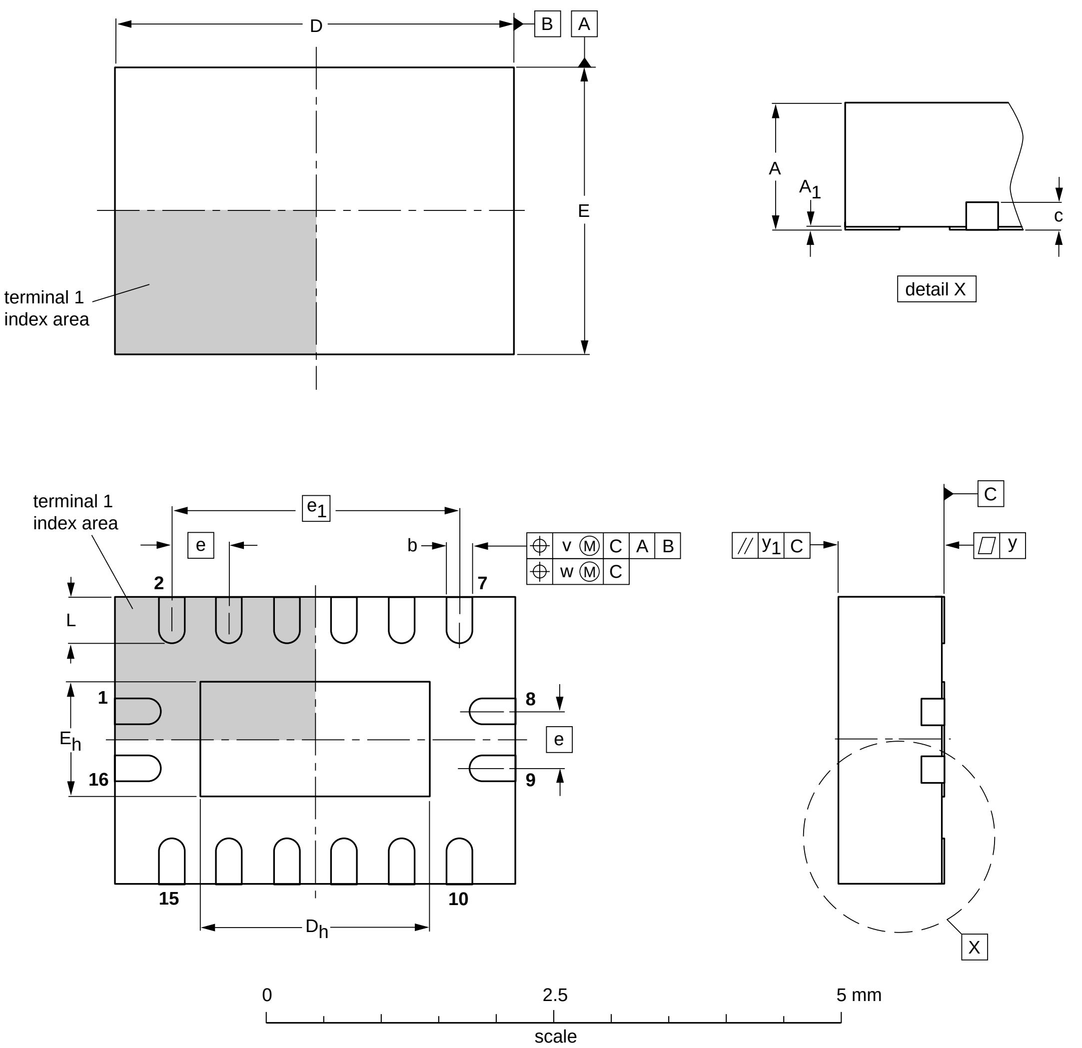
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 23. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm **SOT763-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.6 3.4	2.15 1.85	2.6 2.4	1.15 0.85	0.5	2.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT763-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 24. Package outline SOT763-1 (DHVQFN16)

16. Abbreviations

Table 15: Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
ESD	ElectroStatic Discharge
MM	Machine Model
DUT	Device Under Test

17. Revision history

Table 16: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74HC_HCT4053_4	20060509	Product data sheet	-	-	74HC_HCT4053_3
Modifications:	• Section 5 “Ordering information”: errors corrected, type numbers in wrong order and SOT38-4 is the package for types 74HC4053N and 74HCT4053N				
74HC_HCT4053_3	20060315	Product data sheet	-	-	74HC_HCT4053_CNV_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Added type numbers 74HC4053BQ and 74HCT4053BQ (DHVQFN16) package to Section 5 “Ordering information”, Section 7 “Pinning information” and Section 15 “Package outline”				
74HC_HCT4053_CNV_2	19901201	Product specification	-	-	-

18. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

19. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

20. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status ‘Production’), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

21. Trademarks

Notice — All referenced brands, product names, service names and trademarks are the property of their respective owners.

22. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

23. Contents

Date of release: 9 May 2006
Document number: 74HC_HCT4053_4

Published in The Netherlands