ZL40803

6 GHz Fixed Modulus ÷ 2

Data Sheet

July 2003

Features

- 3.45V Single Supply Operation
- Low Power Dissipation: 250mW typ
- Broadband: DC to 6GHz
- SSB Phase Noise: –147dBc/Hz @ 10KHz
- Pout 0dBm
- Surface Mount Plastic Package: 8 SOIC

Prescaler Modulus

ZL40803 – Divide by 2

Applications

- DC to 6 GHz PLL applications
- HyperLan
- LMDS
- Instrumentation
- Satellite Communications
- Fibre Optic Communications; OC48, OC192
- Ultra Low Jitter Clock Systems

Ordering Information

ZL40803/DCA (tubes)	8 pin SOIC
ZL40803/DCB (tape and reel)	8 pin SOIC

-40°C to +85°C

Description

The ZL40803 are Bipolar 3.45V supply, very low power prescalers for professional applications with a fixed modulus of 2. The ultra low close in (1KHz offset) SSB phase noise performance is ideal for narrow band communications systems or systems with ultra low jitter budgets such as next generation fibre optic communications. The devices are broadband from DC to 6GHz.

See Figure 1 and Application Note for RF Prescalers for more details.

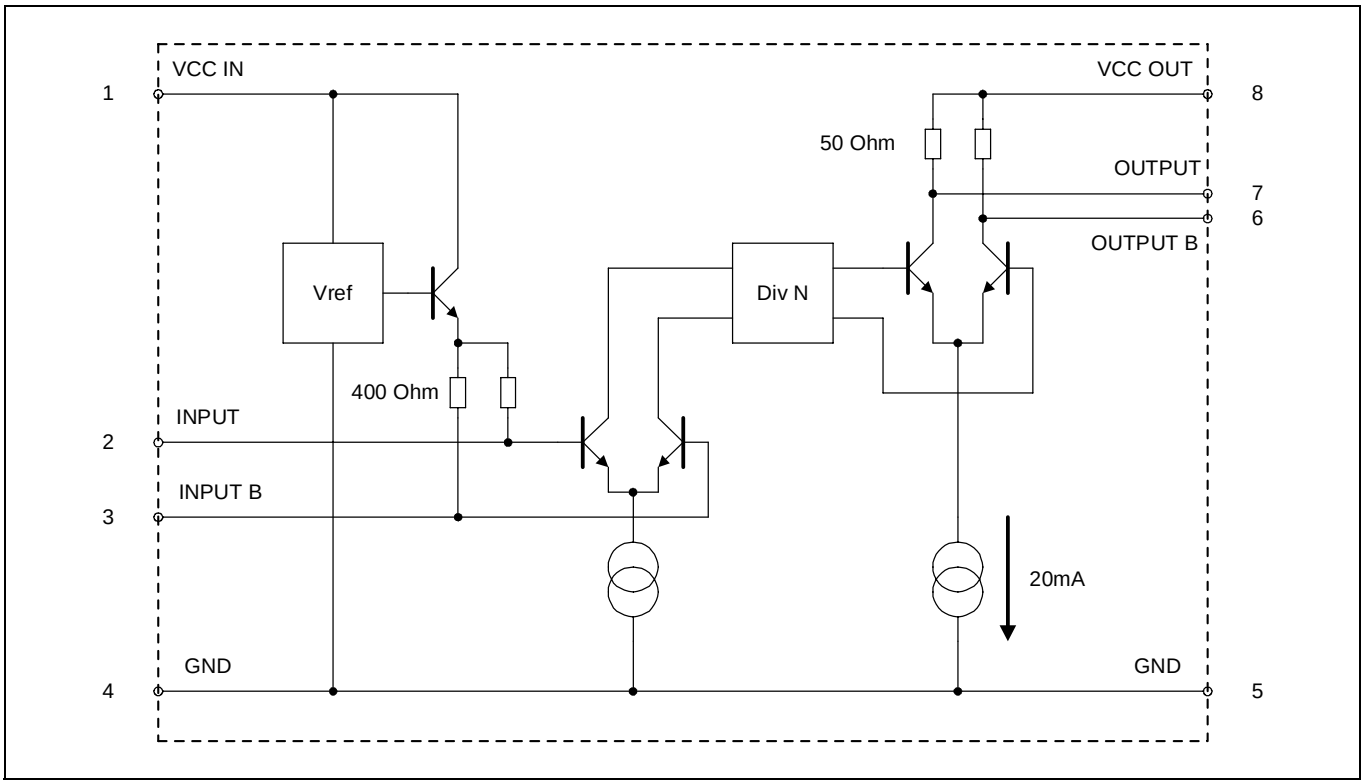


Figure 1 - Functional Block Diagram

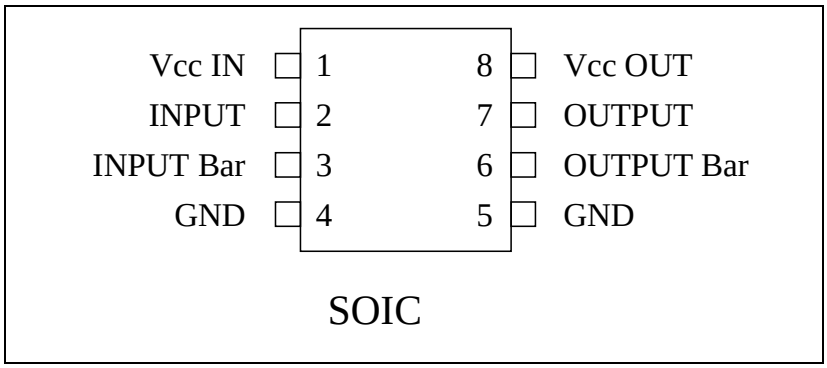


Figure 2 - Pin Connections – Top View

Application Configuration

Figure 3 shows a recommended application configuration. This example shows the device set up for single ended operation.

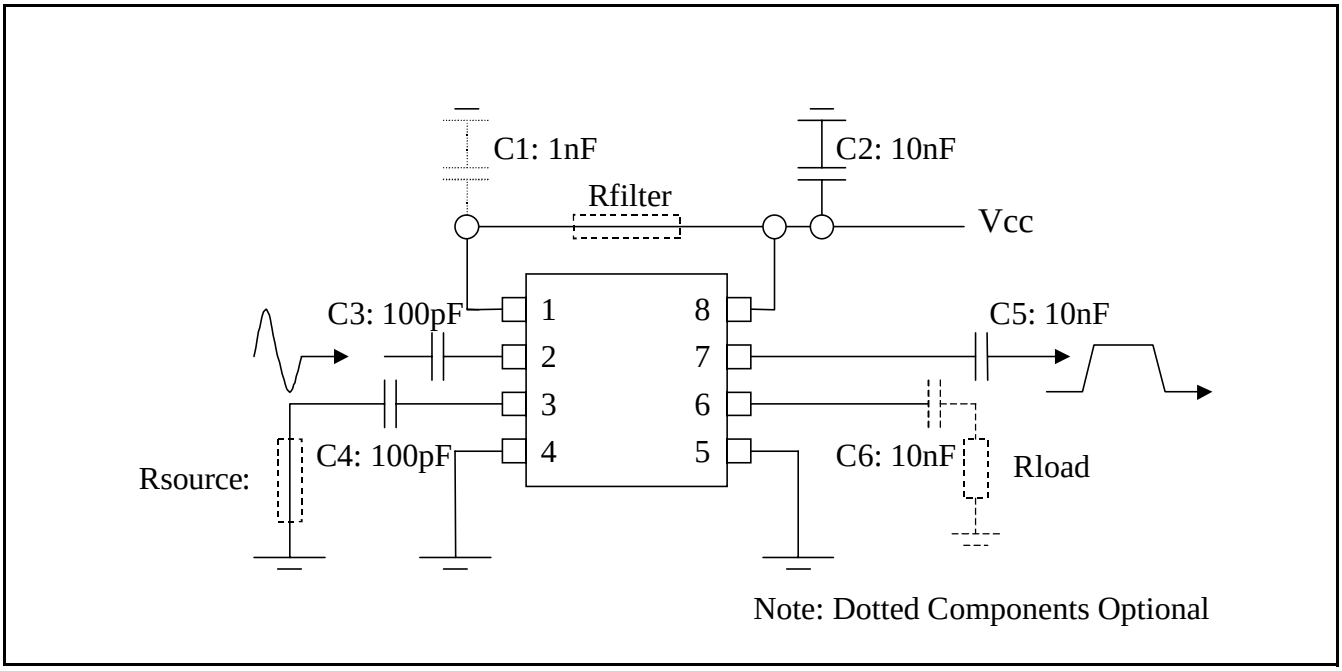


Figure 3 - Recommended circuit configuration

This represents the circuit used to complete characterisation. The tabulated Electrical performance is guaranteed using this application circuit.

Unpopulated evaluation boards are available, type No. ZLE40008. A fully populated evaluation board is also available, type No. ZLE40803.

Circuit Options

The application circuit includes some optional components that may be required to improve tolerance of system noise present in the application.

Dummy R source may be added to the inverting input to provide a better matched source impedance at the input. This will improve the rejection of common mode noise present within the system.

Dummy R load may be added to the inverting output to provide better matched load at the output. This will reduce the radiated EMI at the output and reduce the Output Noise present on the supply rail.

Rfilter can be inserted between the Vcc in and the Vcc_out to provide additional filtering to the input Vcc. The input Vcc powers the input bias reference only and can be a sensitive point to system noise. The nominal input current at Vcc_IN s 0.35mA. An alternative would be to use an inductive choke.

C1 is additional Supply Filtering and should be added with Rfilter. The IC includes 10pF of on Chip Supply Filtering.

Input & Output Circuit

Figure 4 shows the equivalent input and output circuit

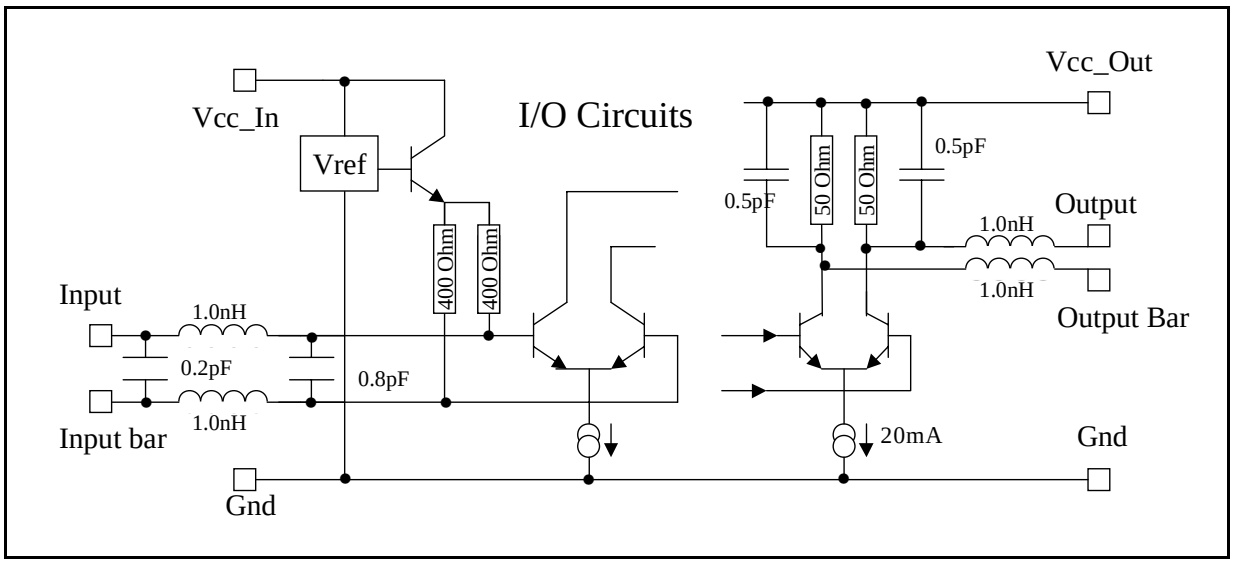


Figure 4 - Input and Output Equivalent Circuit

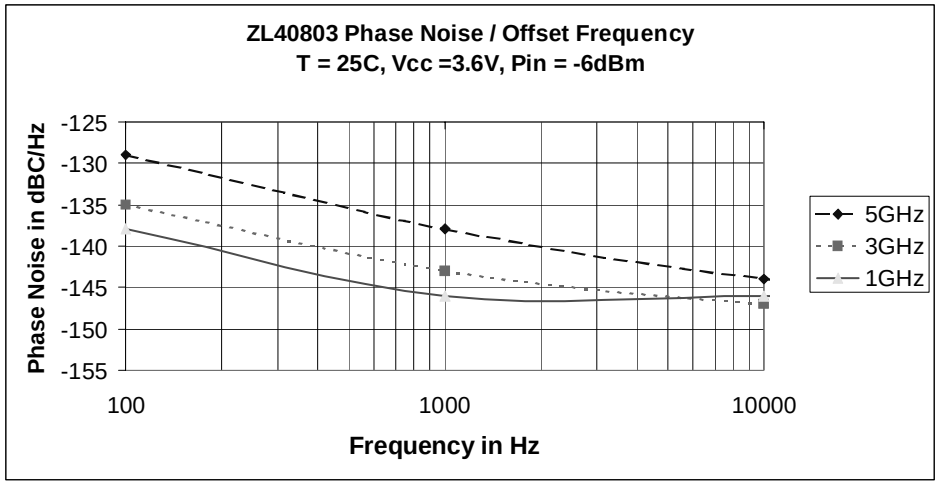


Figure 5 - ZL40803 Typical Phase Noise

Absolute Maximum Ratings

Characteristic	Min	Max	Units	Comments
Supply Voltage (Vcc)	- 0.5	6	V	
RFin		12	dBm	
All I/O ports	-0.5V	Vcc+0.5	V	
Storage Temperature	-55	150	°C	
ESD protection	2KV			Mil-std 883B / 3015 cat1

Operating Range

Characteristic	Min	Typ	Max	Units	Comments
Supply Voltage (Vcc)	3.3		3.6	V	
RFin Frequency Range	0.1		6	GHz	
Operating Junction Temperature	-40		+125	°C	
Junc'n to Amb't resistance Theta Ja		150		°C/W	4 layer FR4 Board
Junc'n to Case resistance Theta Jc		60		°C/W	4 layer FR4 Board

AC/DC Electrical Characteristics

Electrical Characteristics†

Characteristic	Pin	Min.	Typ.	Max.	Units	Conditions
Icc_in (Supply current)	1		0.35		mA	
Icc_out (Supply current)	8	44	72	110	mA	
Input frequency	2,3	1		6	GHz	RMS sinewave,
Input sensitivity	2,3		-20	-10	dBm	fin = 1GHz to 6GHz, Note1
Input overload	2,3	4	10		dBm	fin = 1GHz to 6GHz, Note1
Phase Noise	6,7		-150		dBC/Hz	@ 10KHz Offset Fin = 3GHz
Output voltage	6,7		1		Vp-p	Differential Into 50 ohm pull up resistors
Output power	6,7	-7	-2	2	dBm	fin = 1GHz to 6GHz, Pin = -10dBm, Note 2
Output t-rise	6,7		110		ps	fin = 1GHz to 6GHz, Pin = -10dBm
Output t-fall	6,7		110		ps	fin = 1GHz to 6GHz, Pin = -10dBm
T – prop delay	2,6		250		ps	50% IN to 50% OUT
Jitter	6,7		0.1		ps	
Output Duty Cycle	6,7	45	50	55	%	fin = 1GHz to 6GHz, In = -10dBm
Input. Edge Speed	2,3	500			V/us	For < 1GHz input operation

† These characteristics are guaranteed by design and characterisation over the following range of operating conditions unless otherwise stated: Tamb = -40C to + 85C, Vcc = 3.3V to 3.6V.

Note 1: Pin = power measured into 50 ohm Load from 50 ohm Source.

Note 2: Pout Single Ended AC coupled Single 50 Ohm Termination.

For details of the test set-up, refer to the Application Note for RF Prescalers.

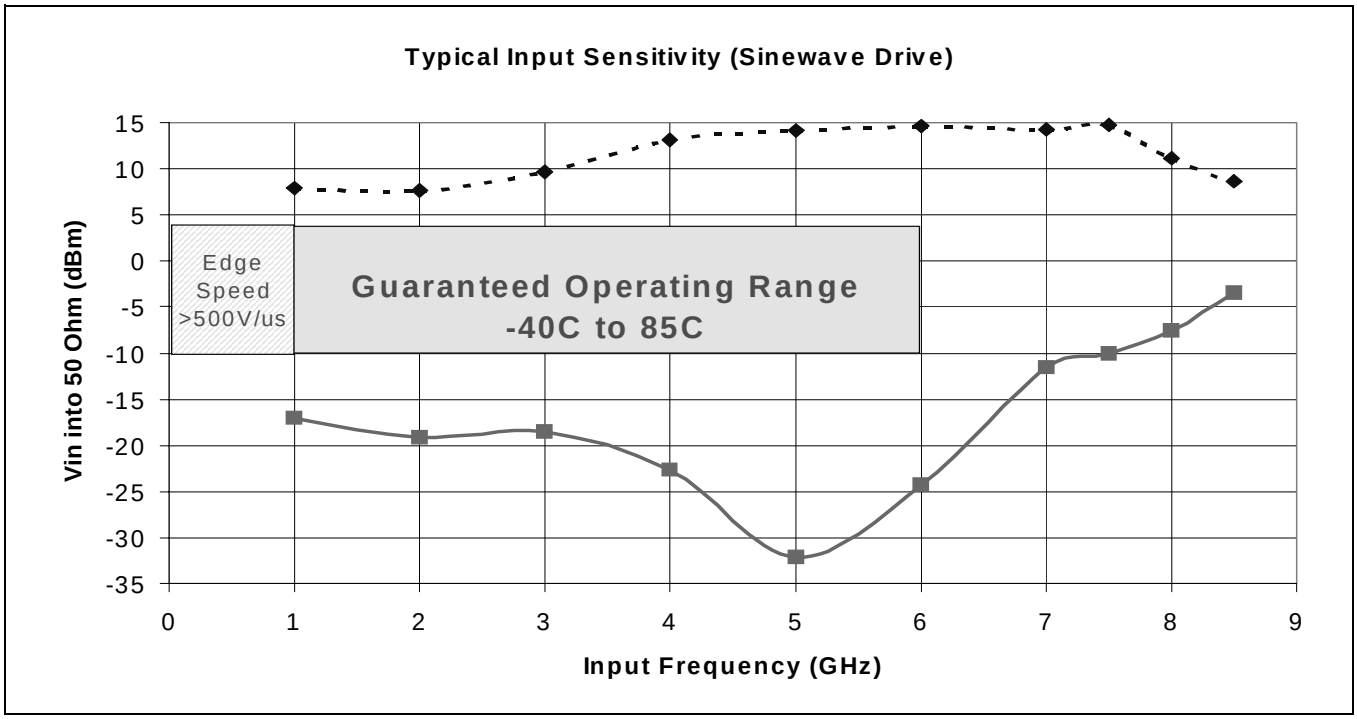


Figure 6 - Typical Input Sensitivity (sine wave drive)

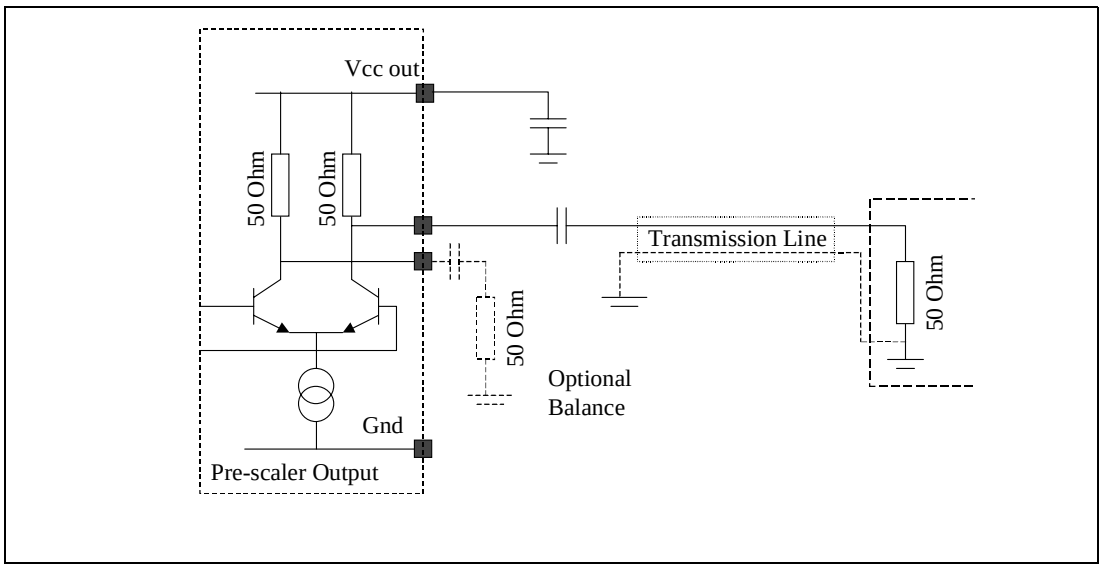


Figure 7 - Single Ended AC Coupled Single Termination

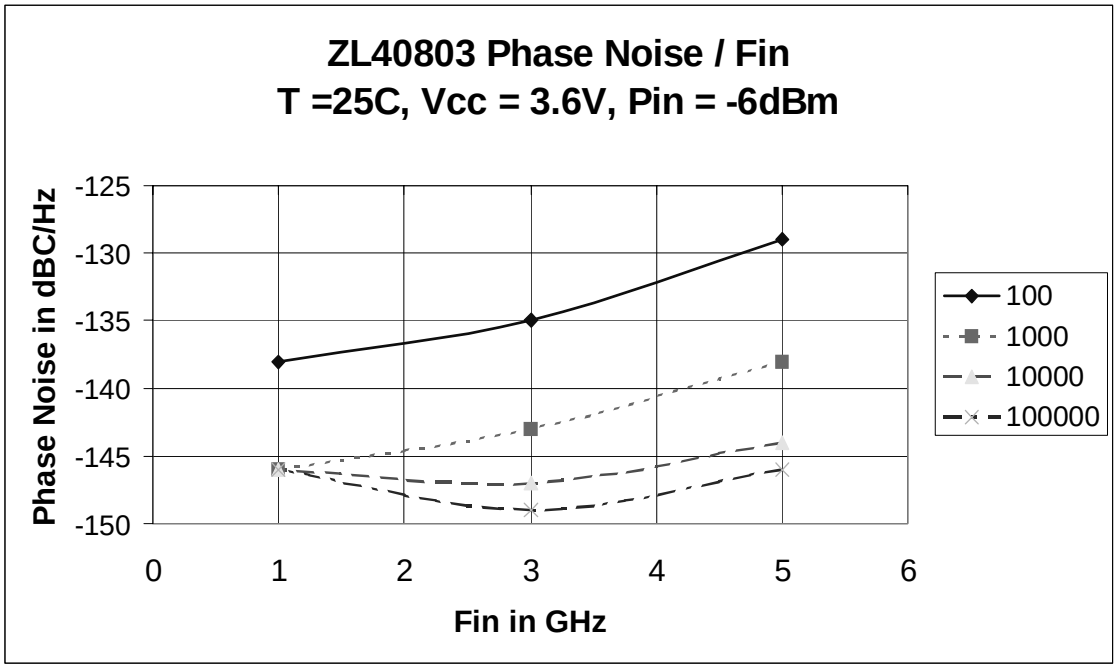


Figure 8 - ZL40803 Phase Noise vs Input Frequency

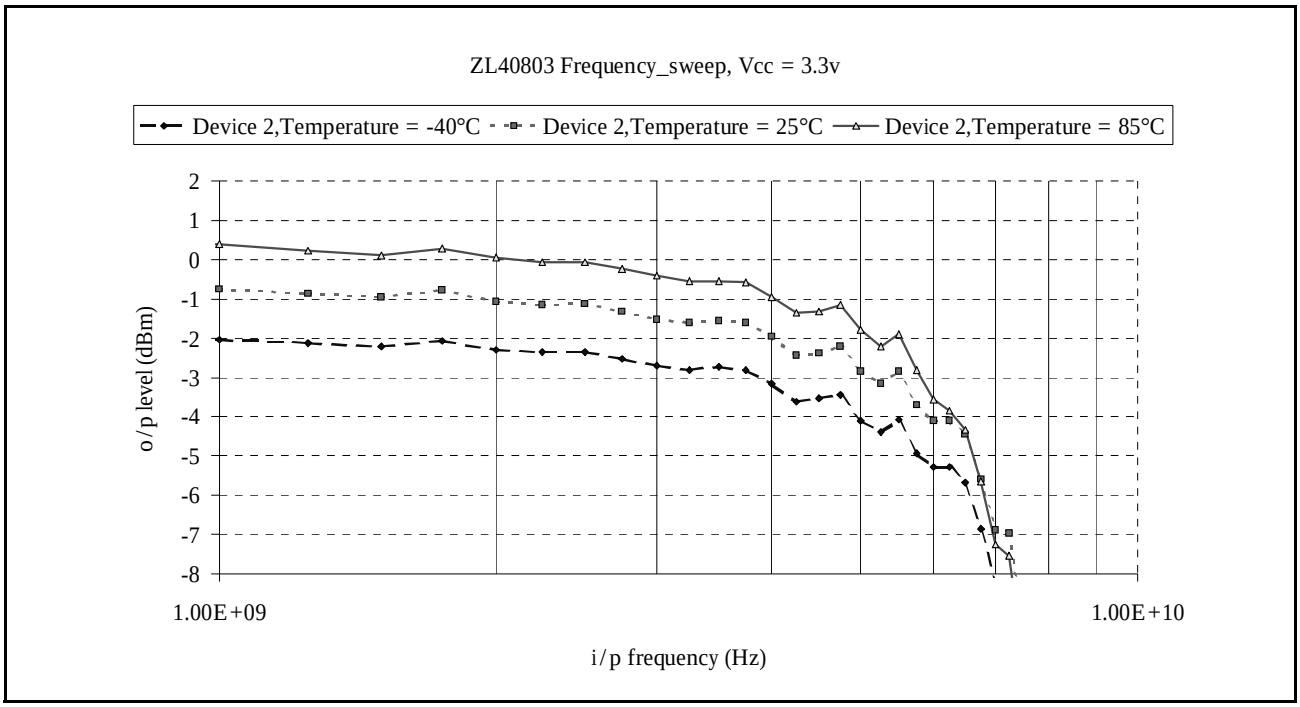


Figure 9 - ZL40803 Pout vs Input Frequency (Vcc = 3.3V, T=25C, T=85C)

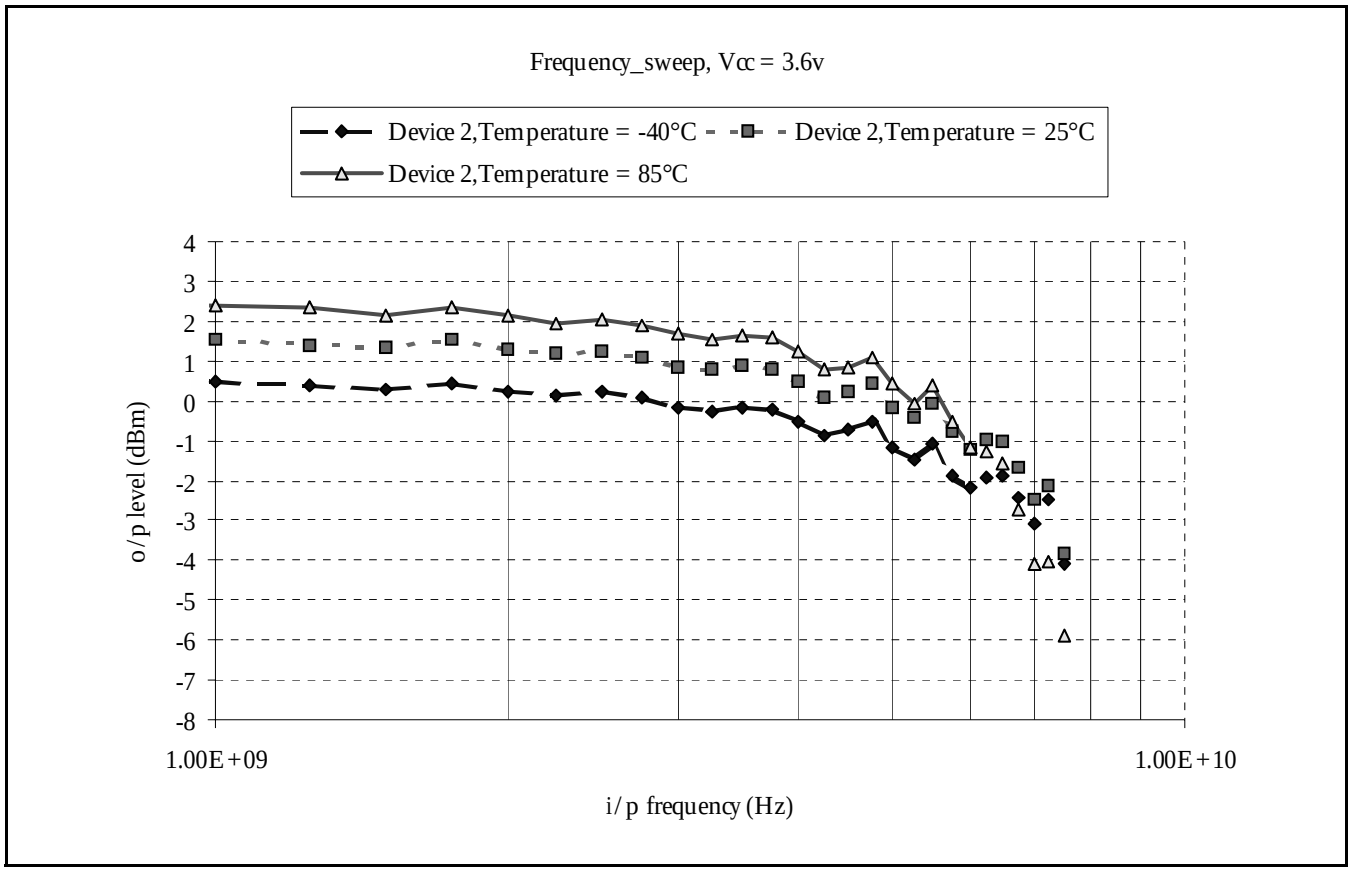


Figure 10 - ZL40803 Pout vs Input Frequency (Vcc = 3.6V, T=25C, T=85C)

Single Ended or Differential Load

Figures 11 and 12 illustrate the output waveform when measured differential and single ended with a 5GHz waveform at the input at a level of +2dBm. The single ended output contains some input frequency break through which contributes to the distortion present. This is a common mode signal which is rejected if the output is taken differentially.

Differential operation also provides an additional 3dB.

Differential Operation reduces the radiated EMI in the system and reduces the susceptibility to common mode system noise.

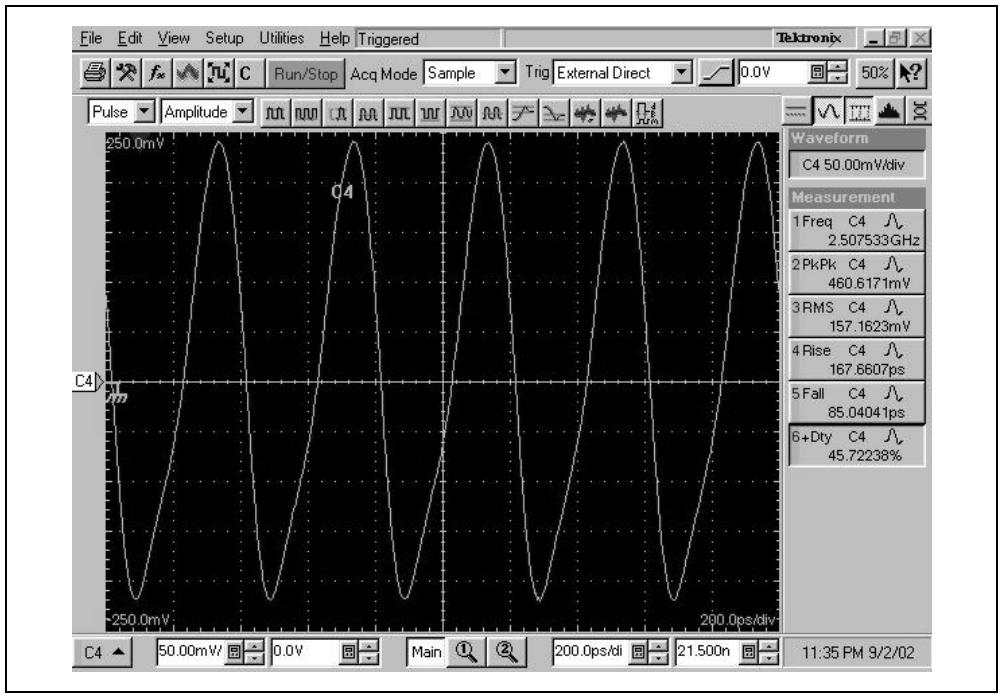


Figure 11 - ZL40803 Single Ended Out @ 5GHz +2dBm

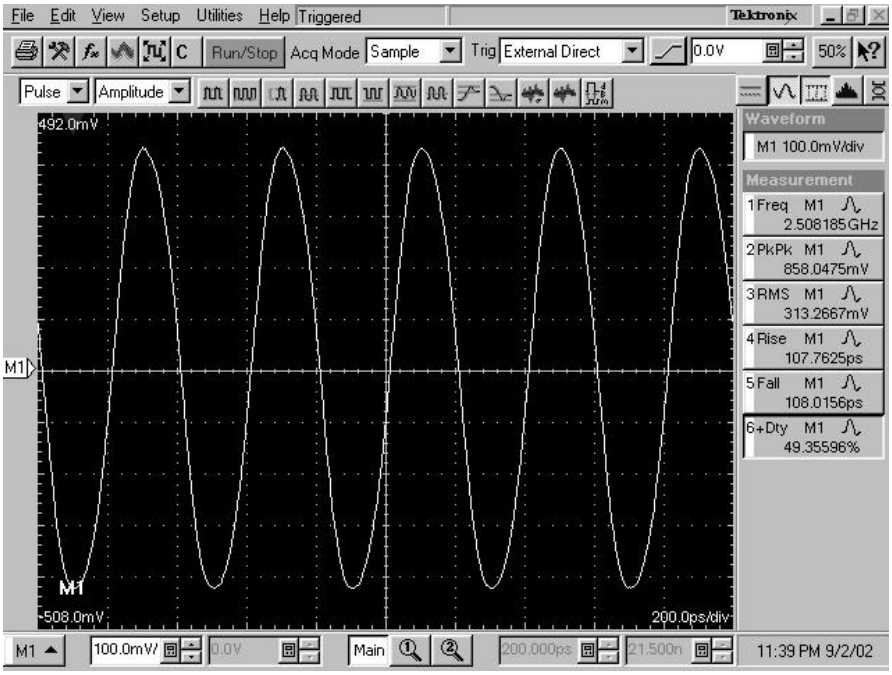
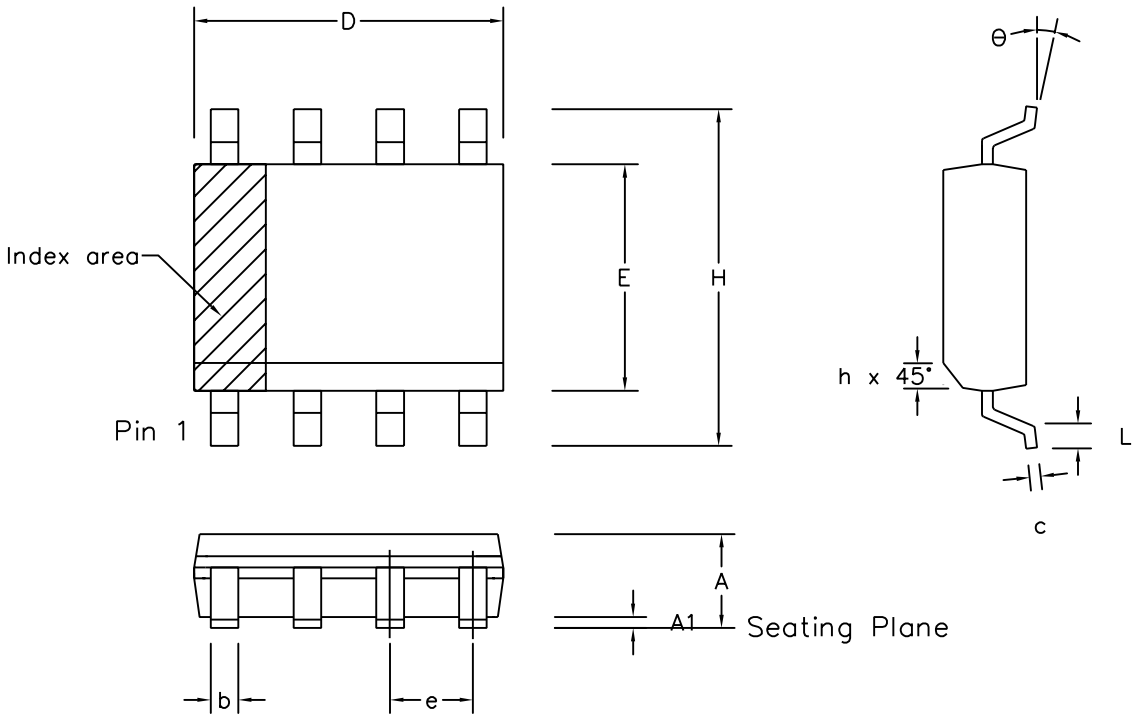


Figure 12 - ZL40803 Differential Out @ 5GHz +2dBm



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.80	5.00	0.189	0.197
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	8		8	
Conforms to JEDEC MS-012AA Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	1	2	3	4	5
ACN	6745	201936	202595	203705	212424
DATE	5Apr95	27Feb97	12Jun97	9Dec97	22Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 8 lead SOIC (0.150" Body width)

GPD00010

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