# VM6101

## I²C color light sensor

## Features

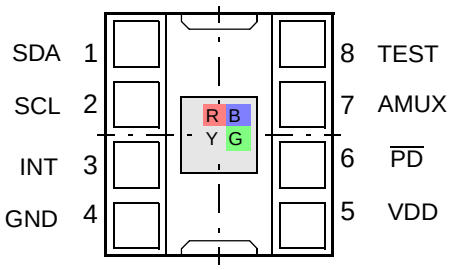
- 4-channel Y+RGB photosensor, with integrated infrared filter
- Wide dynamic range light to frequency converters
- 2-wire serial interface, I²C and SMBus compatible
- PWM output for direct LCD backlight control
- Comparator logic with two programmable thresholds and hysteresis function
- Power down input
- 3.0 V to 3.6 V supply range
- Built-in clock generator, precision voltage and current references
- Low profile Pb-free package (RoHS compliant)

## Applications

- General purpose color measurement
- Automatic backlighting control
- Panel lighting
- White goods

## Pinout

**VM6101V008**
8-lead MLPD
Top view





Optical center location: (+70, +35) µm relative to package center.

Sensitive area: 220 x 240 µm

## Description

The VM6101 is a high dynamic range 4-channel CMOS photosensor suitable for ambient light sensing as well as color light sensing. Light intensity is converted linearly to a variable frequency signal. The signal period is readable through the two-wire serial interface.

A direct PWM output is provided for power saving LCD backlighting applications, where backlighting intensity adapts to the ambient light level. Alternatively, this output can be used as an ambient light level detector output, with two user programmable thresholds.

A power down input puts the VM6101 in ultra low power mode.

The VM6101 is housed in an compact 8-lead surface mount clear plastic package, compliant to RoHS directive.

# Contents

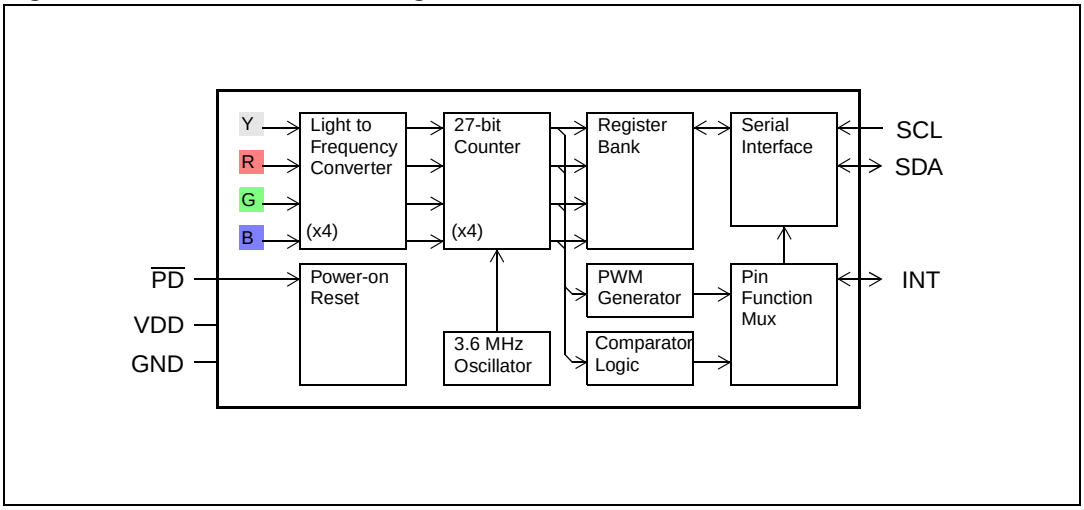
# 1 Pin description

**Table 1. Pin description**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | SDA | I/O | Serial interface data. Requires external pull-up to VDD. |
| 2 | SCL | I/O | Serial interface clock. Requires external pull-up to VDD. |
| 3 | INT | I/O | Dual function output:<br>- Comparator logic output<br>- PWM generator output<br>Input for serial interface 7-bit address select:<br>- low = address 0x10 (default)<br>- high = address 0x11<br>Requires external pull-up or pull-down resistor (1 MΩ typically). |
| 4 | GND | PWR | Ground |
| 5 | VDD | PWR | Positive power supply |
| 6 | $\overline{PD}$ | AIN | Power down control:<br>- low = force low power standby<br>- high = normal operation |
| 7 | AMUX | AIO | Reserved. Do not connect. |
| 8 | TEST | AIN | Reserved. Connect to GND. |

# 2 Functional description

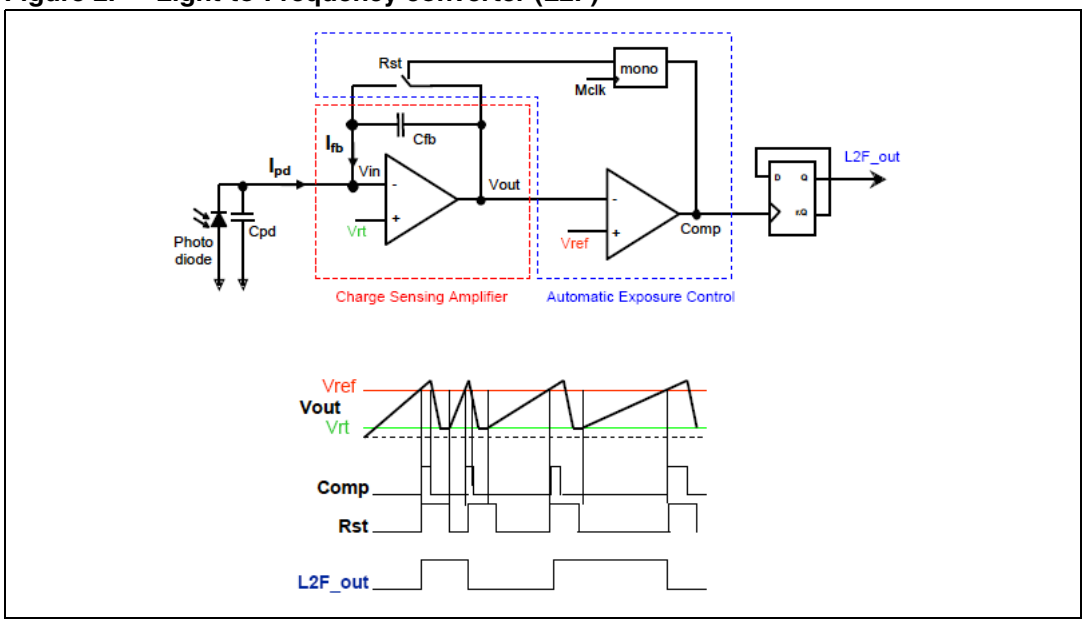
**Figure 1. Functional block diagram**



## 2.1 Light measurement channels

The VM6101 has four independent wide dynamic range photosensors and current-to-frequency converters. Each channel produces a digital output with a frequency proportional to the incoming light level on the photosensor. By construction, the device ensures automatic exposure control.

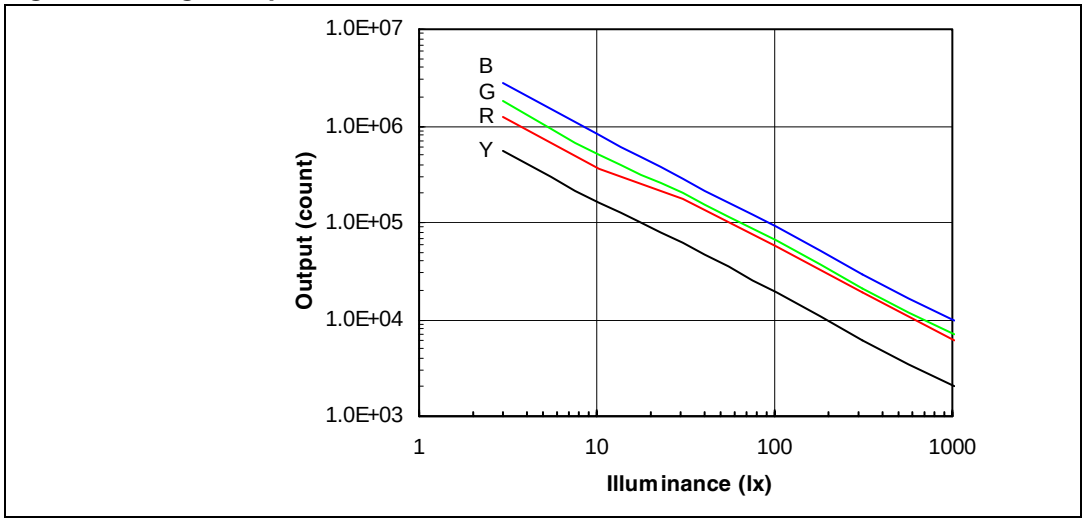
**Figure 2. Light-to-Frequency converter (L2F)**




The output period is measured using a 27-bit free-running counter and the internal 3.6 MHz oscillator clock; counter values are then read through the serial interface.

The typical light response is shown in *Figure 3.* below, obtained using a CIE D65 white point light source (~ daylight illumination) and no light diffuser.

**Figure 3. Light response**



The light response can be approximated by:

- Y channel: $E_{vY} = 1.58e6 \times count^{-0.960}$
- R channel: $E_{vR} = 3.34e6 \times count^{-0.902}$
- G channel: $E_{vG} = 4.92e6 \times count^{-0.944}$
- B channel: $E_{vB} = 8.03e6 \times count^{-0.973}$

The response time is: $t = count / f_{OSC}$ + serial interface read time (about 200 µs)
Example: t = 9.3 ms for 300 lx.

Each channel provides three status flags and a counter value:

- **RESET**: This flag is set upon reset or power-down resume. The counter value is invalid and should be discarded. This flag is cleared after a status read operation.
- **OVERFLOW**: at least one counter overflow occurred: the counter value is invalid and should be discarded. This flag is cleared when a new valid counter value is available.
- **READY**: a new counter value is available. This flag is cleared immediately after the status register read.
- **CNT**: a 27-bit counter value, mapped in 4 consecutive bytes, MSB first and right justified.

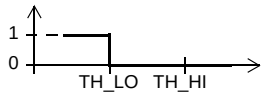
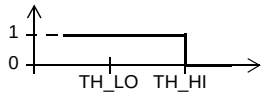
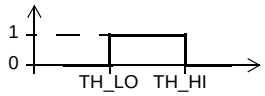
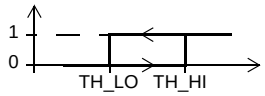
Channel readout must always start by reading the corresponding status register. The suggested read operation is a 5-byte read operation starting at the status register address.

Refer to *Chapter 4: Register description* for details.

## 2.2 Comparator logic

This function compares the light level (i.e. channel counter CNT) with two programmable thresholds (TH_LO and TH_HI) and drives the INT pin accordingly. The following table shows available configurations using TH_CFG register setup:

**Table 2. Threshold module configurations (TH_CFG register usage)**

| EN_HI: EN_LO | INT output | INT versus CNT (assumes INT_POL = 0) |
|---|---|---|
| 00 | 0 | 0 |
| 01 | POL_LO xor (CNT < TH_LO) |  (POL_LO = 0) |
| 10 | POL_HI xor (CNT < TH_HI) |  (POL_HI = 0) |
| 11 | HYST = 0:<br>(POL_LO xor (CNT < TH_LO)) and<br>(POL_HI xor (CNT < TH_HI)) |  (POL_LO = 1, POL_HI = 0) |
| | HYST = 1: see diagram |  (POL_LO = 1, POL_HI = 0) |

Notes

1. Upon reset, the comparator logic is enabled (EN_HI:EN_LO = 01) with POL_LO = 1 and TH_LO = 0x0008. The INT pin is high when Y channel count > 8.
2. Assuming CONTROL= 0x04, i.e. comparator mode using Y channel count (default value for CONTROL register).
3. Ensure TH_LO < TH_HI otherwise unpredictable results may occur.

## 2.3 PWM generator

The pulse width modulator (PWM) generates a signal which may be used to directly control LCD backlight driver ICs according to ambient light level.

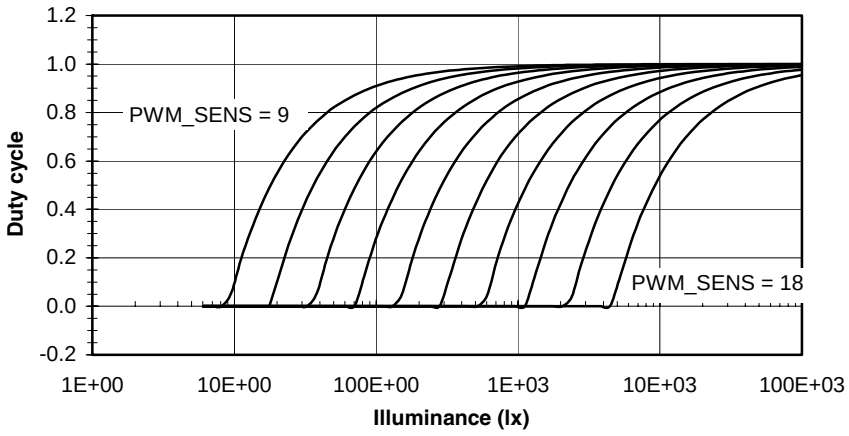
There are three registers to control the PWM generator operation:

- PWM_FREQ register bits [4:0] sets the period of the PWM signal. This is adjustable from 12Hz to 400kHz.
- PWM_SENS register bits [4:0] sets the sensitivity of the PWM signal to light level.
- CONTROL register bit 2 = 0 to select PWM output at INT pin.
- CONTROL register bit 3 controls the polarity of the PWM output (default = 0).

For more details please refer to *Chapter 4: Register description*.

The curve below shows typical PWM output duty cycle (default polarity) as a function of illumination, with sensitivity setting ranging from 9 to 18, corresponding to typical use cases (10 to 10000 lx illumination).

**Figure 4. PWM duty cycle versus illumination**




## 2.4 Two-wire serial interface

The VM6101 two-wire serial interface supports the following features:

- Standard-mode (100 kHz) I²C slave controller supporting 8-bit addressing (7-bit address = 0x10 or 0010 000). SMBus compliant.
- Data and clock deglitching filters (double sampling)
- 8-bit index, i.e. 256 on-chip register address space
- Multiple read or write with index auto-increment
- Alternate address (0x11) selectable

### 2.4.1 Message types

The VM6101 registers are accessed by serial bus byte-oriented transactions. The following message types are supported:

- Master write:
  *<S> <addr><w><A> <index><A> <data><A>[<data><A>...<data><A>]<P>*
- Master read:
  *<S> <addr><r><A> [<data><A>...<data><A>]<data><nA><P>*
- Combined format:
  *<S> <addr><w><A> <index><A>*
  *<Sr> <addr><r><A> [<data><A>...<data><A>]<data><nA><P>*

where:

*S* = start, *S*r = repeated start, *P* = stop, *A*= acknowledge, *nA* = negative acknowledge
*addr* = 7-bit slave address, *w* = write bit (0), *r* = read bit (1),
*index* = 8-bit register address,
*data* = 8-bit register data, *[]* = optional.

### 2.4.2 Alternate slave address selection

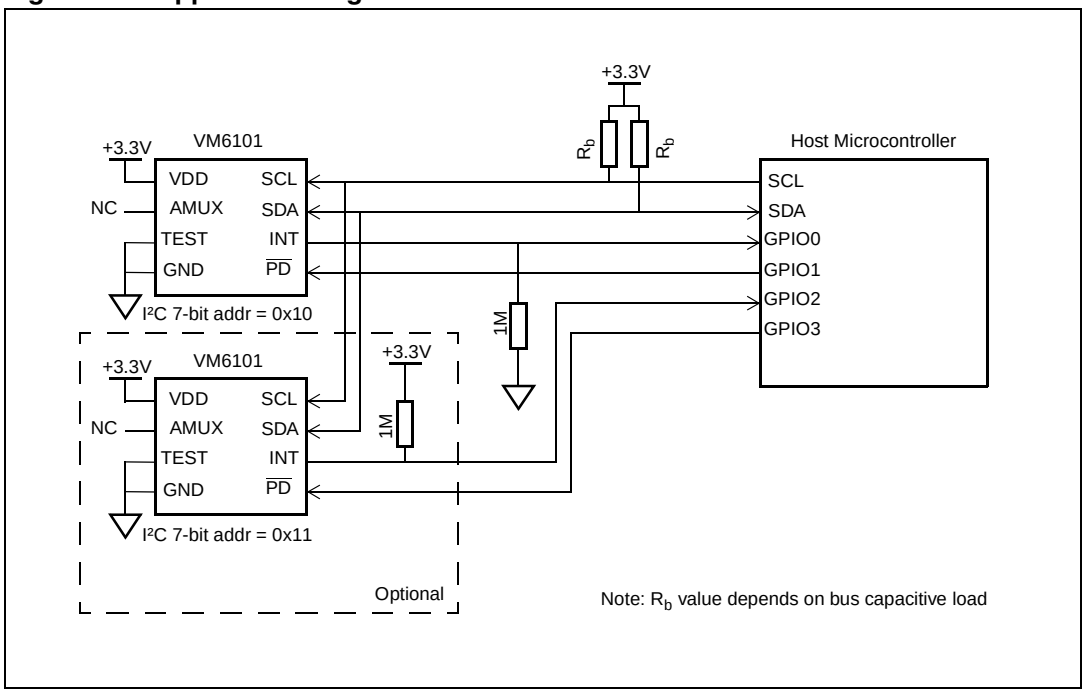
After power-on or after resuming from power-down, the 7-bit slave address is 0x10. If another slave device shares the same address, it is possible to remap the VM6101 to address 0x11 by performing the following operations:

1. Connect the INT pin to a pull-up resistor to $V_{DD}$ (1 MΩ typ.).
2. After power-on or power-down resume, issue a write command to set the ADDR_SEL bit of CONTROL register (i.e. write 0x10 at register address 0x02, slave address 0x10).
3. At this time, the VM6101 samples the INT pin and sets its slave address accordingly:
   INT sampled low: 7-bit address = 0x10,
   INT sampled high: 7-bit address = 0x11.

Two VM6101 can thus coexist on the same bus; one should have its INT pin pulled low, the other one should have its INT pin pulled high (see *Figure 5.*).

# 3 Application information

**Figure 5. Application diagram**



# 4 Register description

*Note: RO = Read Only; RW = Read/Write.*

*Reserved bits must be written with 0s and return 0 upon read; Reserved bytes must not be accessed otherwise unpredictable results my occur.*

**Table 3. Register description**

| Addr. | Bits | Def. | Name | Description |
|---|---|---|---|---|
| 0x00 | [3:0] | 1 | REVISION | Chip revision (RO). |
| 0x00 | [7:4] | 0 | MASK | Mask code (RO). |
| 0x01 | [7:0] | 0x04 | N_PIXEL | (RO) |
| 0x02 | [6:0] | 0x04 | CONTROL | Control register (RW) |
| | [1:0] | 0 | CHSEL | Channel select for comparator and PWM logic:<br>0: Y<br>1: R<br>2: G<br>3: B |
| | 2 | 1 | INT_FSEL | INT pin function select:<br>0: PWM generator output<br>1: Comparator logic output |
| | 3 | 0 | PWM_POL | PWM polarity:<br>0: Normal (Thin pulse for low values, Wide pulses for high values)<br>1: Inverted. |
| | 4 | 0 | ADDR_SEL | Address Select: when written with '1', the INT pin goes high impedance; after a duration T (defined below), the INT pin is sampled and returns to low impedance.<br>The device slave address is set accordingly:<br>INT sampled low: address = 0x20<br>INT sampled high: address = 0x22. |
| | [6:5] | 0 | ADDR_SELW | Address select sampling window duration:<br>0: T = 160 µs (default)<br>1: T = 80 µs<br>2: T = 40 µs<br>3: T = 20 us<br>This duration allows for INT pin pull-up rise time. |
| | 7 | 0 | | Reserved |
| 0x03 | [7:0] | 0 | | Reserved (RO). |
| 0x04 | [2:0] | 0x01 | Y_STATUS | Y-channel status register (RO).<br>Reading this register will cause Y_CNT to be transferred to serial interface buffer. 5 MSBs are read as zeros. |
| | 0 | 1 | RESET | This bit is set after reset. Cleared after first read of STATUS register. |
| | 1 | 0 | OVERFLOW | This bit is set upon counter overflow: current counter values are invalid. |
| | 2 | 0 | READY | When set, indicates that a new count value is available in the 4 registers here below. |

**Table 3. Register description (continued)**

| Addr. | Bits | Def. | Name | Description |
|---|---|---|---|---|
| 0x05 | [2:0] | 0 | Y_CNT3 | Y channel count bits [26:24] (RO). 5 MSBs are read as zeros. |
| 0x06 | [7:0] | 0 | Y_CNT2 | Y channel count bits [23:16] (RO) |
| 0x07 | [7:0] | 0 | Y_CNT1 | Y channel count bits [15:8] (RO) |
| 0x08 | [7:0] | 0 | Y_CNT0 | Y channel count bits [7:0] (RO) |
| 0x09 | [7:0] | 0x01 | R_STATUS | R channel status register (RO). Refer to Y Channel for description. |
| 0x0a | [2:0] | 0x00 | R_CNT3 | R channel count bits [26:24] (RO). 5 MSBs are read as zeros. |
| 0x0b | [7:0] | 0x00 | R_CNT2 | R channel count bits [23:16] (RO) |
| 0x0c | [7:0] | 0x00 | R_CNT1 | R channel count bits [15:8] (RO) |
| 0x0d | [7:0] | 0x00 | R_CNT0 | R channel count bits [7:0] (RO) |
| 0x0e | [7:0] | 0x01 | G_STATUS | G channel status register (RO). Refer to Y Channel for description. |
| 0x0f | [2:0] | 0x00 | G_CNT3 | G channel count bits [26:24] (RO). 5 MSBs are read as zeros. |
| 0x10 | [7:0] | 0x00 | G_CNT2 | G channel count bits [23:16] (RO) |
| 0x11 | [7:0] | 0x00 | G_CNT1 | G channel count bits [15:8] (RO) |
| 0x12 | [7:0] | 0x00 | G_CNT0 | G channel count bits [7:0] (RO) |
| 0x13 | [7:0] | 0x01 | B_STATUS | B channel status register (RO). Refer to Y Channel for description. |
| 0x14 | [2:0] | 0x00 | B_CNT3 | B channel count bits [26:24] (RO). 5 MSBs are read as zeros. |
| 0x15 | [7:0] | 0x00 | B_CNT2 | B channel count bits [23:16] (RO) |
| 0x16 | [7:0] | 0x00 | B_CNT1 | B channel count bits [15:8] (RO) |
| 0x17 | [7:0] | 0x00 | B_CNT0 | B channel count bits [7:0] (RO) |
| 0x18 | [5:0] | 0x03 | TH_CFG | Comparator logic configuration (RW). 2 MSBs are reserved. Refer to *Section 2.2: Comparator logic* for programming details. |
| | 0 | 1 | EN_LO | Enable low threshold comparator (1 = enable, 0 = disable) |
| | 1 | 1 | POL_LO | Low threshold comparator output polarity |
| | 2 | 0 | EN_HI | Enable high threshold comparator (1 = enable, 0 = disable) |
| | 3 | 0 | POL_HI | High threshold comparator output polarity |
| | 4 | 0 | INT_POL | INT pin output polarity |
| | 5 | 0 | HYST | Enable hysteresis function |
| 0x19 | [2:0] | 0x00 | TH_LO3 | Low threshold bits [26:24] (RW). 5 MSBs are read as zeros. |
| 0x1a | [7:0] | 0x00 | TH_LO2 | Low threshold bits [23:16] (RW) |
| 0x1b | [7:0] | 0x00 | TH_LO1 | Low threshold bits [15:8] (RW) |
| 0x1c | [7:0] | 0x08 | TH_LO0 | Low threshold bits [7:0] (RW) |
| 0x1d | [2:0] | 0x00 | TH_HI3 | High threshold bits [26:24] (RW). 5 MSBs are read as zeros. |
| 0x1e | [7:0] | 0x00 | TH_HI2 | High threshold bits [23:16] (RW) |
| 0x1f | [7:0] | 0x00 | TH_HI1 | High threshold bits [15:8] (RW) |
| 0x20 | [7:0] | 0 | TH_HI0 | High threshold bits [7:0] (RW) |

**Table 3. Register description (continued)**

| Addr. | Bits | Def. | Name | Description |
|---|---|---|---|---|
| 0x21 | [3:0] | 0x00 | PWM_FREQ | PWM output frequency (RW)(4 MSBs are reserved):<br>n = 0 to 15<br>$f_{PWM} = f_{OSC} * 2^{n-18}$, where $f_{OSC}$ = 3.6 MHz. |
| 0x22 | [4:0] | 0x00 | PWM_SENS | PWM sensitivity (RW)(3 MSBs are reserved):<br>n = 0 to 26<br>0 = high sensitivity, 26 = low sensitivity. Practical values lie between 9 and 18. Refer to *Figure 4: PWM duty cycle versus illumination* for typical behavior. |
| 0x22<br>...<br>0x27 | [7:0] | | | Reserved. |
| 0x28 | [7:0] | 0x04 | TEST_MOD | Reserved (RW). |
| 0x29 | [7:0] | 0x00 | TEST_SEL | Reserved (RW). |
| 0x2A<br>...<br>0xFF | [7:0] | | | Reserved. |

# 5 Optical characteristics

**Table 4. Optical characteristics (1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| E | Irradiance range | | 0.0001 | | 800 | $Wm^{-2}$ |
| $E_V$ | Illuminance range | | 0.03 | | 170k | lx |

1. Using typical operating conditions: $T_A$ = 25 °C, $V_{DD}$ = 3.3 V

**Figure 6. Spectral response**

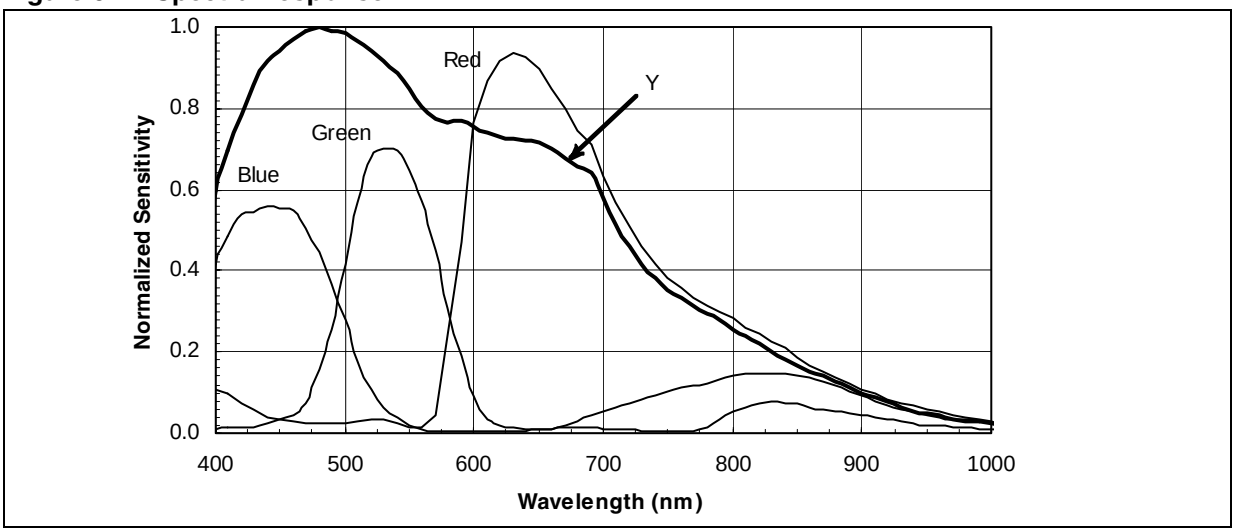



**Figure 7. Angular response**

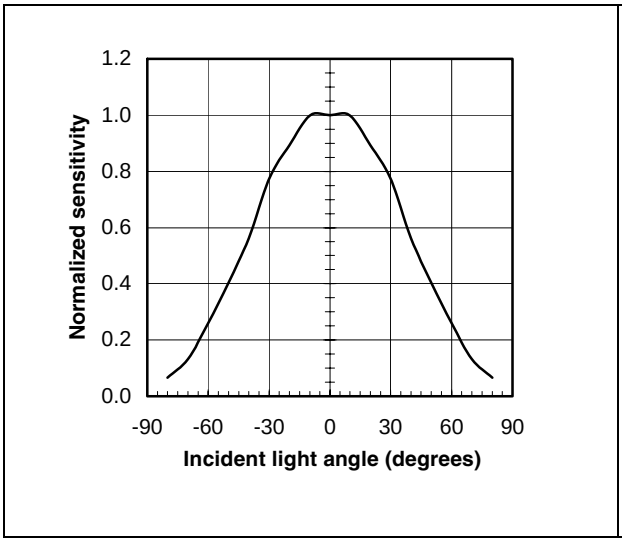
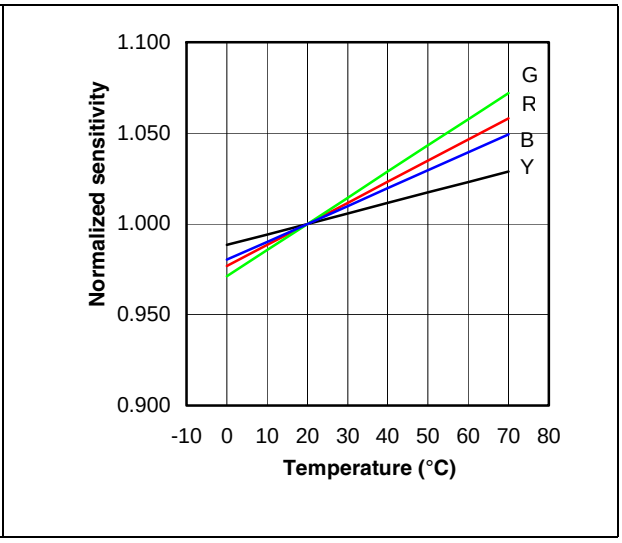



**Figure 8. Relative output versus temperature**



# 6 Electrical characteristics

**Table 5. Absolute maximum ratings (*Note 1*, *Note 2*)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | -0.5 | 3.7 | V |
| $V_{IN}$ | DC input voltage, all I/O pins | -0.5 | $V_{DD}$ + 0.5 | V |
| $T_{STG}$ | Storage temperature | -40 | 85 | °C |
| $T_L$ | Solder reflow peak temperature, JEDEC J STD-020 | | 245 | °C |
| $ESD_{HBM}$ | Human body model ESD rating, all pins, JESD22-A114-B | | 2 | kV |
| $ESD_{MM}$ | Machine model ESD rating, all pins, JESD22-A115-B | | 200 | V |
| $ESD_{CDM}$ | Charged device model ESD rating, all pins, JESD22-C101-C | | 500 | V |

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_A$ | Operating temperature | 0 | 70 | °C |
| $V_{DD}$ | Supply voltage | 3.0 | 3.6 | V |
| $V_{IL}$ | Input low voltage (SCL, SDA) | 0 | 0.3 $V_{DD}$ | V |
| | Input low voltage ($\overline{PD}$) | 0 | 0.8 | V |
| $V_{IH}$ | Input high voltage (SCL, SDA) | 0.7 $V_{DD}$ | $V_{DD}$ | V |
| | Input high voltage ($\overline{PD}$) | 2.0 | | V |
| $I_{OL}$ | Output low current | | 4 | mA |
| $I_{OH}$ | Output high current | | 4 | mA |

**Table 7. DC electrical characteristics (*Note 3*)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low voltage (SDA, INT) | $I_{OL}$ = max, $V_{DD}$ = min | | 0.4 | V |
| $V_{OH}$ | Output high voltage (INT) | $I_{OH}$ = max, $V_{DD}$ = min | 2.4 | | V |
| $I_{IL}$ | Input leakage current | All I/O pins | -1 | +1 | µA |
| $I_{DDPD}$ | Supply current, power-down | $\overline{PD}$ low (Note 4) | | 1.0 | µA |
| $I_{DD}$ | Supply current, active | $\overline{PD}$ high (Note 4) | | 1.1 | mA |

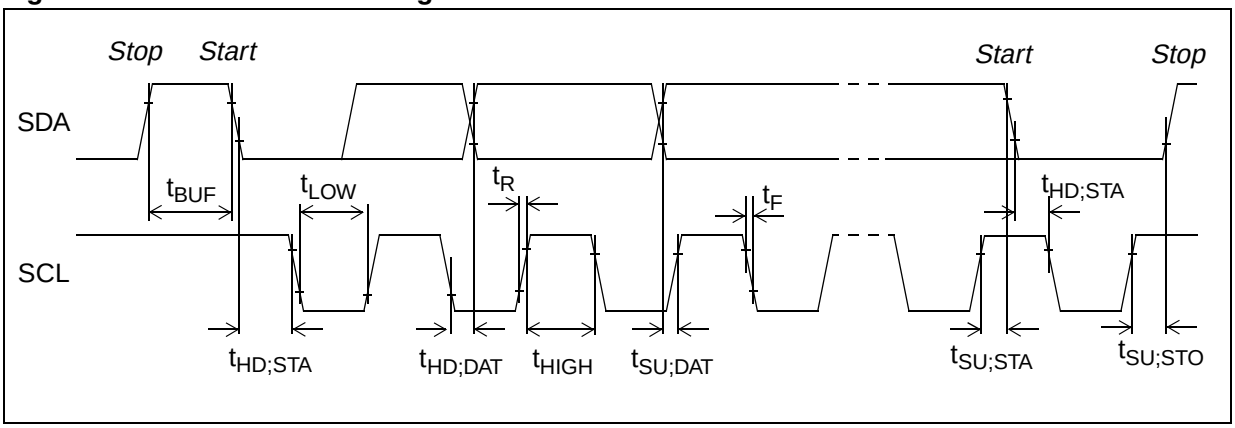
**Table 8. AC electrical characteristics (*Note 3*)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC}$ | Internal oscillator frequency | | | 3.6 | | MHz |

**Table 9. Serial interface timing (*Note 3*)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | kHz |
| $t_{LOW}$ | SCL clock low period | 4.7 | | µs |
| $t_{HIGH}$ | SCL clock high period | 4.0 | | µs |
| $t_{SU;STA}$ | (Repeated) START condition setup time | 4.7 | | µs |
| $t_{HD;STA}$ | (Repeated) START condition hold time | 4.0 | | µs |
| $t_{SU;DAT}$ | Data setup time | 250 | | ns |
| $t_{HD;DAT}$ | Data hold time | 300 | | ns |
| $t_{SU;STO}$ | STOP condition setup time | 4.0 | | ns |
| $t_{BUF}$ | Bus free condition between START and STOP conditions | 4.7 | | µs |
| $t_R$ | Rise time of both SDA and SCL signals | | 300 | ns |
| $t_F$ | Fall time of both SDA and SCL signals | | 300 | ns |
| $C_b$ | Capacitive load for each bus line | | 400 | pF |

**Figure 9. Serial interface timing waveforms**




*Note: 1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

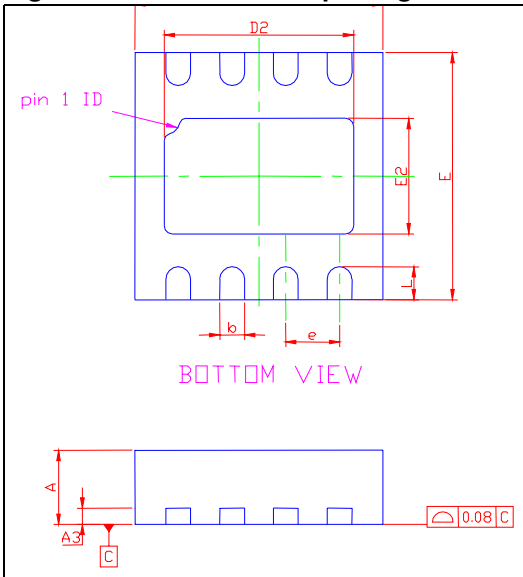
*2 Unless otherwise specified, all voltages are referenced to ground.*

*3 Over recommended operating conditions, unless otherwise specified.*

*4 Using typical operating conditions: $T_A$ = 25 °C, $V_{DD}$ = 3.3 V*

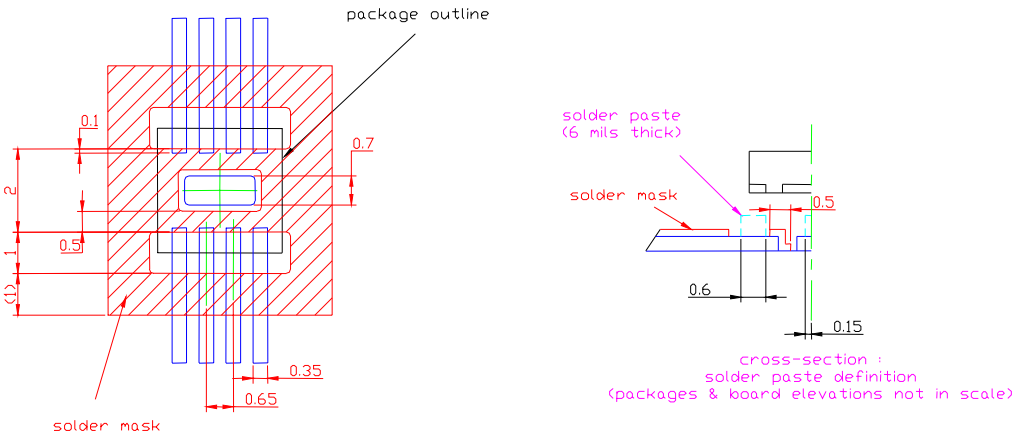
# 7 Mechanical information

**Figure 10. 8-lead MLPD package outline**




| Symbol | Min | Typ | Max |
|---|---|---|---|
| A | 0.65 | 0.7 | 0.75 |
| A3 | | 0.20 | |
| b | 0.25 | 0.30 | 0.35 |
| D | 2.90 | 3.00 | 3.10 |
| D2 | 2.20 | 2.35 | 2.45 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.00 | 1.15 | 1.25 |
| e | | 0.65 | |
| L | 0.55 | 0.60 | 0.65 |
| All dimensions in millimeters | | | |

**Figure 11. Recommended PCB layout**



# 8 Ordering information

**Table 10. Order codes**

| Part number | Description |
|---|---|
| VM6101V008 | 8-lead MLPD 3 x 3 x 0.7 mm, RoHS compliant, tray packing. |
| VM6101V008/TR | 8-lead MLPD 3 x 3 x 0.7 mm, RoHS compliant, 13” tape and reel, 5000 parts/reel. |
| STV-6101-R01 | VM6101 evaluation board |

# 9 Revision history

**Table 11. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 05-Jun-2006 | 1 | Initial release |
| 14-Dec-2006 | 2 | Global update |
| 27-Apr-2007 | 3 | Updated *Chapter 6: Electrical characteristics* and *Chapter 4: Register description* |

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