NEC

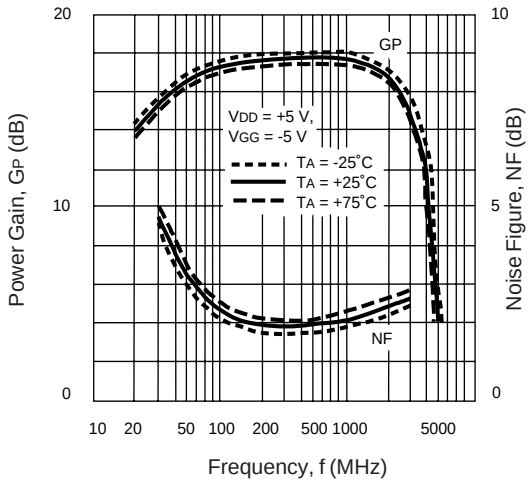
LOW NOISE WIDE-BAND AMPLIFIER

UPG100B UPG100P

FEATURES

- **ULTRA WIDE BAND:** 50 MHz to 3 GHz
- **LOW NOISE:** 2.7 dB TYP at f = 50 MHz to 3 GHz
- **INPUT/OUTPUT IMPEDANCE MATCHED TO 50 Ω**
- **HERMETIC SEALED PACKAGE ASSURES HIGH RELIABILITY**
- **WIDE OPERATING TEMPERATURE RANGE**

POWER GAIN AND NOISE FIGURE vs. FREQUENCY



DESCRIPTION

The UPG100 is a GaAs monolithic integrated circuit designed as a low noise amplifier from 50 MHz to 3 GHz. This device is suitable for low noise IF gain stages in microwave communication and measurement equipment.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD} = +5V, V_{GG} = -5 V, f = 0.05 to 3 GHz, Zs = Z_L = 50 Ω)

PART NUMBER PACKAGE OUTLINE			UPG100B, UPG100P B08, CHIP		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{DD}	Drain Bias Current (RF off)	mA	30	45	60
I_{GG}	Gate Bias Current (RF off)	mA		0.7	1.5
G_P	Power Gain	dB	14	16	
ΔG_L	Flatness Gain	dB			±1.5
NF	Noise Figure	dB		2.7	3.5
P_{1dB}	Output Power at 1 dB gain compression point	dBm	+3	+6	
RL_{IN}	Input Return Loss	dB	7	10	
RL_{OUT}	Output Return Loss	dB	7	10	
ISOL	Isolation	dB	30	40	
$R_{TH\ (CH-C)}$	Thermal Resistance (Channel to Case)	°C/W			33

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DD}	Drain Voltage	V	+8
V_{GG}	Gate Voltage	V	-8
V_{IN}	Input Voltage	V	-3 to +0.6
P_{IN}	Input Power	dBm	+15
P_T	Total Power Dissipation[2]	W	1.5
Top	Operating Temperature	°C	-65 to +125
T_{STG}	Storage Temperature	°C	-65 to +175

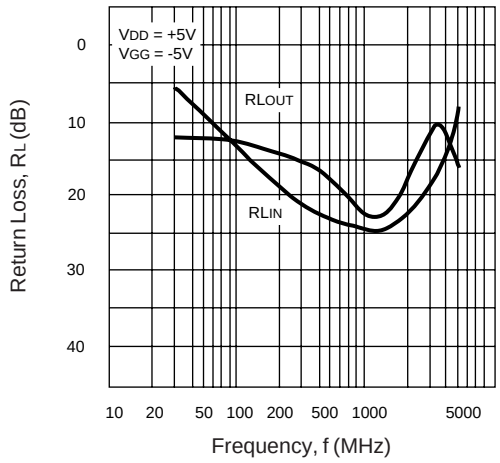
Notes:
1. Operation in excess of any one of these conditions may result in permanent damage.
2. T_{CASE} (T_C) ≤ 125°C

RECOMMENDED OPERATING CONDITIONS

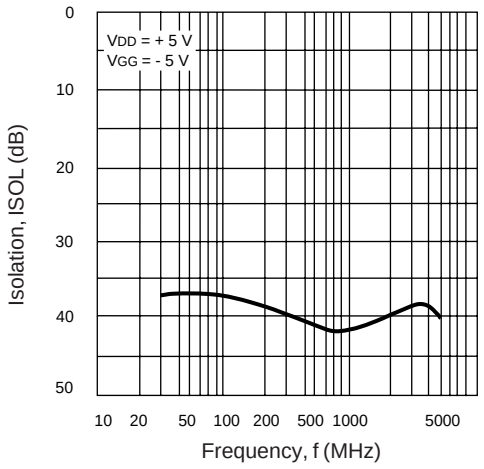
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{DD}	Drain Voltage	V	4.5	5.0	5.5
V_{GG}	Gate Voltage	V	-5.5	-5.0	-4.5
P_{IN}	Input Power	dBm			10
T_{OP}	Operating Temperature	°C	-50	25	+80

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

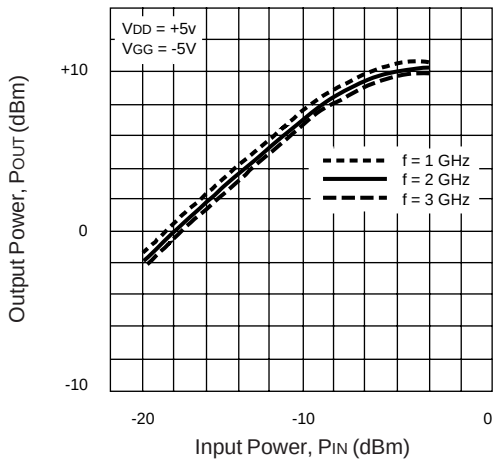
INPUT AND OUTPUT RETURN LOSS vs. FREQUENCY



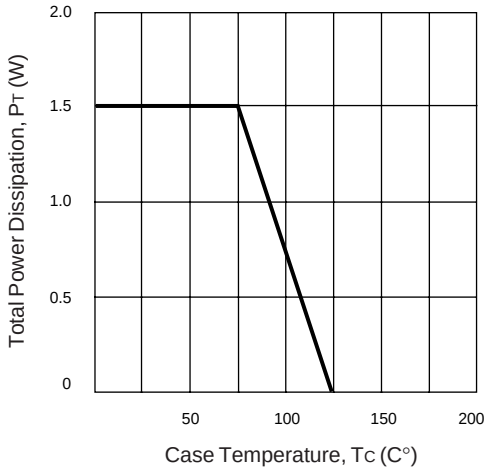
ISOLATION vs. FREQUENCY



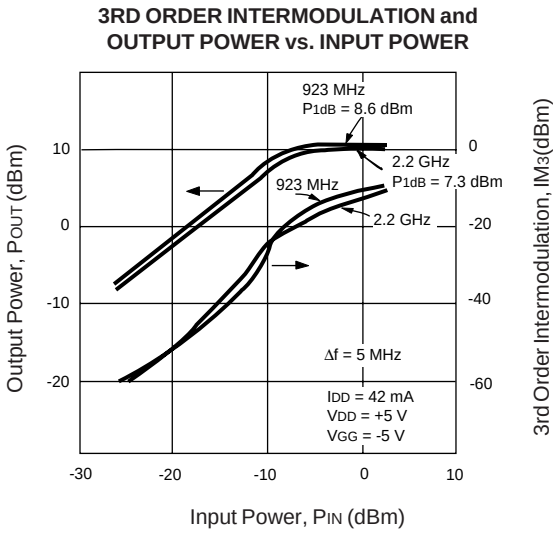
OUTPUT POWER vs. INPUT POWER



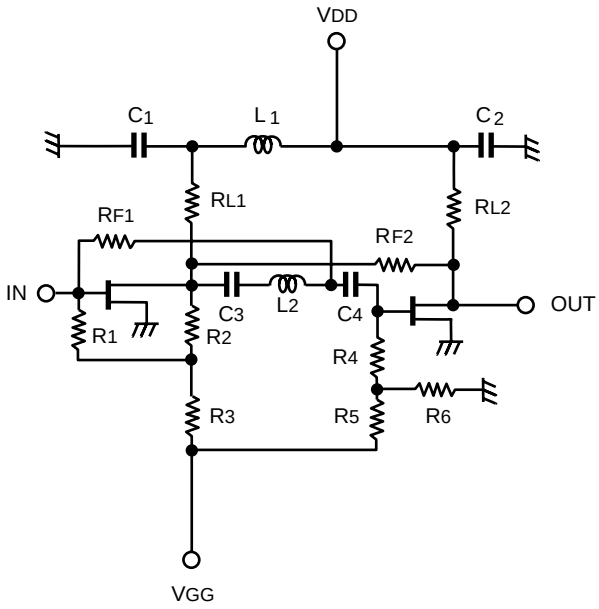
D. C. POWER DERATING CURVE



TYPICAL PERFORMANCE CURVES (TA = 25°C)



EQUIVALENT CIRCUIT



TYPICAL SCATTERING PARAMETERS (TA = 25°C)

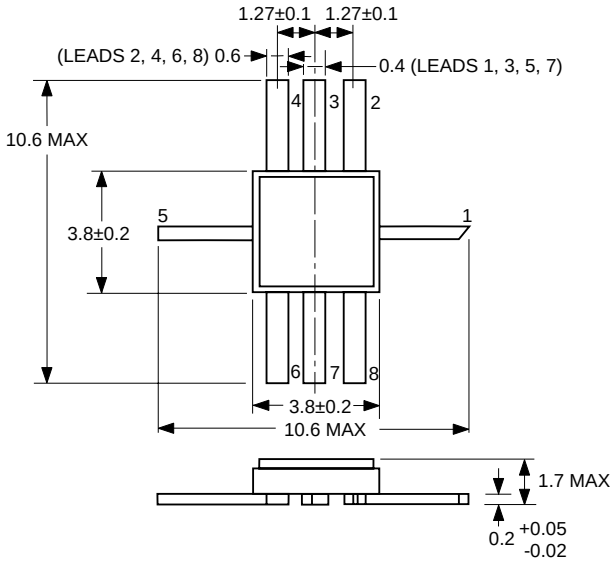
UPG100B

VDD = 5.0 V VGG = -5.0 V

Frequency	S11		S21		S12		S22		k	S21
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG		(dB)
0.1	0.301	-37.5	8.5	23.6	0.009	18.5	0.094	-66.4	5.9	18.6
0.2	0.209	-32.2	8.6	2.5	0.008	7.7	0.048	-61.5	7.0	18.7
0.4	0.194	-33.6	8.9	-17.8	0.008	0.1	0.029	-63.0	6.8	19.0
0.6	0.186	-40.0	9.0	-30.4	0.009	2.8	0.026	-69.6	6.0	19.1
0.8	0.183	-55.6	8.8	-45.6	0.010	-1.5	0.023	-83.6	5.6	18.8
1.0	0.185	-63.1	8.7	-58.1	0.009	1.6	0.022	-110.9	6.2	18.8
1.2	0.182	-79.7	8.7	-71.7	0.012	-7.3	0.030	-163.1	4.7	18.8
1.4	0.157	-94.8	8.5	-83.1	0.011	-20.0	0.034	116.6	5.2	18.6
1.6	0.159	-116.3	8.6	-95.5	0.009	-21.6	0.028	79.5	6.4	18.6
1.8	0.138	-128.1	8.4	-109.1	0.010	-21.9	0.028	69.1	5.9	18.5
2.0	0.135	-142.0	8.9	-123.1	0.009	-9.8	0.033	64.2	6.2	19.0
2.2	0.143	-156.0	8.5	-133.7	0.009	-22.2	0.039	52.6	6.5	18.5
2.4	0.150	-174.3	8.3	-148.1	0.009	1.1	0.039	40.8	6.6	18.4
2.6	0.158	163.8	8.2	-159.6	0.010	-22.8	0.047	38.8	6.0	18.2
2.8	0.172	154.7	8.2	-171.5	0.011	-22.0	0.056	34.8	5.4	18.3
3.0	0.189	137.1	8.0	173.5	0.014	-29.1	0.062	24.8	4.3	18.1
3.2	0.204	127.6	8.1	162.5	0.014	-27.6	0.071	16.6	4.2	18.2
3.4	0.200	111.4	7.8	148.6	0.015	-35.1	0.082	9.5	4.1	17.9
3.6	0.216	107.3	7.8	136.0	0.017	-35.4	0.088	-1.4	3.6	17.8
3.8	0.229	94.0	7.7	123.4	0.019	-38.1	0.099	-12.2	3.3	17.7
4.0	0.231	83.3	7.3	109.8	0.022	-47.6	0.110	-25.0	2.9	17.3
4.2	0.226	77.8	7.3	96.6	0.025	-55.7	0.118	-43.0	2.6	17.3
4.4	0.207	70.2	6.8	84.4	0.027	-62.1	0.127	-64.2	2.6	16.7
4.6	0.164	75.8	6.6	74.8	0.031	-84.1	0.116	-99.6	2.4	16.4
4.8	0.212	89.0	6.8	67.6	0.029	-100.3	0.070	-145.6	2.5	16.7
5.0	0.305	85.6	7.1	51.7	0.022	-100.7	0.013	176.5	3.0	17.1

OUTLINE DIMENSIONS (Units in mm)

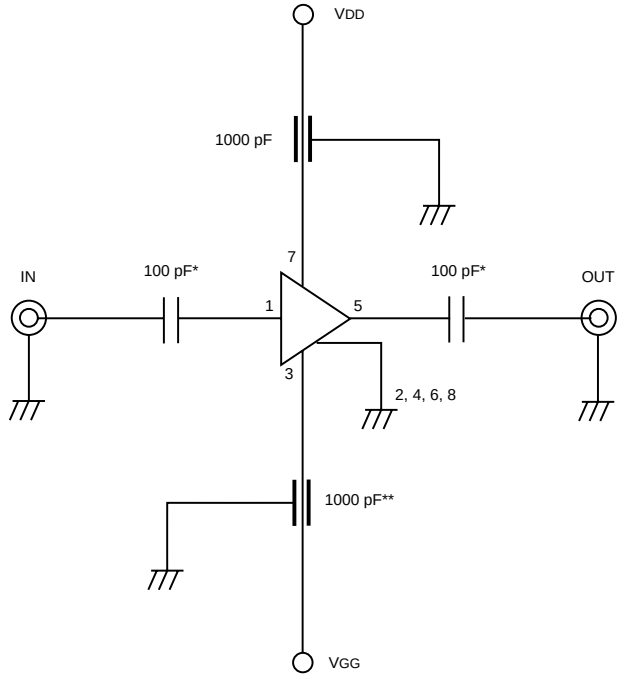
UPG 100B
PACKAGE OUTLINE B08



LEAD CONNECTIONS:

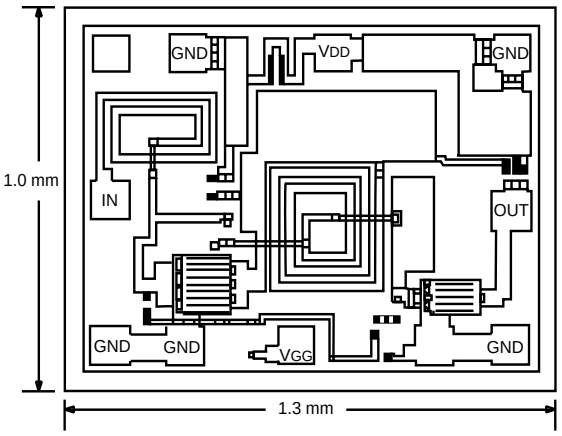
1. INPUT	5. OUTPUT
2. GND	6. GND
3. V_{GG}	7. V_{DD}
4. GND	8. GND

TEST CIRCUIT



* Chip Capacitor
**Recommended when cascading UPG100 with NEC's UPG100, 101, 103B's.

UPG100P (CHIP)



Notes: Bonding Pad Size: 100 µm Square
Distance between Bonding Pad Outer Edge and Die Edge: 70 µm Typical
Chip Thickness: 140± 10 µm

RECOMMENDED CHIP ASSEMBLY CONDITIONS

DIE ATTACHMENT

Atmosphere: N2 gas
Temperature: 320± 5°C
AuSn Preform: 0.5 x 0.5 x 0.05^{t} (mm), 1 piece

The hard solder such as AuSi or AuGe which has higher melting point than AuSn should not be used. Epoxy Die Attach is not recommended.

Base Material: CuW, Cu, Kovar (Other material should not be used)

BONDING

Machine: Thermo-compression bonding. Ultrasonic bonding is not recommended.
Wire: 30 µm diameter Au wire, 10 wires
Temperature: 260 ± 5°C
Strength: 31 ± 3g
Atmosphere: N2 gas

It is critical that GND points be connected to the ground with the shortest possible wire.