Low-Power FM Transmitter / Synthesizer System 26 to 50 MHz

Description

The U3550BM is a radio-frequency IC for analog cordless telephone applications in the 26/50-MHz band (CTO standard). The IC performs full duplex communication. The transmitting and receiving frequency depends on whether the IC is used in the handset or in the base station.

The U3550BM's frequency converter consists of an FM transmitter with switchable output power and receiver Mixer 1 in the same unit. A two-wire bus interface can be used for frequency control as well as for switching the transmitter's power amplifier and the receiver. Fine frequency adjustment of the reference crystal oscillator is programmable.

The receive part is designed for a double-conversion architecture. The incoming radio-frequency signal will be filtered and amplified before reaching the first mixer. At this stage, the RF signal will be converted down to the first intermediate frequency (10.7 MHz) by using a local adjustable oscillator (VCO3). The frequency of this oscillator is controlled by the PLL.
The transmitter part contains two PLL-controlled VCOs. The frequency modulation is accomplished by superposing the incoming audio signal on the first PLL control voltage. In this system, the frequency is a product of mixing VCO1 with local oscillator (VCO3). The FM-modulated carrier is amplified by external power amplifier before entering the output filter and the antenna connector.

Features

- All PLLs and most of the oscillators are integrated
- All functions and channel selection controllable by serial bus
- Receiver Mixer 1 with integrated image rejection
- Up to 25 channels selectable depending on CT0 standard
- Integrated oscillator circuit with external crystal (11.15 MHz)
- Programmable carrier-modulation frequency

Application

- CT0 (USA, France, Spain, Netherlands, Portugal, Korea, Taiwan, New Zealand, China)
- Narrowband voice and data transmitting / receiving systems

Block Diagram

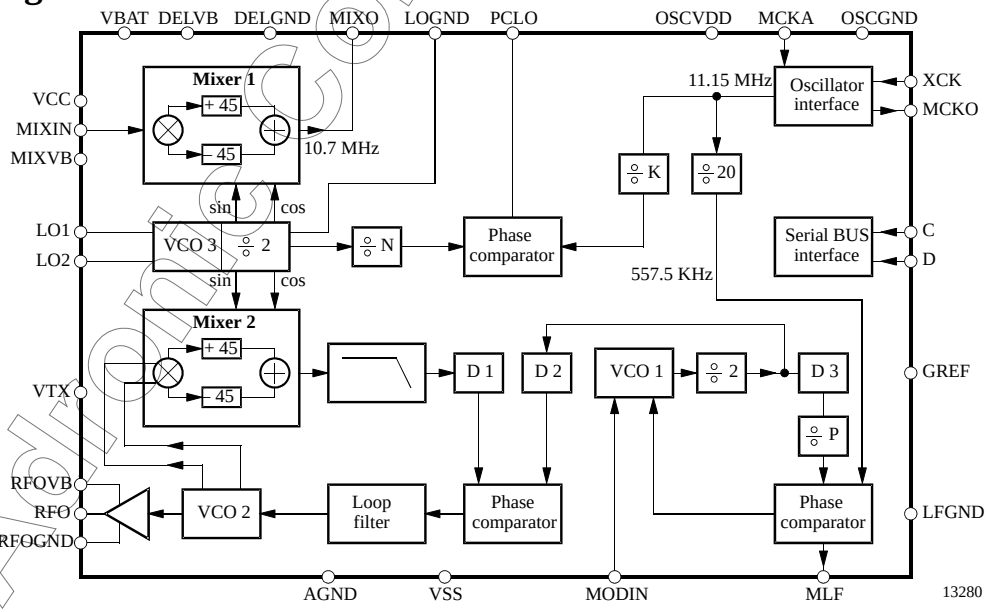


Figure 1. Block diagram

Pin Description

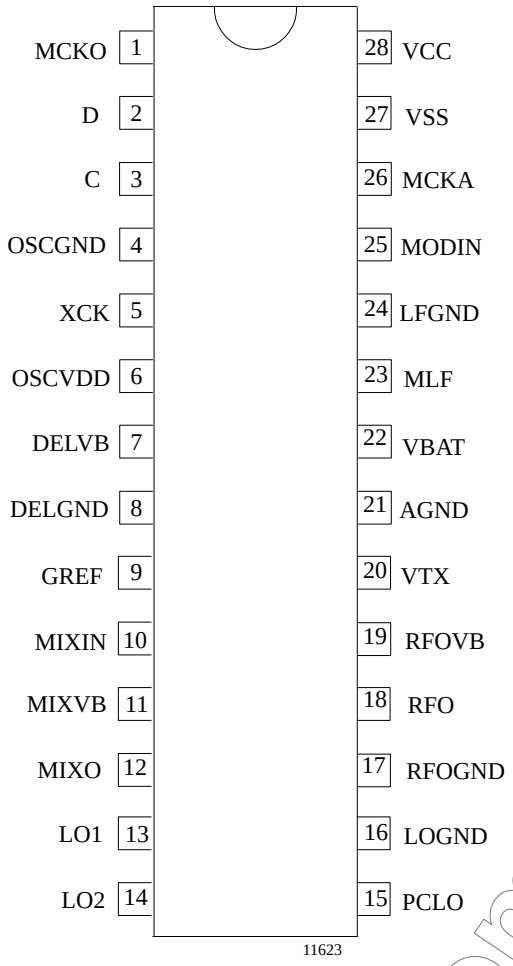


Figure 2. Pinning

Pin	Symbol	Function
1	MCKO	Clock output for peripherals
2	D	Data input of serial bus
3	C	Clock line of serial bus
4	OSCGND	Oscillator ground
5	XCK	Oscillator input (11.15 MHz)
6	OSCVDD	Oscillator supply input
7	DELVB	Phase correction VCO3 supply input
8	DELGND	Phase correction VCO3 ground
9	GREF	Voltage reference for internal current sources
10	MIXIN	Mixer input
11	MIXVB	Mixer-supply input
12	MIXO	Mixer output
13	LO1	Tank elements for LO are connected to these pins
14	LO2	
15	PCLO	Phase comparator PLL3 output
16	LOGND	VCO3 ground
17	RFOGND	RF transmit output ground
18	RFO	RF transmit output
19	RFOVB	Power-supply input of RF transmit output buffer
20	VTX	Power-supply output of RF external power amplifier
21	AGND	Analog ground
22	VBAT	Power supply of analog part
23	MLF	Modulator loop filter
24	LFGND	Modulator loop-filter ground
25	MODIN	Modulator input signal
26	MCKA	Peripheral-clock output adjustment
27	VSS	Digital ground
28	VCC	Power supply of digital part

Order Information

Extended Type Number	Package	Remarks
U3550BM-AFL	SO28	
U3550BM-AFLG3	SO28	Taped and reeled

VCO Adjustments

To be able to use a wide VCO frequency range (i.e., VCO2 = 26.3 to 49.9 MHz), VCO1 and VCO2 have a rough adjust and a fine adjust to increase the frequency range given by the phase comparator.

The 4 rough adjusts for VCO1 and VCO2 (3 used in VCO1) are correlated to the country setting. For each country, there are two sets of VCO rough adjust settings, one for the base and one for the handset (see tables Channel Frequencies, Dividers and Country Settings).

To achieve the adaption to the various country standards, there is a fine adjust with 32 steps for VCO1 and VCO2. These fine adjusts can be set manually (for test purposes) or by the automatically mode. Theoretically, the indicator of the change (increase/ decrease when the voltage of the phase comparator is too high) is selectable. The programming value '1', however, is necessary.

Setting normal conditions VCO1:
EAFA1 = 1, automatic fine adjust VCO1 enabled
SAFA1 = 1, sign of auto fine adjustment VCO1 = 1.

Setting for VCO2 is identical.
For VCO3, there is no internal adjustment.

Speed-up of the Modulator Loop Filter

To obtain a fast locking time for the modulator loop, there is a precharge and a speed-up mode for the external loop filter.

During receive mode (VCO3 enabled, VCO1 disabled), the modulator loop filter is precharged to 1.25 V.

During the first 30 ms after enabling VCO1, the modulator phase comparator is in speed-up mode. In this mode, the current of the phase comparator which charges the loop filter is much larger than in normal mode. The duration of the speed-up mode depends on the number of oscillator clock cycles.

Duration Adjustment of the Anti-Backlash Signals

The phase comparators of the modulator- and the mixer-loop have a 2-bit adjustment for the duration of the up- and down pulses when the loop is locked (anti-backlash).

Best results can be achieved by setting all the bits (AMOD[2:1], AMIX[2:1]) to 0.

Adjustment of the Modulator Gain

To fulfill all requirements of the various countries, three conversion gains of the modulator are selectable by the bits GMOD[1:0].

For country settings, see tables Channel Frequencies, Dividers and Country Settings. For the ranges, see tabel Electrical Characteristics (RF transmitter).

Clock-Output Divider Adjustment

The MCKO pin is a clock output derived from the crystal oscillator. It can be used to drive a microprocessor or other remote components and thereby reduces the number of crystals required.

The crystal oscillator frequency can be divided by an integer value: 1, 2, 3, 4, 6 or switched off.

The divider value is adjusted by an analog level on the MCKA pin.

Table 1 shows the clock-output value on MCKO for different divider values and the corresponding level required on MCKA.

Crystal oscillator = 11.15 MHz.

Table 1. Clock-output values

Level on MCKA	0 to 7% V_{CC}	13% to 27% V_{CC}	33% to 47% V_{CC}	53% to 67% V_{CC}	73% to 87% V_{CC}	93% to V_{CC}
Level on MCKA for V_{CC} = 3.6 V	0 to 0.25	0.47 to 0.97	1.19 to 1.69	1.91 to 2.41	2.63 to 3.13	3.35 to 3.6
Corresponding divider	X	6	4	3	2	1
Corresponding clock on MCKO (MHz)	No output	1.858	2.7875	3.716	5.575	11.15

Frequency Synthesis

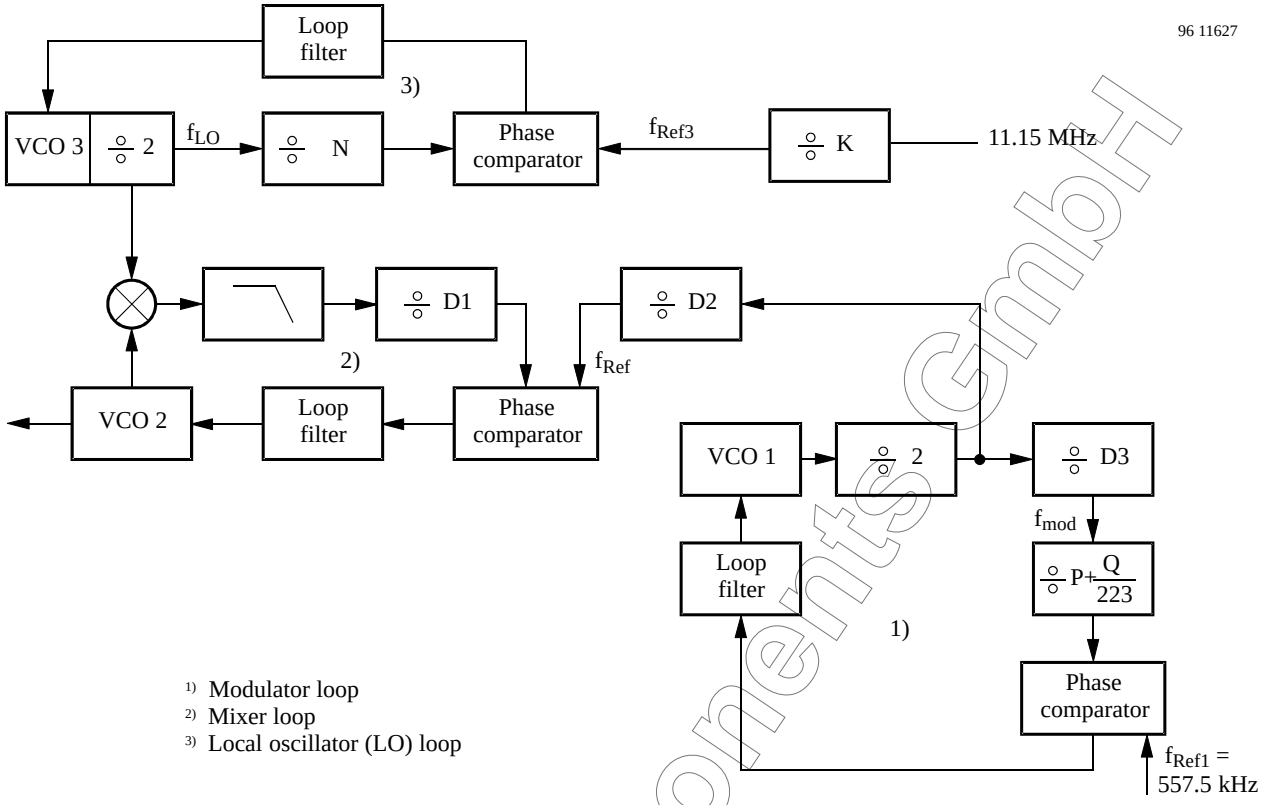


Figure 3.

Modulator Loop and Mixer Loop Dividers

	D1	D2	D3	f_{Ref2} (MHz)	f_{mod} (MHz)
France	4	8	2	1.075	4.3
Spain	2	8	4	0.9	1.8
Netherlands	2	8	4	0.9	1.8
Portugal	2	8	4	0.625	1.25
USA (channels 1 to 10)	8	8	1	0.955	7.64
USA (new channels)	6	6	1	0.943	5.66
Taiwan	8	8	1	0.9625	7.70
New Zealand	4	8	2	0.5875	4.70
Korea	8	8	1	0.955	7.64

For France, Spain, Netherlands, Portugal, Taiwan and New Zealand, f_{Ref2} and f_{mod} do not change when the channel changes. For USA and Korea is valid: f_{Ref2} and f_{mod} are varying according to the channel number. For all countries, f_{Ref2} and f_{mod} are identical for base set and handset.

Reference Frequency Dividers for Local Oscillator

K_0 = 4460
K_1 = 2230
K_2 = 1784
K_3 = 1115
K_4 = 892
K_5 = 446

f_{Ref3} = 2.5 kHz
f_{Ref3} = 5 kHz
f_{Ref3} = 6.25 kHz
f_{Ref3} = 10 kHz
f_{Ref3} = 12.5 kHz
f_{Ref3} = 25 kHz

Modulator PLL

The fractional divider has been chosen to increase reference the frequency of the modulator PLL.

$$557.5\ \text{kHz} = f_{mod} / \left(P + \frac{Q}{223}\right)$$

P: integer part of the fractional divider
Q: fractional part of the fractional divider

$$Q = 223 \times \left(\frac{f_{mod}}{557.5\ \text{kHz}} - P\right)$$

$$223 = \frac{557.7\ \text{kHz}}{2.5\ \text{kHz}}$$

The frequency step 2.5 kHz is a fraction of the reference frequency 557.5 kHz

$$\rightarrow \frac{Qx\ (P + 1) + (223 - Q)P}{223} = P + \frac{Q}{223}$$

For each comparison cycle (f_{Ref1} = 557.5 kHz), the accumulator content is incremented by the Q value and the divider divides by the P value. When the accumulator value reaches or exceeds 223, the divider divides by the value (P + 1). Then, the accumulator holds the excess value (accumulator value – 223). After 223 cycles, the correct division is executed.

Local Oscillator PLL

$$f_{Ref3} = \frac{f_{LO}}{N}$$

Serial Bus Interface

The circuit is remoted by an external microcontroller through the serial bus.

The data is a 12-bit word:

A0 – A3: address of the destination register (0 to 15)

D0 – D7: contents of register

The data line must be stable when the clock is high and data must be shifted serially.

After a 12-clock period, the transfer to the destination register is generated (internally) by a low-to-high transition of the data line when the clock is high.

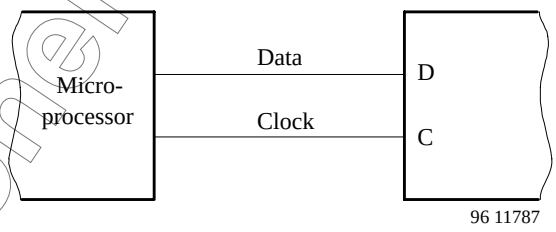


Figure 4.

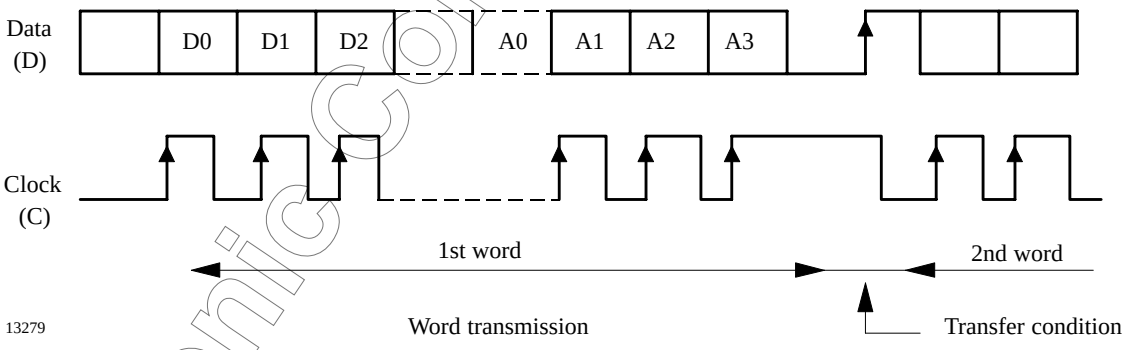


Figure 5. Serial bus transmission

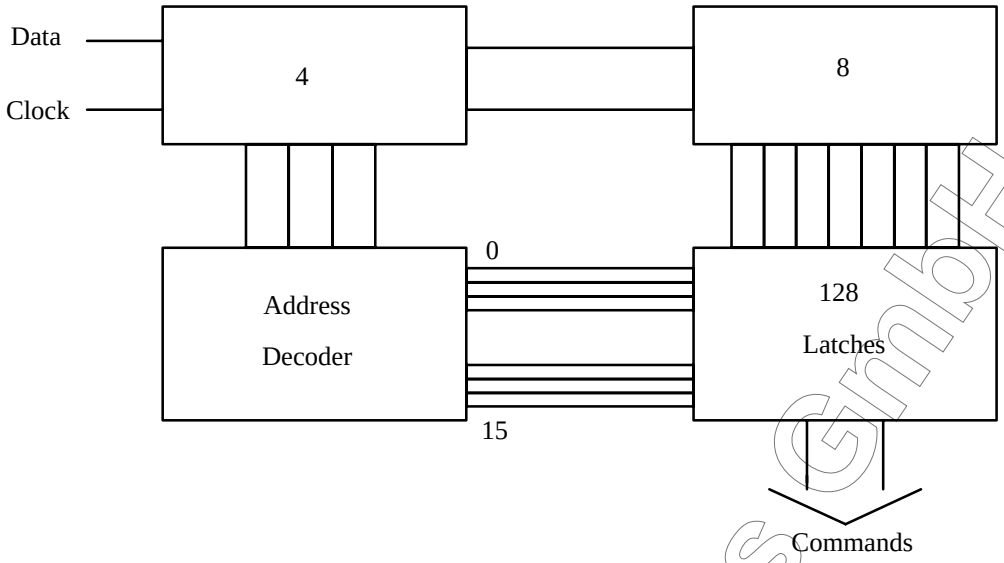


Figure 6.

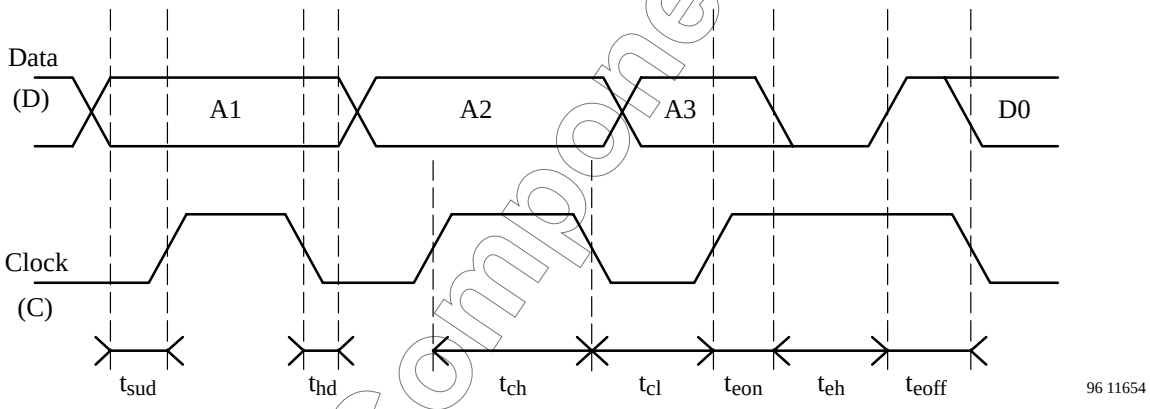


Figure 7.

Content of Internal Registers

The registers have the following structure

D7	D6	D5	D4	D3	D2	D1	D0

R0 – R4: reserved for U3500BM

R5: Gain VCO2

free	free	KV23	KV22	KV21	M12	reserved U3500	

KV2[3:1]: Gain VCO2
M12: Frequency of phase-comparator in Mixer loop

R6: Country setting bits

ETXO	M1CP	UDM1	IMIXI	GMOD1	GMOD0	free	free

ETXO: Enable HF-transmit output
M1CP: Changes 1 dB compression point of Mixer 1
UDM1: Up-/down-mixing of Mixer 1
IMIXI: Inverse inputs of phase comparator in mixer loop
GMOD[1:0]: Modulation gain of VCO1

R7: VCO1 setting

AMOD2	AMOD1	RA11	RA10	DV1I3	DV1I2	DVlI1	DVlI0

AMOD[2:1]: Lengthening anti-backlash signal modulator loop
RA1[1:0]: Rough adjustment VCO1
DVlI[3:0]: Divider setting VCO1 integer part

R8: Divider VCO1 fractional part

DV1F7	DV1F6	DV1F5	DV1F4	DV1F3	DV1F2	DVlF1	DVlF0

DV1F [7:0]: Divider setting VCO1 fractional part

R9: Divider VCO3 integer part LSB

DV3I7	DV3I6	DV3I5	DV3I4	DV3I3	DV3I2	DV3I1	DV3I0

DV3I [7:0]: Divider setting VCO3 integer part LSB

R10: Divider VCO3 integer part MSB

free	DV3I14	DV3I13	DV3I12	DV3I11	DV3I10	DV3I9	DV3I8

DV3I[14:8]: Divider setting VCO3 integer part MSB

R11: Setting VCO2 and VCO3

free	free	FRMT	free	AMIX2	AMIX1	RA21	RA20

FRMT: Output frequency range of Mixer T
AMIX[2:1]: Lengthening anti-backlash signal mixer loop
RA2[1:0]: Rough adjustment VCO2

R12: Divider for country setting, fine adjust oscillator

FAOS2	FAOS1	FAOS0	D31	D30	D20	D11	D10

FAOS[2:0]: Oscillator fine adjust
D3[1:0]: Setting divider D3
D20: Setting divider D2
D1[1:0]: Setting divider D1

R13: VCO1 enable and fine adjust

EVCO1	SAFA1	EAFA1	FA14	FA13	FA12	FA11	FA10

EVCO1: Enable VCO1
SAFA1: Sign for automatic fine adjust VCO1
EAFA1: Enable automatic fine adjust VCO1
FA1[4:0]: Fine adjust VCO1 for manual adjustment

R14: VCO2 enable and fine adjust

EVCO2	SAFA2	EAFA2	FA24	FA23	FA22	FA21	FA20

EVCO2: Enable VCO2 and Mixer T
SAFA2: Sign for automatic fine adjust VCO2
EAFA2: Enable automatic fine adjust VCO2
FA2 [4:0]: Fine adjust VCO2 for manual adjustment

R15: VCO3 enable, oscillator enable, selection of phase comparator VCO3 and speed-up phase comparator for VCO3

EVCO3	EOSC	SU3	E25K	E12K5	E10K	E6K25	E5K

EVCO3: Enable VCO3 and Mixer 1
EOSC: Enable oscillator
SU3: Speed-up phase-comparator for VCO3
E25K: Selection phase-comparator frequency VCO3: f_{Ref3} = 25 kHz
E12K5: Selection phase-comparator frequency VCO3: f_{Ref3} = 12.5 kHz
E10K: Selection phase-comparator frequency VCO3: f_{Ref3} = 10 kHz
E6K25: Selection phase-comparator frequency VCO3: f_{Ref3} = 6.25 kHz
E5K: Selection phase-comparator frequency VCO3: f_{Ref3} = 5 kHz
E5K, E6K25, El0K, E12K5, E25K = 0 Selection phase-comparator frequency VCO3: f_{Ref3} = 2.5 kHz

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S		5.5	V
Junction temperature	T_j		+125	°C
Ambient temperature	T_{amb}	–25	+75	°C
Storage temperature	T_{stg}	–50	+125	°C
Power dissipation T_{amb} = 60°C SO28	P_{tot}		520	mW

Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SO28	R_{thJA}	120	K/W

Electrical Characteristics

T_{amb} = +25°C; V_S = VBAT = MIXVB = RFOVB = DELVB = VCC = OSCVDD; V_S = 3.6 V; f_{MIXIN} = 26.40 MHz, f_{dev} = ±2.5 kHz; V_{MIXIN} = 2.24 mV_{rms}; f_{RFO} = 41.4 MHz; (Fh8) f_{MODIN} = 1.0 kHz; V_{MODIN} = 0.5 V_{rms}; V_{offset} = 1.5 V; V_{MCKA} = V_{CC}; all blocks disabled (ETXO = EVCO1 = EVCO2 = EVCO3 = 0); unless otherwise specified. Test circuit see figure 8.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power supply						
Operating voltage range			3.1	3.6	5.2	V
Operating current in active mode (1)	VBAT = MIXVB = RFOVB = DELVB = 2.9 V OSCVDD = VCC = 0 V				5	µA
Operating current in standby mode, oscillator off (1)	VBAT = MIXVB = RFOVB = DELVB = VCC = OSCVDD = 3.6 V, V_{MCKA} = 0 V, EOSC = 0				200	µA
Operating current in standby mode, oscillator on	VBAT = MIXVB = RFOVB = DELVB = VCC = OSCVDD = 3.6 V, V_{MCKA} = 3.6 V, EOSC = 1				700	µA
Operating current in RX mode	EVCO3 = 1			5	6	mA
Operating current in active mode without TX output	EVCO1 = EVCO2 = 1			12		mA
Operating current in active mode	ETXO = 1, no load at RFO			14	16	mA
RF transmitter						
MODIN input impedance			70	100	130	kΩ
RFO output impedance	Load = 200			300	390	Ω
RFO output-voltage level	ETXO = 0; no load				0.3	V
Lowest operating frequency	France base channel 1 (Fb1) (2)			26.3125		MHz
Highest operation frequency	USA base channel 9 (US1b9) (2)			49.9900		MHz
TX conversion gain RFO – MODIN	Eb1: f_{RFO} = 31.025 MHz US1h9: f_{RFO} = 49.99 MHz Fh6: f_{RFO} = 41.4375 MHz for V_S = 3.1 to 5.2 V			5.7 3.42 2.85		kHz/V kHz/V kHz/V
Demodulated distortion THD	Eb1: Δf = 5.0 kHz Fh9: Δf = 1.5 kHz for V_S = 3.1 to 5.2 V				2	%
Residual modulation (4) on demodulated signal	THD measurement with psophometric filter					dB

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Spurious at RFO output (delta versus carrier)	a/ Fb6: f_{RFO} = 26.375 MHz b/ US1h9: F_{RFO} = 49.99 MHz (3) Δf = ±2.5 kHz Δf = ±12.5 kHz Δf = ±557.5 kHz Δf = ±1/2 f_{mod} Δf = ± f_{mod} for V_S = 3.1 to 5.2 V		60			dBc
VTX output capability	I_{LOAD} = 3 mA ΔV with and without load				0.5	V
VTX output leakage current	ETXO = 0; current to GND				1	µA
PLLs	**V_S = 3.1 to 5.2 V**					
Charge-pump output voltage	EVCO1 =1, output high		2.38	2.5	2.63	V
Precharge voltage at the loop filter	EVCO3 = 1 EVCO1 = 0		1.15	1.4	1.65	V
Charge-pump output current in speed-up mode	EVCO1 = 1 V_{MLF} = 1.25 V, output high		–400	–300	–200	µA
Charge-pump output current	V_{MLF} = 1.25 V, output low		4.3	6.2	8	µA
	V_{MLF} = 1.25 V, output high		–8	–6.2	–4.3	µA
Charge-pump leakage current	V_{MLF} = 1.25 V, output tristate		–100		+100	nA
VCO1 gain	V_{MLF} = 0 V, then 2.5 V		121	140	156	kHz/V
Receiver input mixer (Mixer 1)						
Input frequency range	EVCO3 = 1		20		50	MHz
Output frequency				10.7		MHz
Input resistance			2.4	3.0	3.6	kΩ
Input capacitor			3	3.5	4	pF
Output impedance	M1CP = 0 M1CP = 1		210 50	330 80	390 110	Ω Ω
Voltage gain on MIXO	M1CP = 0 M1CP = 1 for: Fb8: f_{LO} = 30.7 MHz FRF11 = 20 MHz UDM1 = 1 Fb8: f_{LO} = 30.7 MHz FRF21 = 41.4 MHz UDM1 = 0 US1h10: f_{LO} = 57.67 MHz FRF31 = 46.97 MHz UDM1 = 1 for V_S = 3.1 to 5.2 V		9.5 14	12.5 17	15.5 20	dB dB
Noise figure	BW = 1 MHz 50-Ω input impedance			14	18	dB
Input compression point	M1CP = 0 M1CP = 1 50-Ω input impedance		–19 –16	–17.7 –14.3		dBm dBm

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Third order input intercept point	M1CP = 0 M1CP = 1 50-Ω input impedance FRF1 = 41.4 MHz FRF2 = 41.4125 MHz Input level 1 = –30 dBm Input level 2 = –30 dBm		–7 –4	–5 –2		dBm dBm
Image-frequency rejection	Fb8: f_{LO} = 30.7 MHz UDM1 = 0 FRF11 = 41.4 MHz FRF12 = 20 MHz (image) Fb8: f_{LO} = 30.7 MHz UDM1 = 0 FRF21 = 20 MHz FRF22 = 41.4 MHz (image) Fb8: f_{LO} = 57.67 MHz UDM1 = 1 FRF31 = 46.97 MHz FRF32 = 68.37		20			dB
LO to RF MIXIN input isolation	Fb8: measuring, f_{LO} = 30.7 MHz				0.2	mV_{rms}
LO to IF MIXO output isolation	Fb8: measuring, f_{LO} = 30.7 MHz				1.2	mV_{rms}
Isolation transmit path to receive path (crosstalk)	Synthesizer programming as ‘Taiwan channel 5’ (see page 21), transmitter modulation (Pin 25) for Δf = 3 kHz, f_{mod} = 300 to 3400 kHz, M1CP = 1, f_{RF} (Pin 10) = 45.35 or 48.35 MHz unmodulated, –25 dBm (50 Ω) measuring frequency modulation of the 10.7 MHz signal at MIXO (Pin 12)		28			dB
Logical part						
Inputs: C, D Low-voltage input High-voltage input Inputs: C, D, MCKA Input leakage current (0 < VI < VCC)		 V_{il} V_{ih} V_i	 $0.8 \times V_{CC}$ –1		 $0.2 \times V_{CC}$ 1	 µA
Input leakage current Pin XCK (0 < VI < VCC)			–5		5	µA
Output impedance at MCKO			0.5		1.0	kΩ
Serial bus (figure 8) Data set-up rime Data hold time Clock low time Clock high time Hold time before transfer condition Data low pulse on transfer condition Data high pulse on transfer condition		 t_{sud} t_{hd} t_{cl} t_{ch} t_{eon} t_{eh} t_{eoff}	 0.1 0 2 2 0.1 0.2 0.2			 µs µs µs µs µs µs µs

(1) $I_S = I_{VBAT} + I_{VCC} + I_{MIXVB} + I_{RFOVB} + O_{DELVB} + I1OSCVDD$

(2) 1-measure 11.15 MHz at MCKO pin
2-measure FRFO at RFO pin

(3) See country channels

(4) Ratio between demodulated audio level with and without 1-kHz modulation

Fine Adjustment of the Oscillator Frequency

To set the oscillator's frequency exactly to 11.5 MHz, the frequency is adjustable in 8 steps. By adding 3 different internal capacities, the frequency can be reduced. The values of these capacitors are designed to be 0.7 pF (FAO0), 1.4 pF (FAO1) and 2.8 pF (FAO2).

Parameters	Test Conditions / Pins	Min.	Typ.	Max.	Unit
Oscillator frequency without reduction	FAOS (0:2) = 0		11.15		MHz
Changing the oscillator's frequency with FOSC reduction	FAO2 FAO1 FAO0 0 0 1 0 1 0 1 0 0 1 1 1		 100 200 400 700		 Hz Hz Hz Hz

Test Circuit

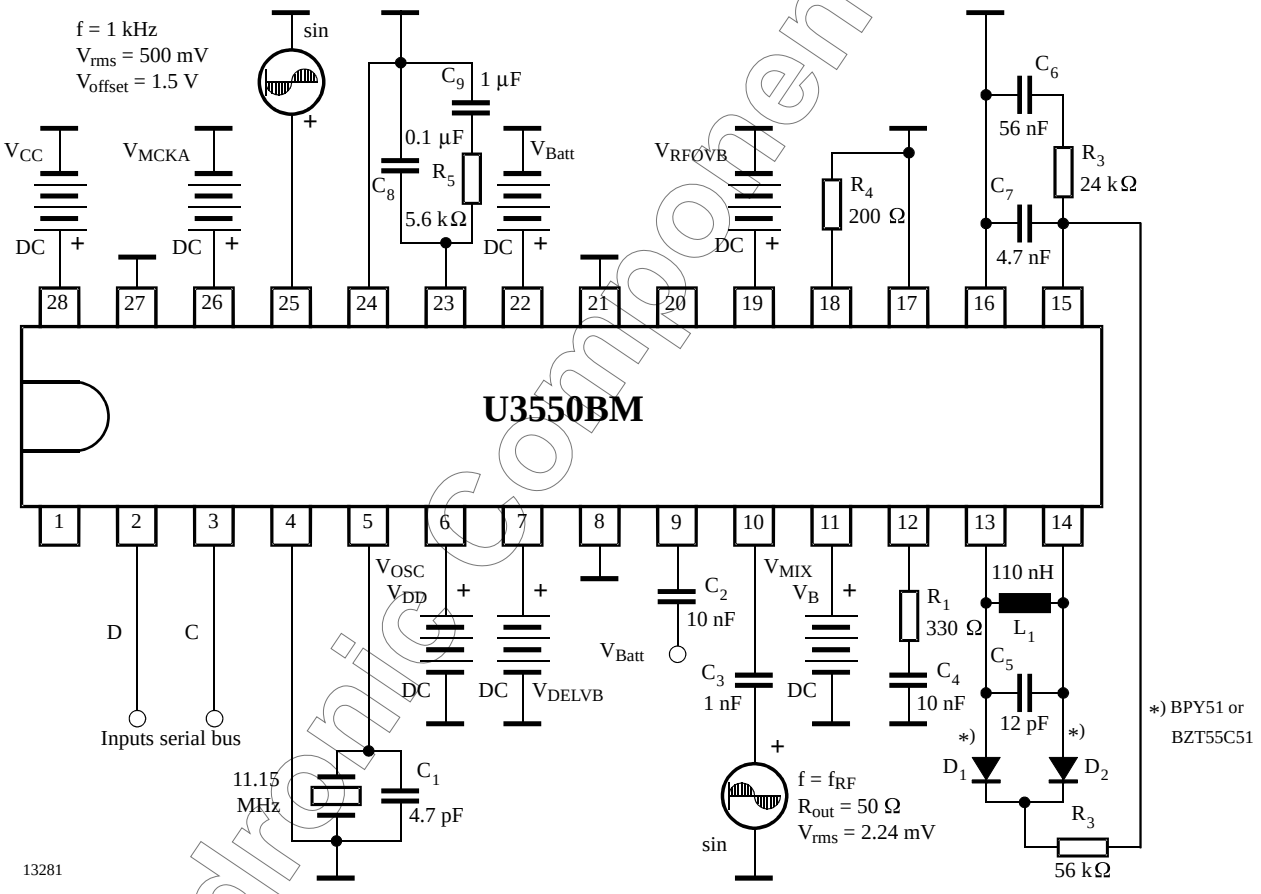


Figure 8. Test circuit

Channel Frequencies, Dividers and Country Settings

To meet all requirements of various countries – France (F), Spain (E), Netherlands (NL), USA and Portugal (P), Korea, Taiwan, New Zealand – and modes – base (b), handset (h) – several bits have to be set which do not change for the different channels. These settings are called country settings.

The country-setting bits are followed by further bits enabling the adjustments given below.

- Rough adjustments for 2 VCOs
- Setting three integer dividers mixer and modulator loop
- Gain adjustment of the VCO2
- Modulator gain
- Up-/down-mixing Mixer 1 and Mixer T
- Output-frequency range of Mixer T

Name Register	Function	Notes	
RA1[0:1]	Rough adjust VCO1	00: is the highest frequency	3
RA2[0:1]	Rough adjust VCO2	00: is the highest frequency	4
D1[0:1]	Integer divider D1	Division by 2, 4, 6, 8	4
D20	Integer divider D2	Division by 6, 8	2
D3[0:1]	Integer divider D3	Division by 1, 2, 4	3
KV[1:3]	Gain VCO2		6
GMOD[0:1]	Modulator gain	00: gain minimal	3
IMIXI	Up-/down-mixing Mixer T	0: if f_{VCO2} lower than f_{LO}	2
UDM1	Up-/down-mixing Mixer 1	1: supra band active (handset)	2
FRMT	Output-frequency range Mixer T	0: for $f_{VCO2} - f_{LO} < 6$ MHz	2

Note: Setting the fractional dividers:
For Q, send the binary equivalent of the numbers given below.
For P (integer part), send the D2 complement (16 – P)
i.e. Fb1 (P = 7, Q = 159 => integer: send 16 – P = 9, fractional: send 159)

France CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	11	11	1	01	100	01	0	0	0
Setting	max	min	4	8	2		mid	supra	infra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	41.3125	30.6125	4898
2	41.3250	30.6250	4900
3	41.3375	30.6375	4902
4	41.3500	30.6500	4904
5	41.3625	30.6625	4906
6	41.3750	30.6750	4908
7	41.3875	30.6875	4910
8	41.4000	30.7000	4912
9	41.4125	30.7125	4914
10	41.4250	30.7250	4916
11	41.4375	30.7375	4918
12	41.4500	30.7500	4920
13	41.4625	30.7625	4922
14	41.4750	30.7750	4924
15	41.4875	30.7875	4926

France CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	01	11	1	01	101	01	1	1	0
Setting	max	high	4	8	2		mid	infra	supra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	26.3125	37.0125	5922
2	26.3250	37.0250	5924
3	26.3375	37.0375	5926
4	26.3500	37.0500	5928
5	26.3625	37.0625	5930
6	26.3750	37.0750	5932
7	26.3875	37.0875	5934
8	26.4000	37.1000	5936
9	26.4125	37.1125	5938
10	26.4250	37.1250	5940
11	26.4375	37.1375	5942
12	26.4500	37.1500	5944
13	26.4625	37.1625	5946
14	26.4750	37.1750	5948
15	26.4875	37.1875	5950

France CT0 Modulation Loop Frequency and Divider

f_{mod} = 4.3 MHz, P = 7, Q = 159

Spain CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	10	00	1	11	100	10	1	0	0
Setting	mid	low	2	8	4		high	infra	infra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	39.925	29.225	4676
2	39.950	29.250	4680
3	39.975	29.275	4684
4	40.000	29.300	4688
5	40.025	29.325	4692
6	40.050	29.350	4696
7	40.075	29.375	4700
8	40.100	29.400	4704
9	40.150	29.450	4712
10	40.175	29.475	4716
11	40.200	29.500	4720
12	40.225	29.525	4724

Spain CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	01	00	1	11	100	10	0	1	0
Setting	mid	high	2	8	4		high	supra	supra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	31.025	41.725	6676
2	31.050	41.750	6680
3	31.075	41.775	6684
4	31.100	41.800	6688
5	31.125	41.825	6692
6	31.150	41.850	6696
7	31.175	41.875	6700
8	31.200	41.900	6704
9	31.250	41.950	6712
10	31.275	41.975	6716
11	31.300	42.000	6720
12	31.325	42.025	6724

Spain CT0 Modulation Loop Frequency and Divider

f_{mod} = 1.8 MHz, P = 3, Q = 51

Netherlands CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	10	00	1	11	100	10	1	0	0
Setting	mid	low	2	8	4		high	infra	infra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	39.9375	29.2375	4678
2	39.9625	29.2625	4682
3	39.9875	29.2875	4686
4	40.0125	29.3125	4690
5	40.0375	29.3375	4694
6	40.0625	29.3625	4698
7	40.0875	29.3875	4702
8	40.1125	29.4125	4706
9	40.1375	29.4375	4710
10	40.1625	29.4625	4714
11	40.1875	29.4875	4718
12	40.2125	29.5125	4722

Netherlands CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	01	00	1	11	001	10	0	1	0
Setting	mid	high	2	8	4		high	supra	supra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	31.0375	41.7375	6678
2	31.0625	41.7625	6682
3	31.0875	41.7875	6686
4	31.1125	41.8125	6690
5	31.1375	41.8375	6694
6	31.1625	41.8625	6698
7	31.1875	41.8875	6702
8	31.2125	41.9125	6706
9	31.2375	41.9375	6710
10	31.2625	41.9625	6714
11	31.2875	41.9875	6718
12	31.3125	42.0125	6722

Netherlands CT0 Modulation Loop Frequency and Divider

f_{mod} = 1.8 MHz, P = 3, Q = 51

USA CT0 Base Set

Country setting channel 1 – 10 (USA1):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	1	0	1
Setting	mid	max	8	8	1		low	infra	infra	high

Country setting new channels (channel 11 – 25, USA2):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	01	01	10	0	00	110	01	1	0	0
Setting	mid	high	6	6	1		mid	infra	infra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 5 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	49.670	38.970	7794
2	49.845	39.145	7829
3	49.860	39.160	7832
4	49.770	39.070	7814
5	49.875	39.175	7835
6	49.830	39.130	7826
7	49.890	39.190	7838
8	49.930	39.230	7846
9	49.990	39.290	7858
10	49.970	39.270	7854

New channels

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
11	48.760	38.06	7612
12	48.840	38.14	7628
13	48.860	38.16	7632
14	48.920	38.22	7644
15	49.020	38.32	7664
16	49.080	38.38	7676
17	49.100	38.40	7680
18	49.160	38.46	7692
19	49.200	38.50	7700
20	49.240	38.54	7708
21	49.280	38.58	7716
22	49.360	38.66	7732
23	49.400	38.70	7740
24	49.460	38.76	7752
25	49.500	38.80	7760

USA CT0 Handset

Country setting channel 1 – 10 (USA1):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	0	1	1
Setting	mid	max	8	8	1		low	supra	supra	high

Country setting new channels (channel 11 – 25 USA2):

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	01	00	10	0	00	110	01	0	1	0
Setting	mid	max	6	6	1		mid	supra	supra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 5 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	46.610	57.31	11462
2	46.630	57.33	11466
3	46.670	57.37	11474
4	46.710	57.41	11482
5	46.730	57.43	11486
6	46.770	57.47	11494
7	46.830	57.53	11506
8	46.870	57.57	11514
9	46.930	57.63	11526
10	46.970	57.67	11534

New channels

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
11	43.720	54.42	10884
12	43.740	54.44	10888
13	43.820	54.52	10904
14	43.840	54.54	10908
15	43.920	54.62	10924
16	43.960	54.66	10932
17	44.120	54.82	10964
18	44.160	54.86	10972
19	44.180	54.88	10976
20	44.200	54.90	10980
21	44.320	55.02	11004
22	44.360	55.06	11012
23	44.400	55.10	11020
24	44.460	55.16	11032
25	44.480	55.18	11036

USA CT Modulation Loop Frequencies and Dividers

N Channel	P	Q	f_{mod} (MHz)
1	13	157	7.640
2	13	95	7.485
3	13	105	7.510
4	13	157	7.640
5	13	123	7.555
6	13	157	7.640
7	13	157	7.640
8	13	157	7.640
9	13	157	7.640
10	13	181	7.700

New channels

N Channel	P	Q	f_{mod} (MHz)
11	10	34	5.66
12	10	10	5.60
13	10	34	5.66
14	10	18	5.62
15	10	10	5.60
16	10	2	5.58
17	10	58	5.72
18	10	50	5.70
19	10	42	5.68
20	10	34	5.66
21	10	66	5.74
22	10	50	5.70
23	10	50	5.70
24	10	50	5.70
25	10	42	5.68

Portugal CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	01	10	00	1	11	010	10	1	0	0
Setting	min	low	2	8	4		high	infra	infra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	37.000	26.300	4208
2	37.025	26.325	4212
3	37.050	26.350	4216
4	37.075	26.375	4220
5	37.100	26.400	4224
6	37.125	26.425	4228
7	37.150	26.450	4232
8	37.175	26.475	4236
9	37.200	26.500	4240
10	37.225	26.525	4244
11	37.250	26.550	4248
12	37.275	26.575	4252

Portugal CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	01	01	00	1	11	001	10	0	1	0
Setting	min	high	2	8	4		high	supra	supra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	27.550	38.250	6120
2	27.575	38.275	6124
3	27.600	38.300	6128
4	27.625	38.325	6132
5	27.650	38.350	6136
6	27.675	38.375	6140
7	27.700	38.400	6144
8	27.725	38.425	6148
9	27.750	38.450	6152
10	27.775	38.475	6156
11	27.800	38.500	6160
12	27.825	38.525	6164

Portugal CT0 Modulation Loop Frequency and Divider

f_{mod} = 1.25 MHz, P = 2, Q = 54

Taiwan CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	110	01	1	0	1
Setting	mid	max	8	8	1		low	infra	supra	higher

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	48.2500	37.5500	6008
2	48.2750	37.5750	6012
3	48.3000	37.6000	6016
4	48.3250	37.6250	6020
5	48.3500	37.6500	6024
6	48.3750	37.6750	6028
7	48.4000	37.7000	6032
8	48.4250	37.7250	6036
9	48.4500	37.7500	6040
10	48.4750	37.7750	6044

Taiwan CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	110	00	0	1	1
Setting	mid	max	8	8	1		low	supra	supra	high

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	45.2500	55.9500	8952
2	45.2750	55.9750	8956
3	45.3000	56.0000	8960
4	45.3250	56.0250	8964
5	45.3500	56.0500	8968
6	45.3750	56.0750	8972
7	45.4000	56.1000	8976
8	45.4250	56.1250	8980
9	45.4500	56.1500	8984
10	45.4750	56.1750	8988

Taiwan CT0 Modulation Loop Frequency and Divider

f_{mod} = 7.70 MHz, P = 13, Q = 181

New Zealand CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	01	11	1	01	110	01	1	0	0
Setting	max	high	4	8	2		mid	infra	infra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
11	40.2500	29.5500	4728
12	40.2750	29.5750	4732
13	40.3000	29.6000	4736
14	40.3250	29.6250	4740
15	40.3500	29.6500	4744
16	40.3750	29.6750	4748
17	40.4000	29.7000	4752
18	40.4250	29.7250	4756
19	40.4500	29.7500	4760
20	40.4750	29.7750	4764

New Zealand CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	00	11	11	1	01	101	01	0	0	0
Setting	max	min	4	8	2		mid	supra	supra	low

Channel frequencies and 1st LO divider, f_{Ref3} = 6.25 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
11	34.2500	44.9500	7192
12	34.2750	44.9750	7196
13	34.3000	45.0000	7200
14	34.3250	45.0250	7204
15	34.3500	45.0500	7208
16	34.3750	45.0750	7212
17	34.4000	45.1000	7216
18	34.4250	45.1250	7220
19	34.4500	45.1500	7224
20	34.4750	45.1750	7228

New Zealand CT0 Modulation Loop Frequency and Divider

f_{mod} = 4.70 MHz, P = 8, Q = 96

Korea CT0 Base Set

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	1	0	1
Setting	mid	max	8	8	1		low	infra	infra	high

Channel frequencies and 1st LO divider, f_{Ref3} = 5 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	49.6700	38.9700	7794
2	49.8450	39.1450	7829
3	49.8600	39.1600	7832
4	49.7700	39.0700	7814
5	49.8750	39.1750	7835
6	49.8300	39.1300	7826
7	49.8900	39.1900	7838
8	49.9300	39.2300	7846
9	49.9900	39.2900	7858
10	49.9700	39.2700	7854
11	49.6950	39.9950	7799
12	49.7100	39.0100	7802
13	49.7250	39.0250	7805
14	49.7400	39.0400	7808
15	49.7550	39.0550	7811

Korea CT0 Handset

Country setting:

Name	RA1[1:0]	RA2[1:0]	D1B[1:0]	D2B0	D3B[1:0]	KV2[3:1]	GMOD[1:0]	IMIXI	UDM1	FRMT
Value	10	00	01	1	00	100	00	0	1	1
Setting	mid	max	8	8	1		low	supra	supra	high

Channel frequencies and 1st LO divider, f_{Ref3} = 5 kHz

Channel Number	RX Channel Frequency (MHz)	1st LO Frequency (MHz)	N
1	46.6100	57.3100	11462
2	46.6300	57.3300	11466
3	46.6700	57.3700	11474
4	46.7100	57.4100	11482
5	46.7300	57.4300	11486
6	46.7700	57.4700	11494
7	46.8300	57.5300	11506
8	46.8700	57.5700	11514
9	46.9300	57.6300	11526
10	46.9700	57.6700	11534
11	46.5100	57.2100	11442
12	46.5300	57.2300	11446
13	46.5500	57.2500	11450
14	46.5700	57.2700	11454
15	46.5900	57.2900	11458

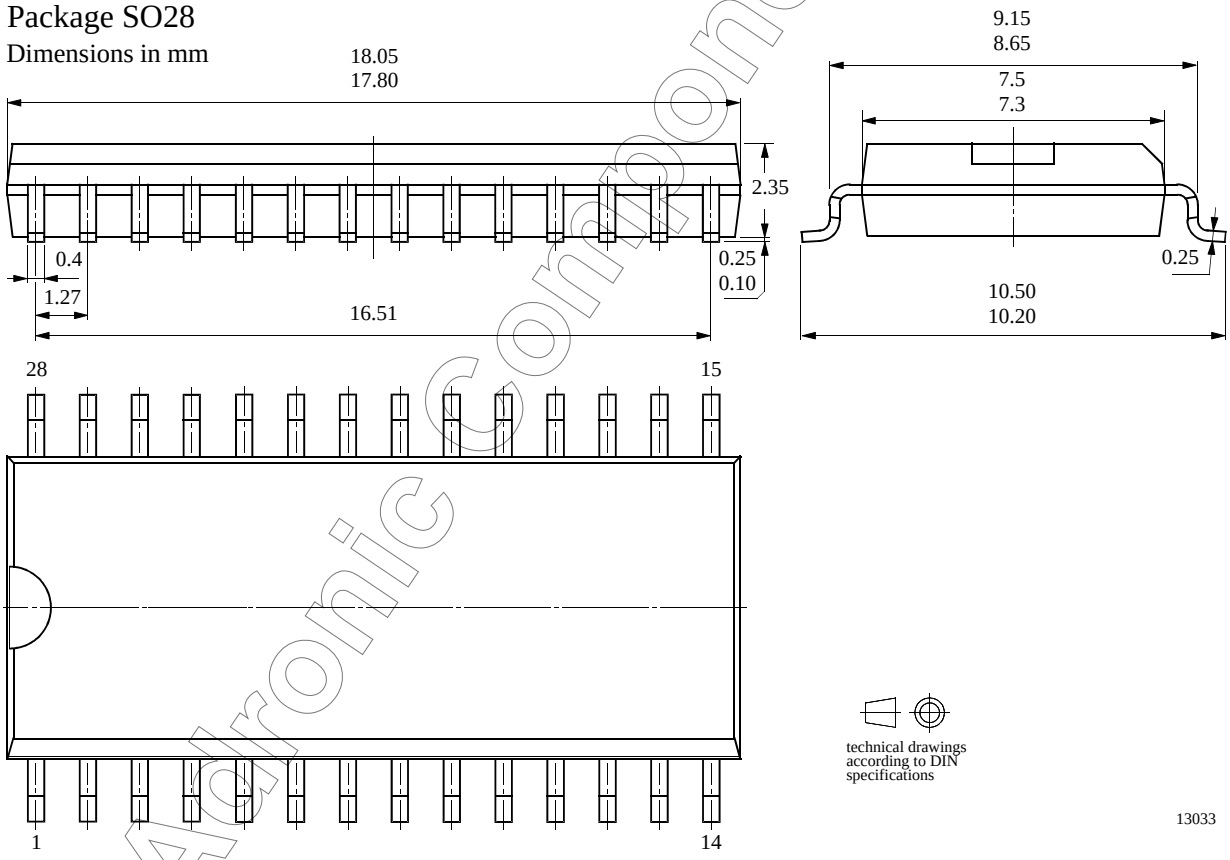
Korea CT Modulation Loop Frequencies and Dividers

N Channel	P	Q	f_{mod} (MHz)
1	13	157	7.640
2	13	95	7.485
3	13	105	7.510
4	13	157	7.640
5	13	123	7.555
6	13	157	7.640
7	13	157	7.640
8	13	157	7.640
9	13	157	7.640
10	13	181	7.700
11	13	107	7.515
12	13	109	7.520
13	13	111	7.525
14	13	113	7.530
15	13	115	7.535

Package Information

Package SO28

Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

TEMIC TELEFUNKEN microelectronic GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423