Data Sheet



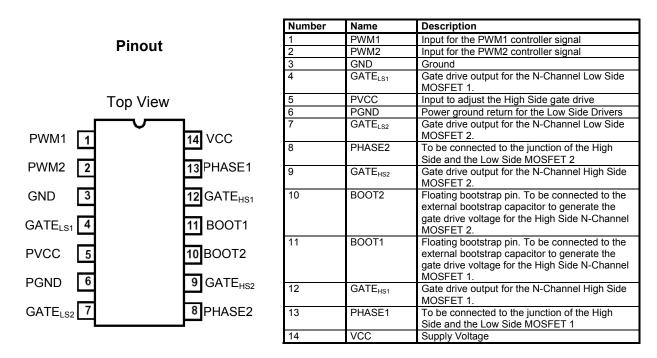
High speed Driver with bootstrapping for dual Power MOSFETs



Features

- Fast rise and fall times for frequencies up to 2 MHz
- Capable of sinking more than 4 A peak current for lowest switching losses
- Charges the High Side and Low Side MOSFET's gate to 6..12 V according to PVCC setting.
- Adjustable High Side and Low Side MOSFET gate drive voltage via PVCC pin for optimizing ON losses and gate drive losses
- Integrates the bootstrap diode for reducing the part count
- Prevents from cross-conducting by adaptive gate drive control
- High voltage rating on Phase node
- Supports shut-down mode for very low quiescent current through three-state input
- Compatible to standard PWM controller ICs (Intersil, Analog Devices)
- Floating High Side MOSFET drive
 - · Ideal for multi-phase Desktop CPU supplies on motherboards and VRM's

Туре	Package	Marking	Ordering Code
TDA21102	P-DSO-14-3	21102	Q67042-S4244





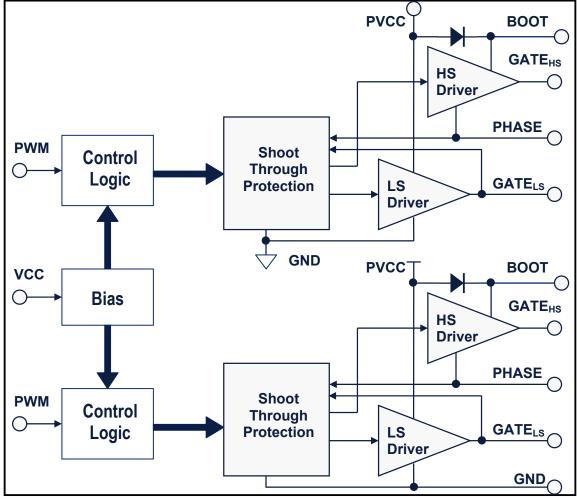
General Description

The dual high speed driver is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges. It has a small propagation delay from input to output, short rise and fall times and the same pin configuration as the HIP6602B. In addition it provides several protection features as well as a shut down mode for efficiency reasons. The high breakdown voltage makes it suitable for mobile applications.

Target application

The dual high speed driver is designed to work well in half-bridge type circuits where dual N-Channel MOSFETs are utilized. A circuit designer can fully take advantage of the driver's capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM's but also in motor drive and class-D amplifier type applications.

Block Diagram





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Absolute Maximum Ratings At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Va	lue	Unit
		Min.	Max.	
Voltage supplied to 'VCC' pin	V _{VCC}	-0.3	25	
Voltage supplied to 'PVCC' pin	V _{PVCC}	-0.3	25	V
Voltage supplied to 'PWM' pin	V _{PWM}	-0.3	5.5	
Voltage supplied to 'BOOT' pin referenced to 'PHASE'	V _{BOOT} – V _{PHASE}	-0.3	25	
Voltage rating at 'PHASE' pin, DC	V_{PHASE}	-1	25	
Voltage rating at 'PHASE' pin, t _{pulse_max} =500ns Max Duty Cycle = 2%		-20	30	
Junction temperature	TJ	-25	150	°C
Storage temperature	Τs	-55	150	
ESD Rating; Human Body Model			4	kV
IEC climatic category; DIN EN 60068-1		55/1	50/56	-

Thermal Characteristic

Parameter	Symbol	Values		Unit	
	-	Min.	Тур.	Max.	
Thermal resistance, junction-case	Rth-JC		44,7		K/W
Thermal resistance, junction-ambient	Rth-JA		116,2		

Electrical Characteristic

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit	
	-		Min.	Тур.	Max.		
Supply Characteristic							
Bias supply current	I _{VCC}	f = 1 MHz,					
		NO LOAD		0.95	1.65		
		$V_{PVCC} = V_{VCC} = 12 V$					
Quiescent current	Ivccq	$1.8~V \leq V_{PWM} \leq 3.0~V$		0.75	3	mA	
Power supply current	I _{PVCC}	f = 1 MHz,					
		NO LOAD		26			
		$V_{PVCC} = V_{VCC} = 12 V$					
Under-voltage lockout		V _{VCC} rising threshold	9.7	10.1	10.5	V	
Under-voltage lockout		V _{VCC} falling threshold	7.3	7.6	8.0	V	
Input Characteristic							
Current in 'PWM' pin	I _{PWM L}	V _{PWM} = 0.4 V	-80	115	-150	μA	
Current in 'PWM' pin	I _{PWM H}	V _{PWM} = 4.5 V	120	180	250		
Shut down window	VIN SHUT	t_ _{SHUT} > 320 ns	1.7		3.1	V	
Shut down hold-off	t_ _{SHUT}	1.7 V \leq V _{PWM} \leq 3.1 V	100	230	350	ns	
time							
PWM pin open	V _{PWM_0}		1.8	2.0	2.2		



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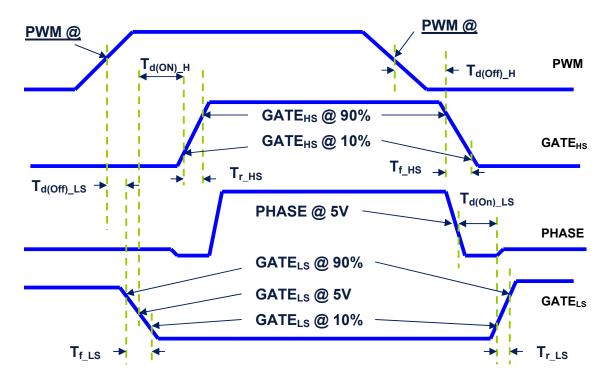
TDA21102

PWM Low level threshold (falling)	V _{PWM_L}		1.45	1.55		V
PWM High level threshold (rising)	V _{PWM_H}			3.45	3.6	
Pulse Width High Side	t_p	= Pulse with on PWM pin	40			ns

At Tj = 25 °C, unless otherwise specified

Dynamic Characteristic							
Turn-on propagation	t _{d(ON)_HS}			27	35		
Delay High Side*							
Turn-off propagation	$t_{d(OFF)_{HS}}$			16	21		
delay High Side							
Rise time High Side	t _{r_HS}			20	25		
Fall time High Side	t _{f_HS}	$P_{PVCC} = V_{VCC} = 12 V$		11	20	ns	
Turn-on propagation	t _{d(ON)_LS}	C _{ISS} = 3000 pF		20	23		
Delay Low Side							
Turn-off propagation	t _{d(OFF)} LS			13	20		
delay Low Side							
Rise time Low Side	t _{r_LS}			22	25		
Fall time Low Side	t _{f_LS}			13	20		

Measurement Timing diagram





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Operating Conditions At Tj = 25 °C, unless otherwise specified

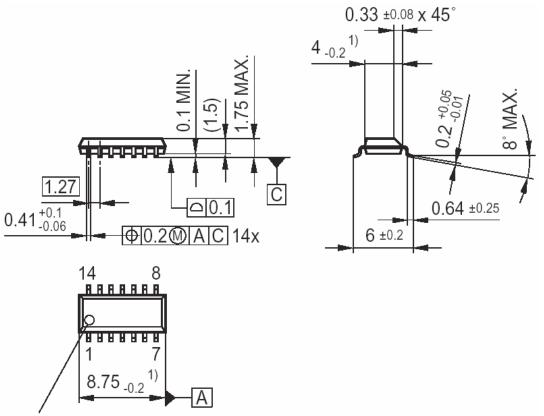
Parameter	Symbol	Conditions	Values			Unit
			Min.	Тур.	Max.	
Voltage supplied to 'VCC' pin	V _{VCC}		10.8		13.2	V
Voltage supplied to 'PVCC' pin	V _{PVCC}		6		13.2	V
Input signal transition frequency	f		0.1		2	MHz
Power dissipation	P _{TOT}	T _A = 25 °C, T _J = 125 °C		0.9		W
Junction temperature	ΤJ		-25		150	°C

At Tj = 25 °C, unless otherwise specified

Parameter		Conditions	Values			Unit
			Min.	Тур.	Max.	
Output Characte	ristic High Side	e (HS) and Low Side (LS), (ensure	ed by d	lesign	
Output	HS; Source	$P_{PVCC} = V_{VCC} = 12 V$		1.2		Ω
Resistance		$I_{HS_{SRC}} = 2 A$				
	HS; Sink	$P_{PVCC} = V_{VCC} = 12 V$		1	1.5	Ω
	LS; Source	$P_{PVCC} = V_{VCC} = 12 V$		1		Ω
		I _{HS SRC} = 2 A				
	LS; Sink	$P_{PVCC} = V_{VCC} = 12 V$		1	1.3	Ω
	HS; Source	$P_{PVCC} = V_{VCC} = 12 V$	4			
Peak output-	HS; Sink	t_ _{P_Hs} / Pulse < 20 ns	4			А
current	LS; Source	t_ _{P_LS} / Pulse < 40 ns	4			
	LS; Sink	D_ _{HS} < 2%, D_ _{LS} < 4%	4			



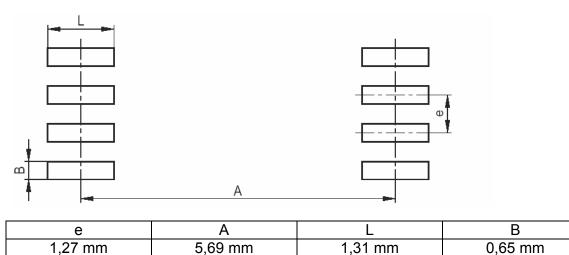
Package Drawing P-DSO-14-3



Index Marking

¹⁾ Does not include plastic or metal protrusion of 0.15 max. per side

Layout Footprints





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